CHAPTER - 5

EZ - SOURCE INVERTER FED INDUCTION MOTOR DRIVE

5.1. Introduction

The Voltage Source Inverter (VSI) based system has the following theoretical barriers and limitations.

- The AC output voltage is limited below and cannot exceed the DC voltage.
- The upper and lower devices of each phase leg cannot be switched on simultaneously.
- An output LC filter is needed for providing a Sinusoidal voltage.

The Current Source Inverter (CSI) based system has the following theoretical barriers and limitations.

- At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the DC inductor would occur and destroy the devices.
- Overlap time for safe current commutation is needed in the current source converter, which also causes waveform distortion, etc.

Impedance Source (Z - Source) Inverter is used to overcome the problems in the conventional source inverters. It employs a unique impedance network coupled with the inverter main circuit to the power source. This performs fast energy conversion using L and C as impedance network. So far, various Z - source methods have been developed with either voltage or current type conversion ability [1] - [4].

73
Therefore, instead of using an external LC filter, this work proposes an alternative family of Embedded Z-source (referred to as EZ-source in short, where “E.M.F” is embedded into Z-network) inverters, which adopts the concept of embedding the input DC sources within the LC impedance network. Using its inductive elements for current filtering in voltage-type EZ-source inverters, and its capacitive elements for voltage filtering in current-type EZ-source inverters, the proposed EZ-Source is shown in Fig. 5.1.

Despite these modifications, the voltage or current gain of the inverters is kept unchanged, as can be proven mathematically. The proposed EZ-source inverters [25] are therefore competitive alternatives that can be used for cases where implicit source filtering is critical. The concepts have been tested extensively in the laboratory using experimentally constructed two and three-level neutral-point-clamped (NPC) inverters.

Fig. 5.1: EZ-Source Inverter
5.2.  EZ Source Inverter

The EZ-source inverter shown in Fig. 5.1 has its DC sources embedded within the X-shaped LC impedance network with its inductive elements $L_1$ and $L_2$ respectively, used for filtering the currents drawn from the two DC sources without using any external LC filter. Quite obviously, the immediate disadvantage shown in Fig. 5.1 is that two DC sources of $V_{dc}/2$, instead of the single DC source are needed for the EZ-source inverter. Although this requirement can at times translate to a slightly higher cost, it is not a major issue for Photo Voltaic Cell or even fuel-cell applications.

The Impedance Source Inverter (ZSI) is originally designed for usage, since the isolated sources can simply be obtained by rerouting the existing panels or cell units already needed in producing the required voltage and current ratings. Therefore, it is not viewed as a serious limitation and can definitely be outweighed by advantages exhibited by the EZ-Source Inverter, including its inherent filtering ability. These advantages are more clearly illustrated by analyzing the inverter operating principle, which again involves Shoot-Through (ST) and Non-Shoot-Through (NST) states produced by a modulator that can be equally used for controlling EZ- and Z-source inverters.

Noting that there is again an inductive element placed along all current paths in the DC front-end, the switches from the same phase-leg can, as usual, be turned ON simultaneously to introduce a Shoot-Through (ST) state without damaging semiconductor devices. The resulting equivalent circuit is shown in Fig. 5.2 (a)-(b), where it is shown that when the inverter bridge is Shoot-
Through (ST), the front-end diode D is reverse biased with its blocking-voltage expression and other state equations written as follows.

**Shoot-Through**

\( S_x = S_x' = \text{ON}, x = A, B, \text{or } C; D = \text{OFF} \)

\[
\begin{align*}
v_L &= V_C + V_d/2 \\
v_i &= 0 \\
v_d &= v_D = -2V_C & \quad \ldots 5.1 \\
i_L &= -i_C \\
i_i &= i_L - i_C \\
i_{dc} &= 0 & \quad \ldots 5.2
\end{align*}
\]

Assuming that now the inverter returns back to its Non-Shoot-Through (NST) active or null state, the redrawn equivalent circuit is shown in Fig. 5.2.(b) with diode D conducting and the inverter bridge and external (usually inductive) load replaced by a current source, whose value is nonzero for active state and zero for null state. Using this equivalent circuit, the second set of state equations is derived as follows.

**Non-Shoot-Through**

\( S_x \neq S_x', x = A, B, \text{or } C; D = \text{ON} \)

\[
\begin{align*}
v_L &= V_d/2 - V_C \\
v_i &= 2V_C \\
v_d &= v_D = 0 & \quad \ldots 5.3 \\
i_{dc} &= i_L + i_C \\
i_i &= i_L - i_C \\
i_{dc} \neq 0 & \quad \ldots 5.4
\end{align*}
\]

76
Fig. 5.2: Equivalent circuits of EZ-Source Inverter when in (a) Shoot Through and (b) Non-Shoot-Through states.
Performing state-space averaging then results in

\[ V_c = \frac{V_{dc}/2}{1 - 2T_o/T} \]

\[ \tilde{v} = \frac{v_k}{1 - 2T_o/T} = Bv_k \]

\[ \tilde{v}_i = M\tilde{v}_i = B(M \frac{v_k}{2}) \].....5.5

The above Equation 5.5 compared with Impedance Source Inverter (Z-Source) [1], clearly shows that both Z - Source and EZ - Source inverters produce the same transfer gain even though the EZ - Source inverter has its DC sources embedded within the impedance network for achieving inherent filtering. Observing carefully, a second advantage is also noted in (5.5) when comparing its capacitive voltage \( V_c \) with that expressed in Impedance Source (Z-Source) Inverter [1], to be specific, \( V_c \) in (5.5) is only a fraction of that in Impedance Source (Z-Source) Inverter with their ratio mathematically expressed as

\[ \frac{V_{c(ZS)}}{V_{c(EZ)}} = \frac{1}{2(1 - \frac{T_o}{T})} \].....5.6

Where the subscripts in (5.6) represent the numbering of the respective \( V_c \) expressions. Noting that \( T_o/T \) is always less than 0.5; the ratio in (5.6) is calculated to span from 0.5 to 1 as \( T_o/T \) rises from 0 to 0.5, inferring that the second advantage introduced by embedding the sources is a significant reduction of the capacitor sizing (voltage rating). The reduction is as much as 50% under nominal condition during which \( M \) is set close to unity (or 1.15 if triple offset is injected) and \( T_o/T \) is kept small. Qualitatively, the gaining of this
favorable feature can also be explained by understanding that the embedded sources now help to partially maintain the required voltage level within the impedance network, allowing the X-shaped capacitors to carry a lower voltage than that found in the Z-Source as network reviewed in Chapter 4.

Proceeding on to identify other characteristic features of the EZ-Source Inverter, Equation (5.5) is substituted into (5.1), (5.2), (5.3), and (5.4) to derive the following set of additional equations.

\[ v_D = \frac{-v_{dc}}{1 - 2T_e/T} \]

.....5.7

Inductor voltage

\[ v_L = V_{dc} \frac{(1 - T_d/T)}{(1 - 2T_e/T)} \quad \text{During Shoot-Through} \]

\[ v_L = -V_{dc} \frac{(T_d)}{(1 - 2T_e/T)} \quad \text{During Non-Shoot-Through} \quad \text{.....5.8} \]

Comparing with Impedance Source Inverter (Z-Source) [9], it is obvious that the EZ-source inverter does not need a diode with higher blocking voltage and these does not occur any changes to its inductive-current ripple for the same commanded Shoot-Through (ST) duration \( T_d/T \). Also noting that the average inductive current \( I_L = I_i = I_{dc} \) (where uppercase "I" represents average value) is the same for both Z-Source and EZ-Source inverters. The same design criteria are expected to indifferently apply on them if those typical modes stated in [10] are to be avoided.

Although the two-level EZ-source inverter shown in Fig. 5.1 uses two independent DC sources for producing a balanced front-end impedance
network, in practice, it is not necessary for both sources to be balanced. For the extreme case, one of the sources can in fact be omitted. The omission of one source is in principle favorable to the industry, where locating a single source is definitely much easier. Relevant mathematical analysis and experimental testing for the case of only a single source powering the EZ-source inverter have already been presented by the authors in [16], where it is generally concluded that a single source is sufficient, if unbalanced voltage drops across the front-end passive LC elements are acceptable. In addition to [16], the same analysis can also be found in [20] - [21].

5.3. Simulation Results

5.3.1. Impedance Source Inverter (Z - Source) fed Induction Motor Drive

The simulation is done using MATLAB/ SIMULINK and the results are presented here.

![Figure 5.3. (a): Z - Source Inverter fed Induction Motor Drive](image)

Fig. 5.3. (a): Z - Source Inverter fed Induction Motor Drive
Fig. 5.4.(a): Line voltages

Fig. 5.4.(b): Line currents
Fig. 5.4.(c): Rotor speed

Fig. 5.4.(d): FFT analysis

Fundamental (50Hz) = 31.88, THD = 5.73%
The SIMULINK model of Impedance Source Inverter (Z-Source) fed Induction Motor Drive is shown in Fig. - 5.4. (a) Shows the line voltages. Fig - 5.4. (b) Shows the line currents. The variation of speed with reference to time is shown in Fig - 5.3. (c). The F.F.T. analysis is done and spectrum is shown in Fig - 5.3. (d). The T.H.D. value is 5.73%.

5.3.2. EZ - Source Inverter fed Induction Motor Drive

The SIMULINK model of EZ source inverter fed Induction Motor Drive is shown in Fig - 5.5. The increase in ripple is due to the shifting of the source. The line voltages are shown in Fig - 5.6. (a). They are displaced by 120°. The variation of speed with reference to time is shown in Fig - 5.6. (c). The rotor speed increases and settles at 50 r.p.s. The F.F.T

Fig. 5.5: EZ - Source Inverter fed Induction Motor Drive
analysis is done for the stator current and the spectrum is shown in Fig. 5.6.(d). The T.H.D is 4.83%. Thus the T.H.D. of EZ source inverter fed Induction Motor Drive is slightly less than that of Z - Source fed Induction motor system.

![Fig. 5.6.(a): Line voltages](image)

![Fig. 5.6. (b). Line currents](image)
Fig. 5.6 (c): Rotor speed

Fig. 5.6 (d): FFT analysis
5.4. **Hardware Implementation**

The hardware of EZ source inverter system is fabricated in the laboratory and it is tested. The hardware circuit is shown in Fig. 5.7.

![Hardware Circuit](image)

*Fig: 5.7: Hardware Circuit*

The hardware consists of power board and control board. AC input voltage is shown in Fig. 5.8 (a). Switching pulses for M1 and M3 are shown in Fig. 5.8 (b).
5.4.1. Hardware Implementation Results

Fig. 5.8. (a): Input voltage

Fig. 5.8. (b): Switching Pulse for M1, M3
Fig. 5.8.(c): Switching Pulse for M1, M5

Fig. 5.8.(d): Line Voltage
Switching pulses for M1 & M5 are shown in Fig 5.8.(c). Line voltage is shown 5.8.(d). Phase voltage is shown in Fig 5.8.(e).

5.5. Conclusions

EZ Source Inverter fed Induction Motor Drive is modeled and simulated using MATLAB 6a/SIMULINK. The results of Impedance Source Inverter (Z-Source) and EZ-Source Inverter fed Induction Motor Drive systems are presented.

Frequency spectrum indicates that T.H.D value of EZ - Source Inverter fed Induction Motor Drive system is 1% less than that of Impedance Source (Z - Source) Inverter system. The EZ - Source system has advantages like shoot-through capability, boosting ability and reduced T.H.D. Therefore, EZ - Source fed Induction Motor Drive system is a viable alternative to the existing drive systems. The experimental results are similar to the simulation results.
5.6 General Hardware Implementation description

Both Z – Source & EZ – Source Inverter fed Induction motor drive consists different components. They are listed below as

1. Power supply circuit
2. PIC Microcontroller 16F84A
3. Optocouplers
4. AT89C2051 Microcontroller
5. IC IR2110 for the amplification of the pulses given by 16F84A.
6. MOSFETs

5.6.1 Power Supply Circuit

Both Z – Source & EZ – Source Inverter fed Induction motor drive consists the following power supply circuit shown in figure.

![Fig.5.9: Power Supply Circuit](image-url)
FEW SIGNIFICANT POINTS REGARDING THE POWER CIRCUIT

- A step-down transformer (230/15) V is used to give input supply to the power circuit.
- The 15V AC input is rectified into 15V pulsating DC with the help of full bridge rectifier circuit.
- The ripples in the pulsating DC are removed and pure DC is obtained by using a capacitor filter.
- The positive terminal of the capacitor is connected to the input pin of the 7812 regulator for voltage regulation.
- An output voltage of 12V obtained from the output pin of 7812 is fed as the supply to the pulse amplifier.
- An output voltage of 5V obtained from the output pin of 7805 is fed as the supply to the micro controller.
- From the same output pin of the 7805, a LED is connected in series with the resistor to indicate that the power is ON.

5.6.2. PIC CONTROLLER

In this project the hardware is implemented using the Pic-Microcontroller “Pic 16F84A”. The advantages of the Pic- microcontroller is that the instruction set of this controller are fewer than the usual microcontroller. Unlike Conventional processors, which are generally complex, instruction set computer (CISC) type, Pic microcontroller is a RISC processor.
The advantages of RISC processor against CISC processor are:

1. RISC instructions are simpler and consequently operate faster.

2. A RISC processor takes a single cycle for each instruction, while CISC processor requires multiple clocks per instruction (typically, at least three cycles of throughput execution time for the simplest instruction and 12 to 24 clock cycles for more complex instruction), which makes decoding a tough task.

3. The control unit in a CISC is always implemented by a microcode, which is much slower than the hardware implemented in RISC.

The idea of using the Pic microcontroller is because:

1. To employ the frequently used instructions as the instruction set while using a few instructions to achieve the same function performed by a much more complex instruction in a CISC.

2. The RISC itself has a large number of general purpose registers, largely reduced the frequency of the most time-consuming memory access.

3. In terms of clock rate, the RISC with its much simpler circuits can have a higher clock rate that again increases the performance of a processor.

Overall the RISC processor can provide processing power more than three times of a CISC processor in a particular field of application.
Features of PIC-microcontroller “Pic16F84A”

The Features and Pin diagram of Pic 16F84A are indicated below

- Only 35 single word instructions to learn
- All instructions single-cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of Data RAM
- 64 bytes of Data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 Special Function Hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt-on-change
  - Data EEPROM write complete
5.6.3 Optocouplers

There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronics equipment, or from one piece of equipment to another, without making a direct electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a Triac which is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from over voltage damage.
Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they're electro-mechanical, relays are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an optocoupler. These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation.

Optocouplers typically come in a small 6-pin or 8-pin IC package, but are essentially a combination of two distinct devices: an optical transmitter, typically a gallium arsenide LED (light-emitting diode) and an optical receiver such as a phototransistor or light-triggered Diac. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. The basic idea is shown in Fig, along with the usual circuit symbol for an Optocoupler.

The most important parameter for most Optocouplers is their transfer efficiency, usually measured in terms of their current transfer ratio or CTR. This is simply the ratio between a current change in the output transistor and the current change in the input LED which produced it. Typical values for CTR range from 10% to 50% for devices with an output phototransistor and up to 2000% or so for those with a Darlington transistor pair in the output. Note, however that in most devices CTR tends to vary with absolute current level. Typically it peaks at a LED current level of about 10mA, and falls away at both higher and lower current levels. Other Optocoupler parameters include the
output transistor’s maximum collector-emitter voltage rating $V_{CE\text{ (max)}}$, which limits the supply voltage in the output circuit; the input LED maximum current rating $I_{F\text{ (max)}}$, which is used to calculate the minimum value for its series resistor; and the Optocouplers bandwidth, which determines the highest signal frequency that can be transferred through it determined mainly by internal device construction and the performance of the output Phototransistor.

5.6.4 AT89C2051 MICROCONTROLLER

The AT89C2051 is a low-voltage, high performance CMOS 8-bit microcomputer with 2K Bytes of Flash programmable and erasable read only memory. The device is manufactured using ATMEL high-density nonvolatile memory technology and is compatible with the industry standard MCS-51 instruction set. By combining a versatile 8-bit CPU with flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer, which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C2051 provides the standard following features: 2K bytes of flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timers/counters, a five vector two level; interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic operation down to zero frequency and supports two software selectable powers saving down to zero frequency and supports two software selectable power saving modes. The idle mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue
functioning. The power Down Modes saves the RAM contents but freezes the oscillator disabling all other chip functions until there next hardware reset.

PIN CONFIGURATION

![Pin diagram of AT89C2051](image)

**Fig 5.12: Pin diagram of AT89C2051**

OPERATING DESCRIPTION

The details descriptions of the AT89C2051 include in description are

- Memory map and register
- Timer/counter
- Other information
- Flash memory

MEMORY MAP AND REGISTERS

The ATM89C2051 has separate address spaces for program and data memory. The program and data memory can be up to 64KB long. The lower 4k program memory can reside on-chip.
The ATM89C2051 has 129 bytes of on-chip RAM plus number of special function registers. The lower 128 bytes can be accessed either by direct addressing or by indirect addressing.

The lower 128 bytes of RAM can be divided into three segments as

- Register banks 0-3
- Bit addressable area
- Scratch pad area.

5.6.5 IR 2110 – HIGH AND LOW SIDE DRIVER

- Some of the features of IR 2110 are:
  - Floating channel designed for bootstrap operation
  - Gate drive supply range from 10 to 20V
  - Under voltage lockout for both channels
  - 3.3V logic compatible
  - Separate logic supply range from 3.3V power ground ± 5V power ground ± 5V offset
  - CMOS Schmitt-triggered inputs with pull down
  - Cycle by cycle edge-triggered shutdown logic
  - Matched propagation delay for both channels
  - Outputs in phase with inputs

The IR2110 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. It is fully operational to +500V or +600V and tolerant to negative transient voltage dv/dt immune. Logic inputs are compatible with standard CMOS or LSTTL output,
down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction.

Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Fig 5.13: Pin Diagram of IR2110

IR2110/DIP14
**LEAD DEFINITIONS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Logic Supply</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate drive output (HO), in phase</td>
</tr>
<tr>
<td>SD</td>
<td>Logic input for shut down</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic ground</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>

**5.6.6 MOSFET**

The following sections describe the components used and their properties affecting the design of multi-level inverter. The MOSFET or Metal Oxide Semiconductor Field Effect Transistors by the far most common field effect transistor in both digital and analog circuits. The MOSFET is composed of a channel of n-type or p-type semiconductor material, and is accordingly called as NMOSFET or a PMOSFET. Unfortunately, many semiconductors with better electrical properties than silicon such as gallium arsenide do not form good gate oxides and thus are not suitable for MOSFETS.
The gate terminal is a layer of poly silicon (polycrystalline silicon) or aluminum placed over a channel, but separated from the channel by a thin layer of insulating silicon dioxide. A simplified diagram of the N-channel enhancement MOSFETS is shown in figure. Drain and source connections are made to higher conduction high doped regions. The metal gate is electrically isolated from the P-type substrate by a layer of non-conducting silicon oxide (SiO2). When a positive voltage is applied to the gate with respect to the source an electric field will be created pointing away from the base and across the P-region directly under the base. The electric field will cause positive charges in the P-region to move away from the base inducing or enhancing an N-region in its place.

Conduction can then take place between the N+ (drain) N (enhanced region) N+(source). Increasing or decreasing in size thus controlling conduction. Varying the voltage between the gate and body modulates the conductivity of this layer and makes it possible to control the current flow between drain and source.

*Fig 5.14: Simple model of an N-channel enhancement type MOSFET*
In practice, a fairly large current in the order of 1-2A can be required to charge the gate capacitance at turn ON to ensure that switching times are small. Due to gate leakage current, nano-amps are needed to maintain the gate voltage once the device is ON. A negative voltage is often applied at turn OFF to discharge the gate for speedy switch OFF. It is obvious that faster switching speeds can be obtained with well-designed gate driver circuits.

**FEATURES OF POWER MOSFETS**

Power MOSFET has lower switching losses but its on-resistance and conduction losses are more. MOSFET is a voltage-controlled device. MOSFET has positive temperature co-efficient for resistance. This makes parallel operation of MOSFET easy. If a MOSFET shares increased current initially, it heats up faster its resistance rises and this increased resistance causes this current to shift to other devices in parallel. In MOSFET secondary break down does not occur, because it has positive temperature co-efficient. Power MOSFETS in higher voltage ratings have more conduction losses.

**IRF 840 - POWER MOSFET**

1) Dynamic dv/dt Rating
2) Repetitive Avalanche Rated
3) Fast switching
4) Ease of paralleling
5) Simple Drive requirements
DESCRIPTION

The IRF-840 provides fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.