ABSTRACT

In recent years parallel and distributed computing has become very popular as it provides a means to overcome the limitations imposed by sequential computers. A common situation in parallel systems is one in which a set of processors have to access a set of memory modules or processors. Obviously, connecting every processor to all memory modules through direct links is not an efficient solution. Multistage Interconnection Networks (MINs) achieve the full access property with far fewer connections and hence have become very popular. In the future, multistage switching architectures are also expected to be used in broadband integrated services digital networks (B-ISDN) and transport systems based on the asynchronous transfer mode (ATM). An MIN consists of a stack of switching elements interconnected with permuters. The MINs are usually designed for N inputs and N outputs using m X m switching elements. In this thesis a new multistage interconnection network is proposed and analysed. Architecture, fault tolerance, routing, simulation, performance evaluation and cost estimation are taken as the points for analysis. Analysis of three more multistage interconnection networks is also reported to highlight the superiority of the proposed network. The analysis shows that though the proposed network is irregular and has fewer switching elements than a conventional multistage network, it maintains full access property. Since, the proposed network provides larger number of paths between the two modules being connected, bandwidth offered by this network is larger than other multistage interconnection networks. The analysis shows that the proposed network has better reliability and throughput than other networks. Comparison with other networks justifies this venture. Fault tolerance of proposed network can be increased by increasing a term K. However, cost of network increases, as the fault tolerance increases. In multiprocessor applications, where the communication is largely localised and intense within small sets of processors and memory modules, and where the communication delay is of less relevance than throughput and reliability, the proposed network performs better than conventional regular and other irregular multistage interconnection networks of same size.