Chapter – III

EXPERIMENTAL

In order to investigate the objectives discussed and set in chapter-II, appropriate Schottky diode structures are required to be fabricated considering various essential aspects e.g. nature of chosen metal and semiconductor, feature of structural definition and their compatibility for mounting in sample holding arrangement etc. All these and related measurements require certain infrastructure facilities. Such infrastructure facilities may spread over a variety of things like furnaces, cleaning and washing facilities, vacuum coating unit, data acquisition and analysis facilities etc. A brief description of some of the important infrastructure facilities, (existing, accumulated and modified) used in present studies consist of –

(1) Vacuum coating unit.
(2) Sample holding arrangements.
(3) Data acquisition facilities for Current-Voltage(I-V) and Capacitance-Voltage(C-V) measurements.

3.1 VACUUM COATING UNIT:

In present investigations the box vacuum coater unit model BC 300, supplied by Hind High Vacuum Co. Ltd. Bangalore was used for fabricating and processing the requirements of metal-semiconductor junctions. The coating unit comprises of diffusion pump backed by a rotary pump with a liquid nitrogen trap to create vacuum of the order of 3X10^-7 torr. Although different materials can be evaporated to form their thin films by different techniques viz. (i) thermal evaporation (ii) e-beam evaporation and (iii) sputtering; thermal evaporation technique has been used in deposition of metal films required in the present study.
A systematic operation of a vacuum system helps in maintaining long life of the system along with obtaining a rated pump down time. Hence a proper sequence in the timings of operating roughing, backing and baffle valves and pouring liquid nitrogen in the trap is required to be critically observed for attaining ultimate vacuum in minimum time. The vacuum chamber, after loading the substrate to be coated, may be allowed to follow ion-cleaning process. For this the required level of vacuum is about $10^{-2}$ to $10^{-3}$ torr. Since clean and chemically non-interacting processes are necessary to be followed, particularly in case of semiconductor devices, the vacuum system after achieving the ultimate vacuum is normally isolated from the pumping system and flushed thoroughly by an inert gas like argon with the help of rotary pump only. The argon pressure of the order of $10^{-2}$ torr is generally utilised for ion-cleaning process. After doing this again the system is allowed to achieve its ultimate vacuum and then the thin film deposition process may be started. The vacuum level can be monitored by thermocouple gauge and pirani gauge and ultimate pressure is measured with the help of Bayard Alpert ionisation gauge for better accuracy. Additionally, a quartz crystal thickness monitor is arranged to measure the thickness of the deposited material. At any stage of deposition the thickness may be controlled by bringing an externally accessible shutter between the source and the substrate. The rate of deposition may be controlled by the control knobs, which supply power to the evaporation source. The complete unit is fitted with various safety interlocks for electrical connections and proper pressure levels.

3.2 SAMPLE HOLDING ARRANGEMENT:

For the study of liquid metal–semiconductor contacts a specially designed sample holder as shown in Fig. 3.1 was constructed and used. The large thermal capacity copper base of this sample holder has been used to mount the prepared silicon crystal and the back contact has been bonded with this base using a highly conducting adhesive silver paste (Eltech-1229C). The upper clean surface was then allowed to come in direct contact with the liquid metal filled into various capillaries that can be positioned as required by moving up and down by
Fig. 3.1 Sample holding arrangement for liquid metal-semiconductor Schottky contacts.
a D.C. motor. For external measurements platinum wires from the top end of the capillaries are used to have contact with the liquid metal in order to complete the circuit with the copper base back contact.

3.3 DATA ACQUISITION FACILITIES:

Amongst various characterising techniques used to investigate Schottky barrier devices, the electrical characteristics viz Current-Voltage and Capacitance-Voltage measurements lead to evaluation of some fundamental parameters as well as some other parameters, which can be used as ready reference during selection of a device for particular application. Apart from evaluation of certain basic device parameters, this can also be used to study the dominating charge transport mechanism at measurement temperature, insulating oxide layer thickness at the interface and interface state density etc. All these aspects may be covered if a full flexible data acquisition scheme is adopted for dc and ac measurements at a required bias voltage within the chosen temperature region.

Thus, in the present study of electrical measurements on prepared devices the data acquisition system has been arranged in two separate modes viz. (i) I-V-T (dc) measurements and (ii) C-V-T (ac) measurements.

3.3.1 I-V-T (dc) Measurements:

For dc measurements of current-voltage characteristics a high sensitivity electrometer of Keithly make (model 614) has been arranged with 8085 microprocessor based programmable voltage source as shown in Fig.3.2. This voltage source has been developed to cover the range of 0 to 1 Volt in forward bias with 5-mV step and 0 to −10 V in reverse bias with 50 mV step.

To facilitate these measurements over a wide temperature range (77K to 360 K) a glass research cryostat (Scientific Solution –Mumbai) has been used with a cryocontroller (model CAT-601) as shown in Fig. 3.2. The fabricated
Fig. 3.2 Glass research cryostat for I-V and C-V measurements at low temperatures.
devices were mounted on a gold-plated copper base of sample holder and the leads for electrical connections were bonded on the devices with the help of conducting silver paste. One common contact comes from the copper base where the back aluminium evaporated contact has already been bonded using silver paste. This sample holder was then inserted in a steel pipe making a cylindrical long vacuum jacket and evacuation was done using a rotary pump. The whole assembly was then placed in a glass cryostat and liquid nitrogen was poured into it. The temperature was measured using Silicon / GaAs diode and controlled with an accuracy of 0.1 K. At a set and desired temperature the current–voltage characteristics can be then recorded with the help of the data acquisition system described above.

3.3.2 C-V -T (ac) Measurements:

These measurements have been designed to analyse the ac characteristics of prepared devices with super imposed dc bias voltages. For this the Hewlett–Packard digital LCR meter (model 4274A with frequency range from 100 Hz to 100 kHz) along with a dedicated computer was used to work in HP-Basic environment for programming the measurement parameters e.g., frequency and dc bias voltage and its step size also(Fig.3.3). The LCR meter has accuracy of 0.01pF for capacitance measurements, which is most suitable part when one has to measure low capacitances and their variation with bias voltage and temperature.

For evaporated metal-semiconductor Schottky devices a glass cryostat scheme was directly used. But for liquid metal-semiconductor device a specially designed sample holder with capillaries to hold the liquid metal was used and the variation in temperature was made using a thermoelectric cooler coupled with a high thermal capacity copper base. The whole arrangement was then placed in a vacuum deccicater and various electrical leads were taken out for thermoelectric cooler supply, thermocouple and device connections. A chromel-alumel thermocouple was used to measure the temperature of measurements (Fig. 3.3).
Fig. 3.3 Thermoelectric cooler based low temperature measurement set-up for measuring ac and dc parameters of liquid metal-semiconductor Schottky contacts.
3.4 SURFACE PREPARATION TECHNIQUES FOR DEVICE FABRICATION:

Schottky barrier devices are surface barrier devices in their various planer geometries with its major integrated circuit forms. Apart from their power device structures majority of the structures are formed over the bare semiconductor surfaces. The properties of solids differ very remarkably at the terminations of 3-D lattice on the surfaces, which leaves unstable chemical and electronic states on the surfaces. In addition to this, the way in which the terminations are produced may also lead to deviations in the desired structure of surfaces e.g. defects, out diffusion of impurities, local flaws, dangling bonds etc. Hence surface preparation techniques i.e. cleaning, etching and passivation of semiconductor surfaces have drawn attention of researchers to obtain the desired kind of surface properties for the development of devices. These techniques in general are primarily aimed at following aspects of surface modifications for the semiconducting substrates-

(I) Cleaning - to provide clean semiconductor surfaces from various kinds of contaminations e.g. organic contamination and metallic particulates etc.

(II) Etching –to bare and smoothen the semiconductor surface and

(III) Passivation - to have saturated surfaces for long time stability required for further processing.

These steps are required for almost all semiconductor surfaces and only the ways by which they are achieved differ according to the nature of chosen semiconductor. These steps are also an integral part of the whole device fabrication process as the semiconductor materials are brought into device quality shape by passing through various processes like crystal growth, cutting, polishing, cleaning etching and passivation. Therefore various routes to do these have been framed and they are centered around the optimization of conditions to have the desired kind of surfaces.
Since the present investigations are centered around silicon as the substrate material, a brief review of surface preparation techniques in case of silicon are described briefly over here.

3.5 CLEANING AND ETCHING PROCESSES:

Since the bare surfaces of silicon are known to react with the ambient atmosphere to acquire an oxide layer, it is very essential to wash, etch and passivate its surface for the required metallic contact i.e. preparation of the surface for device fabrication. Both wet and dry etching and cleaning methods have been evolved with time. However, the mostly used are the wet cleaning methods. Since in present investigations the wet cleaning method has been used, a brief description about cleaning formulation available and those, that have been used here, are described briefly.

3.5.1 Dry Processes:

Dry type of processes for substrate cleaning and etching [1] are generally used at the final stages after washing the substrates thoroughly in the sequence involving deionized water (DI), chemical reagents (like detergent solution, ether, alcohol etc.) and again by DI water. The residues of these steps may generally be evaporated by heating the substrates under high vacuum and following it by etching using the ion cleaning process. For this, the inert gas is leaked into the vacuum chamber to create the required low pressure and then the ions of inert gas are generated by applying high electric potential between cathode and ground electrodes. The high energy ions generated in this way strike the substrate surfaces and remove top layers leaving behind a fresh layer which is then utilised for device fabrication work.

In this context the work of David Kinosky [2] can be referred for cleaning of Si (100) surfaces by hydrogen plasma for removal of oxygen and carbon and subsequent etching of Si surface. Electron cyclotron plasma and aerosol jet
cleaning have also been tried by Zhimin et al. [3] and Po-Sheng et al. [4] for etching and cleaning of Si substrates for device fabrication work.

3.5.2 Wet Processes:

The wet cleaning and etching methods [1] are frequently used techniques for commercial device fabrication work. In present work also some wet cleaning and etching sequences have been identified and used for surface preparation of p-type silicon substrates. Noteworthy amongst these techniques are RCA cleaning sequence [5] which involves solution of NH$_4$OH, H$_2$O$_2$, H$_2$O and HCl, H$_2$O$_2$, H$_2$O for quick removal of metal complexes and organic contaminations. This generates smooth silicon surfaces of hydrophilic nature with low oxide coverage.

The cleaning sequence adopted in this work are:-

(i) Washing in boiling DI water for five minutes. This not only removes contaminations but the etching nature of boiling DI water also helps in removing the upper layer of substrate surface and thus it tends to provide a smooth surface. This has been used in each cleaning step before using other wet chemical formulations for various purposes. Two kinds of wet formulations have been used -

(ii) (a) A mixture of electronic grade HNO$_3$ (79% by weight), HF (49% by weight) and CH$_3$COOH acids with 4:1:3 proportions have been used. This provides etching by oxidation-reduction process which is followed by dissolution of oxidation products. In this process nitric acid acts as an oxidant and hydrofluoric acid dissolves the oxidised products. The isotropic nature of etching by this HNO$_3$ rich solution provides smoother surfaces with thin oxide layer.
(b) A wet etching formulation consisting of electronic grade HF:HN03:CH3COOH in 1:3:3 proportions has also been used for surface cleaning and etching.

(iii) Last step used involves a brief dip into HF:H2O (1:9) solution and it provides surfaces terminated by hydrides. Such surfaces are referred as hydrophobic in nature and are less susceptible to changes in the ambient and hence provide good stability against exposure to air over large periods[6].

3.6 PROBABLE ERROR IN MEASUREMENTS AND STANDARD DEVIATION:

In any kind of measurements carried out with the aim to arrive at values of characterizing parameters associated with the device behaviour, the results are usually obtained after a specific analysis of the acquired data. The values finally obtained are always associated with an error margin that marks the precision and accuracy of the results. It is very essential to know about this so that the obtained results and interpretations derived from it are based on sound footings. An effort to estimate such errors consists in estimating significant places of results and standard deviations expected in them. Thus an estimation of maximum possible deviations and the significant place of the arrived results up to which they can be confidently reported have been made in present context.

There are various methods of measuring the Schottky barrier characterising parameters like barrier height, ideality factor, series resistance etc. But primarily one would like to know very precisely the value of the barrier height of a chosen metal-semiconductor system. There are various methods for measuring barrier heights of Schottky barriers. These methods involve;

(i) Current-voltage measurement [7]
(ii) Capacitance-voltage measurement [7]
(iii) Conductance-voltage measurement [8]
Amongst these the current-voltage, the capacitance-voltage, the activation energy method and the Norde plots have been employed to estimate barrier height values of Ga-Si (p) and In-Si (p) Schottky barriers. Basic measurands for this analysis are applied bias voltages, resulting currents and the capacitances of the barrier. Thus, all methods used here correspond to two sets of basic measurements. The following section describes the estimation of the significant figure and the standard deviation of the results.

3.6.1 Significant Figures and Standard Deviation of the Results:

3.6.1.1 Current-Voltage measurement method:

This method is one of the prime and easiest method for determining the barrier height. The measurements involved in this method are that of current and voltage and this also provides firsthand information about rectification ratio and the ideality factor of the barrier at the interface.

Considering the thermionic emission process as the dominant one for the charge transport across the barrier, the determination of barrier height can be done using the following relationship -

$$I = I_o \exp \left( \frac{qV}{kT} \right) \left[ 1 - \exp \left( \frac{-qV}{kT} \right) \right]$$

(3.1)

where, $$I_o = A A^* T^2 \exp \left( \frac{-q\Phi_b}{kT} \right)$$

(3.2)

Here $$I_o$$ is the saturation current determined by ln I vs V plot and hence uncertainties in the measured values of current and voltage will propagate for the
uncertainty in the value of $I_0$. Thus, along with the uncertainty in the measured value of the diode's cross-sectional area $A$, the uncertainty in the $I_0$ will also propagate to give a net uncertainty in the determined value of the Schottky barrier height. Furthermore, the least count limitations of the measured parameters also determine the significant figure of the computed value of the Schottky barrier height.

Eqn. 3.1 can be rearranged for saturation current and approximated as

$$I_0 = I \exp\left(\frac{-qV}{kT}\right)$$

(3.3)

Whose differentiated logarithm is

$$\frac{\Delta I_0}{I_0} = \frac{\Delta I}{I} - \frac{q}{kT} \Delta V$$

(3.4)

Since errors propagate to add up $\Delta I_0$ can be written as

$$\Delta I_0 = I_0 \left[ \frac{\Delta I}{I} + \frac{q}{kT} \Delta V \right]$$

(3.5)

Here $\Delta I_0$ represents maximum least count error in $I_0$ and $\Delta I$, $\Delta V$ represent the least counts of $I$-$V$ measurements respectively.

Now, barrier height is determined using the expression

$$I_0 = A A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)$$

(3.6)

Following the similar procedure as given above,

$$\frac{\Delta I_0}{I_0} = \left(\frac{\Delta A}{A}\right) - \frac{q}{kT} \Delta \phi_b$$
Therefore,

\[ \Delta \phi_b = \frac{kT}{q} \left[ \frac{\Delta I_o}{I_o} + \frac{\Delta A}{A} \right] \]  

(3.7)

In present investigations data acquisition for current and voltage were made using Keithley electrometer (Model 614) and a programmable voltage source / Systronics micro voltmeter (Model 412). The least counts for current I and voltage V are \( \Delta I = 1\, \text{nA} \) and \( \Delta V = 1\, \text{mV} \) in the ranges of these instruments used for measurements. Also the diode area were measured by a comparator possessing least count \( \Delta A = 0.0001\, \text{cm} \). Substituting these quantities with typical value of and \( A = 0.094\, \text{cm}^2 \), \( I_o = 1.41 \times 10^{-7}\, \text{A} \) in Eqn. 3.7, we obtain

\[ \Delta \phi_b = 0.0002\, \text{eV} \]

**Standard Deviation:**

The approximated I-V characteristic as given in Eqn 3.3 has a form which can be expressed [10] as

\[ X = u \exp(-bV) \]  

(3.8)

Here \( u \) and \( V \) are variables and \( b \) is constant, with this form of relationship the standard deviation \( \sigma_X \) for \( X \) can be expressed [12] as

\[ \sigma_X^2 = \sigma_u^2 \left( \frac{\partial x}{\partial u} \right)^2 + \sigma_v^2 \left( \frac{\partial x}{\partial v} \right)^2 \]  

(3.9)

Hence standard deviation \( \sigma_{I_o} \) for \( I_o \) can be written as,

\[ \sigma_{I_o}^2 = I_o^2 \left[ \left( \frac{2}{I_0^2} \right) + \left( \frac{q^2}{k^2 I_0^2} \right) \sigma_v^2 V \right] \]  

(3.10)
The relationship between the uncertainty $\Delta x$ (that is the probable error) and the standard deviation $\sigma$ is then found by evaluating the point at which the integral probability curve has a probability of one-half [11]. This is given as

$$\sigma_1 = 1.4826 \Delta I \text{ and } \sigma_\nu = 1.4826 \Delta V$$

Therefore,

$$\sigma_{I_b}^2 = (1.4826)^2 I_0^2 \left[ \frac{\Delta^2 I}{I^2} + \frac{q^2}{k^2T^2} \Delta^2 V \right]$$

(3.11)

Now, the barrier height can be expressed in terms of saturation current as

$$\phi_b = \frac{kT}{q} \ln \left( \frac{AA^*T^2}{I_0} \right)$$

(3.12)

which is of the form

$$x = a \ln (\pm bu)$$

(3.13)

The standard deviation $\sigma_x$ for $x$ here is

$$\sigma_x = a \frac{\sigma_u}{u}$$

(3.14)

Hence, the standard deviation $\sigma_{\phi_b}$ in $\phi_b$ is

$$\sigma_{\phi_b} = \left[ \left( \frac{kT}{q} \right) \frac{\sigma_{I_b}}{I_0} \right]$$

(3.15)

Substituting the value of $\sigma_{I_b}$ as obtained from Eqn.3.11 standard deviation $\sigma_{\phi_b}$ comes out to be 0.0015.
It is seen from this analysis that both least count error and standard deviation are in the third decimal place and hence the values of barrier heights reported here as measured by I-V data are obtained after rounding of the calculated values upto second decimal place.

3.6.1.2 Capacitance – Voltage measurement method:

Capacitance – Voltage data of a reverse biased barrier can be used to deduce the barrier height value using the relation

\[ \phi_b = V_{bi} + \xi \]  

(3.16)

where \( V_{bi} \) is the built in potential and \( \xi \) is the difference of energy between Fermi level and the top of the valence band / bottom of the conduction band. \( V_{bi} \) can be given as-

\[ V_{bi} = \left( \frac{q\varepsilon_s N_D A_{eff}^2}{2C^2} \right) - V_R \]  

(3.17)

Here \( V_R \) is the intercept on voltage axis of \( C^2 \) vs \( V \) straight line plot. \( N_D \) is the doping concentration, \( A_{eff} \) is the effective area of the diode and \( \varepsilon_s \) is the permittivity of the semiconductor.

Hence, the least count of measured values of diode area, capacitance and reverse voltage will determine the least count in measured barrier height. The diode area, as mentioned above, were measured by a comparator with least count of \( 10^{-4} \) cm and capacitance and applied reverse bias voltage were measured using a computer controlled multifrequency LCR meter (Hewlett-Packard Model 4274 A) with least counts of 0.01 pF and \( 10^{-3} \) V. Thus the significant decimal place, up to which the barrier height can be reported, is determined by the least count of the reverse bias voltage measurements.
The built in potential Eqn.3.17 can be written as;

\[ V_{\text{bi}} = \left( \frac{1}{k^2} \right) C^{-2} - V_R \]  

(3.18)

where \( \frac{1}{k} = \frac{q_e s N_D A_{\text{eff}}^2}{2} \). Eqn.3.18 has the form

\[ x = (au^2 \pm bv) \]  

(3.19)

where \( u \) and \( v \) are variables and \( a \) and \( b \) are constants

For this type of relationship standard deviation \( \sigma_x \) for \( x \) can be written as

\[ \sigma_x^2 = \sigma_u^2 \left( \frac{\partial x}{\partial u} \right)^2 + \sigma_v^2 \left( \frac{\partial x}{\partial v} \right)^2 \]  

(3.20)

Hence the standard deviation \( \sigma_{V_{\text{bi}}} \) for built in potential \( V_{\text{bi}} \) is given as

\[ \sigma_{V_{\text{bi}}}^2 = \left( \frac{4\sigma_c^2}{k^2c^6} \right) + \sigma_v^2 V_R \]  

(3.21)

Again using \( \sigma_c = 1.4826 \Delta C \) and \( \sigma_{V_{\text{bi}}} = 1.4826 \Delta V_R \)

\[ \sigma_{V_{\text{bi}}}^2 = (1.4826)^2 \left[ \left( \frac{4\Delta^2 c}{k^2c^6} \right) + \Delta^2 V_R \right] \]  

(3.22)

Thus, using equation (3.16) the standard deviation \( \sigma_{\phi_b} \) in \( \phi_b \) is completely determined by that for \( V_{\text{bi}} \).

Therefore,

\[ \sigma_{\phi_b} = \sigma_{V_{\text{bi}}} \]  

(3.23)

Substituting numerical values as mentioned above the standard deviation in built-in potential \( \sigma_{V_{\text{bi}}} \) is obtained as 0.004 and therefore the standard deviation in the
barrier height may be expected to be of similar magnitude. Hence in the present investigations barrier heights estimated by C-V method have been reported after rounding off the values up to the second decimal place.
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