Chapter-II

CHOICE OF THE TOPIC

2.1 CHARACTERISING PARAMETERS OF SCHOTTKY INTERFACES:

2.1.1 Barrier Height:

Most important characterising parameter of Schottky interfaces is the Schottky barrier height. The effective barrier height $\phi_{be} (V,T)$ at such interfaces is defined as "The effective potential that carriers have to overcome so that they can be transported across the interface." The voltage and the temperature at which the value of these barrier heights are specified should be indicated because the practical Schottky interfaces show sensitivity to variation in the bias voltage and temperature due to various reasons. More often the experimentally determined barrier heights are labeled as zero bias barrier height $\phi_{be} (0,T)$ or $\phi_{bo} (T)$, since they are the values at zero bias voltage. In comparison to the above, the more fundamental barrier height of such interfaces is the flat band barrier height $\phi_{bf} (T)$. This represents the barrier height under zero field conditions i.e. when enough forward bias has been applied across the interface in order to eliminate the band bending.

2.1.2 Ideality factor:

Even in ideal interfaces, different charge transport mechanisms [1] e.g. thermionic emission (TE), tunneling (T) etc. or their combination like thermionic field emission (TFE) may be present depending on the nature of barrier potential i.e. its width, height etc. Further, depending on the conditions of material within the interface region, generation–recombination of carriers etc. can also make additional contribution to the charge transport across the interface. Therefore, Schottky interfaces tend to exhibit deviations from the ideal thermionic
emission transport across them. With only thermionic emission charge transport across Schottky interfaces, the current $I$ across them under applied bias $V$ is given as

$$I = I_s \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]$$

(2.1)

where $I_s$ is the saturation current given as

$$I_s = A A^* T^2 \left[ \exp \left( -\frac{q\phi_{bo}}{kT} \right) \right]$$

(2.2)

Here $A$ is area of interface, $A^*$ is Richardson constant, $T$ is temperature in K.

In presence of the multiplicity of charge transport mechanisms, the actual current $I$ across the Schottky interface is given as

$$I = I_s \exp \left( \frac{qV}{nkT} \right) \left[ 1 - \exp \left( -\frac{qV}{kT} \right) \right]$$

(2.3)

Here $n$ is the ideality factor [2] and is contemplated to be a parameter that gives the deviation of actual charge transport from the thermionic emission charge transport. Obviously the ideality factor for pure thermionic emission transport is unity. However in real Schottky interface the deviations may arise additionally on account of other reasons also e.g. differences in the bias voltage applied and the one that is actually occurring across the interface etc. Therefore, in general, deviations from thermionic emission situation, arising on account of various reasons, are all depicted by the ideality factor since they all tend to effect the net charge transported across the interface.
2.2 CHOICE OF SYSTEMS:

In the background of what has been discussed briefly in chapter-1, it is quite evident that-

(i) both the bulk and the interface play a role in the development of the characteristic behaviour exhibited by Schottky interfaces.

(ii) since the application of a Schottky interface based device is determined by its voltage – current behaviour across its terminals, efforts are continually being made to enhance the physical understanding about separating the influencing roles of both the bulk and the interface as well as to devise the ways and means to control the terminal behaviour.

The terminal current-voltage behaviour of Schottky devices is mainly determined by the barrier height and this was mostly found to be dictated by the Fermi level pinning. However, the controversy regarding what determines the pinning levels in different Schottky interfaces e.g. the bulk in the form of MIGS or the intrinsic and extrinsic defects at the interfacial layers or both remained unresolved and hence they required and encouraged, the need for more closer examination of the evolutionary aspects of such barriers.

Both theoretical and experimental efforts have been continuously undertaken in this direction. Notable theoretical efforts were made in the form of ‘ab initio ’ calculations, [3,4] taking into consideration the interface electronic structure and this provided a strong evidence against any universal kind of defect pinning of the Fermi level at the interface. Since such calculations were not easily extendable beyond some idealised systems e.g. epitaxial M-S interfaces, this approach thus seems to be limited in scope looking into the variety of possible practical Schottky interfaces. Experimental efforts on Fermi level pinning issues were made by many workers [5,6,7,8] and gave conflicting results. These studies did utilize various techniques like photoreflectance, photoluminescence and photoemission etc. and attempted to investigate the barrier evolution from initial
stages of the interface formation [9]. These kinds of experimental results gave impetus to intense investigations for understanding the evolution and possible controlling techniques of the barrier (reviewed in chapter-I ) at Schottky interfaces. A new dimension, which was added during these investigations, was the issue of lateral barrier height variations on a local scale i.e. barrier height fluctuations as all earlier models implicitly assumed the seemingly faulty assumption that each interface barrier is a constant characteristic of the entire interface. Noteworthy advances in the technology have supplemented and supported the investigations in this direction e.g. photoelectron spectromicroscopy [10,11,12] free electron laser techniques [13,14,15] and ballistic electron emission microscopy (BEEM ) etc. [16,17].

These investigations have shown that spatial variations in barrier heights is a distinct feature associated with Schottky interfaces and it is the least barrier height filament among the range of distribution, which will determine the overall behaviour. Further, the average barrier height determining the overall device behaviour can be expected to show variations with decreasing spatial dimensions when an array of such devices are made. Moreover, thickness variations can also accompany this feature.

The above discussions, reviewing briefly the investigations on the evolution of barriers at Schottky interfaces show that

(1) both chosen bulk semiconductor and the overlayer metals have a bearing on it.

(2) the condition existing at the interface between the two i.e. interfacial layer conditions e.g. its chemical and electronic situations, crystallographic nature, strain and morphology etc. also affect the resulting barrier.

(3) conditions of initial few layers are relatively more important in comparison to further layers of the metal.
(4) globally seen barrier is an average one of the spatial and lateral
fluctuations, which may gain prominence under certain situations e.g. with
reduction in the interface dimensions etc. However even global value
seems to be determined by the element of the interface, which has the
least barrier height value.

Thus, Schottky interfaces and devices based on them still constitute
an open problem both from fundamental physics and applications / technological
points of view. As has happened in the field of semiconductor interface research
and other fields, there is still need and scope to devise means and ways, which
can still focus on the evolutionary aspects of the barriers at such interfaces.

In this context Schottky barriers fabricated utilising metallic
overlayers in the liquid form may be revealing. This is expected because, in case
of such metallic overlayers

(1) no costly technology e.g. high vacuum and associated equipments etc. are
required for fabrication, since interfaces can be simply made on the
semiconductor substrates by putting these liquid metals and confining them
in area on the cleaved / chemically prepared semiconductor surfaces.

(2) The time gap elapsing between the time when such substrates were
prepared and the time when the metallic overlayers are made (e.g. by
evaporation, sputtering etc.) can be drastically reduced allowing little time
for ambient driven chemical and electronic changes which might take place
on the surface of the semiconductor.

(3) The possibility of changes in the morphology and electronic structure driven
by impingement of high velocity atoms / molecules / species of evaporated /
sputtered metallic elements / systems on the semiconductor surface will be
automatically eliminated. Moreover, the above kind of changes driven by
the heat of condensation during equilibration of such metallic evaporant
species will also be eliminated. In light of above, the Fermi level pinning issues may be investigated a fresh.

(4) When an overlayer of liquid metal is made on the semiconducting substrate, the bonding between metallic overlayers and the substrate is loose in contrast to the relatively stronger bonding between an evaporated / sputtered and condensed metallic overlayer. This can be compared to the requirement of ideal Schottky interfaces with no chemical interaction between the two sides of the interfaces e.g. metallic overlayers on layer type semiconductors which have a strong intra layer but weak inter layer [18] bondings perpendicular to layers.

Thus, Schottky interfaces with liquid metal overlayers provide an exciting opportunity to develop various kinds of experiments to investigate the evolutionary aspects of fundamental nature on such interfaces. One of these can consist of utilising such interfaces to look for influencing factors which might have been getting overshadowed by the usual methods of preparing metallic overlayers. It is in this context that investigation of gallium - silicon Schottky interface has been selected and is discussed in chapter - IV.

Mostly, the evolutionary aspects of Schottky interfaces have been probed by evaluating the value of the characterising parameter namely barrier height of such interfaces resulting from band realignment and equilibration of the Fermi levels on account of charge transfer across it. Barrier heights of such interfaces are usually measured by current-voltage ( I – V ), capacitance-voltage ( C – V ) or photoelectric current methods. Although, photoelectric method and its extensions where the current / energy spectra resulting from photoexcitation is analysed to estimate the barrier height, the C-V and I-V methods are more near in comparison to the real time terminal behaviour of devices based on such interfaces. Therefore, all the above three methods assume importance since some evolutionary aspects may be more amenable to one or other specific methods. For example, the aspects of barrier height variation related to initial stages of growth of metallic overlayers can be more successfully probed by
photoelectron spectroscopy. On the other hand, evolutionary aspects and barrier height variations related to and affecting the real time terminal behaviour of device based on such interfaces can be more successfully probed by current-voltage and capacitance-voltage methods.

The evolutionary aspects, more important from technical / applications points of view, are the one which get reflected into the terminal behaviour of real devices based on Schottky interfaces. Therefore, in this context current-voltage and capacitance-voltage methods become significant. But one has to consider the complete equivalent circuit represented by the device under probe [Fig. 2.1(a)] while using these methods. As it is seen from here the presence of the two resistances, one the series resistance $R_s$ in series with the barrier (arising on account of material out side it and the contact resistances at the two terminals) and the other, the shunt resistance $R_{sh}$ in parallel to the barrier (arising from characteristics of the material within the barrier including insulating interfacial layer, if any) cannot be overlooked. It has been found that in addition to deviations caused by presence of multiplicity of charge transport mechanisms, sizeable deviations in the terminal characteristics (both Current-Voltage and Capacitance-Voltage characteristics) can be caused by presence of these resistances. Figure 2.1(b) shows parts of current-voltage characteristics affected by these resistances and figure 2.3(c) shows the effect on capacitance-voltage characteristics. These kinds of anomalies have formed the subject matter of discussions in several papers by various investigators[19]. Further, the current–voltage and the capacitance-voltage characteristics are also affected by the presence of insulating layer at the interfaces and interface states, inhomogeneities in barrier heights commonly present at the peripheries of interfaces etc. In light of these facts, it becomes imperative to correctly evaluate the characterising parameters e.g. barrier height etc. in order to obtain a more realistic picture about some unseen dormant evolutionary aspects and other physical feature of the Schottky interface behaviour through I-V and C-V investigations.
Fig. 2.1 (a) Equivalent circuit of a practical Schottky diode with Series ($R_s$) and Shunt ($R_{sh}$) resistances.
(b) Its current – voltage characteristics and (c) Capacitance – voltage characteristics.
It is in this context that indium–silicon system has been chosen. p-type silicon is chosen, as there are comparatively smaller amount of reports on p type substrates than on n type substrates. Further, for this system, the Mott-Schottky work function model predicts a barrier height of around the band gap of silicon and this value is expected to go down to one third of band gap in case of Bardeen model with charge neutrality level assumed to be around one third band gap of the silicon. Thus, with contributions from one or more kind of variations in the interfacial conditions the actual value will have a large span (between the band gap and the charge neutrality level) in which the real value of the barrier height can be expected. Moreover higher sensitivity to variations in the interfacial condition resulting from substrate preparation condition etc. can also be expected.
References:


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