Chapter VI

CONCLUSIONS AND FUTURE SCOPE

In accordance with the objectives laid down for the present thesis and discussed in chapter II, the two Schottky systems namely gallium p-silicon and indium p-silicon were fabricated and investigated. The details of the investigations carried out and the results of investigations on these systems have been given in Chapter IV and V respectively. The discussions of the results obtained on gallium p-silicon Schottky system as discussed in Chapter IV clearly bring out the following –

(1) There is an anomaly in the charge transport behaviour of this system across the melting point of gallium. This is clearly reflected in the percentage change in the forward and reverse currents with temperature across the melting point of gallium, which is shown in Fig. 6.1. It has been shown that this anomaly is manifested in the form of
   (a) sudden increase in shunt conductance within a very narrow temperature range centered around the melting point of gallium.
   (b) significant increase in the series resistance across the melting point of gallium such that series resistance in liquid phase of gallium is much more than in its solid phase.
   (c) the zero bias barrier height in the liquid phase is higher than zero bias barrier height in the solid phase.
   (d) the device capacitance also increases across the melting point of gallium. However, it is more easily notable in the rate of increase of capacitance near melting point as seen from Fig. 4.23 where large increase occurs in a narrow range of temperature centered across the melting point.
Fig. 6.1 Relative change in current vs temperature of Ga-Si(p) Schottky diode (Sample-B).
All these are evidences of the fact that the electric field at the junction of investigated device undergoes a significant change near the melting point of gallium. This may be related to the phase transition driven physical processes e.g. breaking of bonds both between gallium atoms and between gallium atoms and silicon interface; change from long range to short range order in gallium, strain relaxations at the interface etc. In nutshell it can be said that the phase transition suddenly increases the lateral inhomogeneities of the interface so that the electric field distributions across the interface changes. However, the change is such that mean electric field at the interface is not significantly disturbed and hence the capacitance barrier does not undergo as large change as the zero bias barrier height. However, strain build up or relaxation appears to be the dominant reason for the observed anomalous behaviour.

The observed results are quite significant in the sense that they provide an experimental proof of the expectations that strain of Schottky interfaces etc. should make a contribution to the barrier heights. Thus, it will be interesting to investigate in more detail the phase transition driven anomaly in the behaviour of Schottky diodes e.g. are they confined to phase transitions of the first order only or they accompany the phase transition of second order also ?; are the changes completely reversible or they are accompanied by any hysteresis effect ?; etc.

Another significant observation is that the rectification characteristics are generally better in the liquid phase of gallium than in its solid phase. This fact is reflected in the rectification ratio given in Table 6.1. From here it can be seen that while the rectification ratio in liquid phase is generally high, it varies in solid phase depending on the quality of interface. This throws up a possibility that if proper designs are developed, liquid metal Schottky diodes capsules can be put to applications. Hence, further investigations may be interesting in this direction also. The liquid metal Schottky devices have a good potential for investigating barrier height engineering through alloying technique since obtaining an alloy of liquid metal is comparatively easier than obtaining a solid metal alloy.
Table 6.1 Rectification ratio at different biases

<table>
<thead>
<tr>
<th>Phase</th>
<th>Bias (volt)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.3</td>
</tr>
<tr>
<td>Solid (295 K)</td>
<td>5(A) 32(B)</td>
</tr>
<tr>
<td>Liquid (305 K)</td>
<td>251(A) 17(B)</td>
</tr>
</tbody>
</table>

The results and discussions of investigations on indium p-silicon Schottky system indicates that the as fabricated diode of such a system on chemically prepared silicon surface possesses an interfacial insulating layer with high density of interface states. An indication to this can be obtained from the analysis of series and shunt resistance corrected forward bias characteristics used for obtaining the ideality factor. Its value in excess of around 1.5 definitely indicates the presence of interfacial layer and under this condition, the genuine value of zero bias barrier height can not be obtained from the plot of the function $\ln \left[ \frac{l}{1-\exp(-qV/kT)} \right]$ vs $V$. In case of the presence of interfacial layer an idea about the lateral inhomogeneity of the interface can be obtained by finding out the density of interface states, presence of $T_0$ effect, non-linearity of activation energy and Richardson plots. The above kind of analysis also gives indications about the dominant nature of the operative charge transport mechanisms in case the investigations have been made over a wide temperature range. Such investigations on indium p-silicon diode in present case has revealed that the diode possesses a strong $T_0$ effect with inhomogeneous interface described by barrier height fluctuations having a standard deviation of around 1.1. All this reflects on the technology adopted for fabricating the present diode for investigations and indicates that it needs improvement for enhancing the quality of the fabricated diode. However, even under these limitations, the flat band barrier
heights give a genuine value for the barrier height. This kind of analysis has revealed that the fabricated and investigated indium p-silicon diode possesses a flat band barrier height of around one electron volt. This is also close to the value obtained as average barrier height on inhomogeneities model and by the modified Richardson plot given in Fig. 5.24 using the excess temperature $T_0$ shown by the investigated diode. The obtained value lies between the Schottky limit value of 1.2eV and the Bardeen limit value of 0.36eV limit value for the In-Si(p) diode assuming charge neutrality level of interface states to lie around one third of the silicon band gap. However, the nearness of the obtained value to the Schottky limit value indicates that the presence of insulating layer may lead to weakening of the Fermi level pinning. Thus, it can be seen that even in the case of not so good diodes, the evaluation of characterizing parameters can be obtained by systematically proceeding and analyzing the behaviour exhibited by the diode over a wide temperature range.

Since indium easily dissolves in gallium and forms alloys and the solid liquid phase transition for such alloys is a function of amount of indium dissolving in gallium, it may be interesting to investigate Schottky diodes of this system to further the objectives of the kind of investigations reported in the thesis.
LIST OF PUBLICATION / PRESENTATION

1. "A Study of The Electrical Behaviour of The Schottky Barrier Contact" National Academy of Science, India, held at S. V. N. University., Tirupati, (November 3-5,1995).


8. "Understanding Tuning of Schottky Barriers: Metal Alloy –p Silicon System" DAE Solid State Physics Symposium Organized by Board of Research in Nuclear Physics, Department of Atomic Energy, Govt. of India at Indira Gandhi center for atomic Research, Kalpakakkam (Tamilnadu) during (December20-24,1999).

9. "Temperature dependence of Barrier Heights in In-pSi Schottky Barriers" one day Seminar on condensed matter physics, Department of physics, Sardar Patel University, Vallabh vidyanagar, (March 5, 2000).
10. "Barrier Height Zn-(p)Si System" Eleventh Annual General of Material Research Society of India to be held at M. S. University, Baroda (February 3-5, 2000).

11. "Flat Band Barrier Height of In-pSi Schottky Diode" one day Seminar on condensed matter physics, Department of physics, Sardar Patel University, Vallabh vidyanagar, March 17, 2001.

12. "Barrier Height of In-pSi Schottky Diode" DAE Solid State Physics Symposium organized by Board of Research in Nuclear Physics, Department of Atomic Energy, Govt. of India at Bhabha Atomic Research Centre Trombay, Mumbai (December 26-30, 2001).