Fabrication and Characterization of Al/Al$_2$O$_3$/p-Si MOS Capacitors

MOS capacitors were fabricated on silicon substrates. ALD deposited Aluminum Oxide was used as dielectric material. Various electrical and dielectric characterization of these structures were done in detail.

6.1 Introduction

As technology demands smaller devices due to various reasons newer processes have to be developed to fabricate nanoscale devices. Metal-Oxide-semiconductor (MOS) type structures play a crucial role in many such devices especially in microelectronics and optoelectronics. In recent years there has been a growing interest in metal oxides as dielectric materials for gate oxide of MOSFETs and stable capacitors in ultra large scale integrated electronic circuits (ULSI). Maintaining the quality and reliability of gate oxides is one of the most critical and challenging tasks in any MOS devices. Study of the MOS structure is a source of a wealth of interesting and important informations from the material science point of view. It also provides an insight into semiconductor surface conditions during device operation. Numerous studies have been conducted and various models were developed for understanding the behavior of oxide-semiconductor interface and the current transport mechanisms in MOS capacitors [1,2,3]. This is essential for the design and manufacture of better-quality, long-lived and faster schottky and MOS structures like capacitors, diodes, transistors and integrated circuits. The performance and reliability of these devices are strongly dependent on the formation of insulator layer (native or deposited), interface states ($N_{ss}$) localized at the semiconductor-insulator interface and the series resistance ($R_s$). The electrical and dielectric properties of these devices strongly depend on applied voltage, frequency and temperature. Hence an understanding of the effect of frequency and bias voltage on the
electrical and dielectric properties is very much essential for designing MOS devices.

Nevertheless satisfactory understanding of all details has still not been achieved. At high-frequencies (such that the carrier life time $\eta$ is much larger than $1/\omega$ where $\omega$-angular frequency of the applied gate voltage) the charges at the interface states cannot follow an ac signal, whereas at low-frequencies they can easily follow the signal. Therefore, the dependence of electrical and dielectric properties on frequency is very crucial while considering the accuracy and reliability of such devices [4-8].

In the present work we report the effect of bias voltage, frequency and temperature on electrical and dielectric properties of Al/$\text{Al}_2\text{O}_3$/p-Si structure in which the $\text{Al}_2\text{O}_3$ dielectric layer is deposited by ALD.

### 6.2 Metal-Oxide-Semiconductor structures (MOS)

Metal-Oxide-Silicon (MOS) capacitor is the basic structure used in silicon FET to control the conductive channel by gate bias. Figure 6.1 shows the cross sectional view of a MOS capacitor, where $V_G$ is the applied gate voltage. For an ideal MOS capacitor, both the oxide and the oxide-semiconductor interface are assumed to be free of charges and defect states. Depending on the polarity and magnitude of the applied gate voltage, the carrier concentration and band structure of semiconductor changes resulting in different electrical characteristics of the MOS capacitor.

![Figure 6.1: Schematic diagram of MOS Capacitor](image)

A MOS structure with $\Phi_{\text{MS}}$, which is the work function difference between metal and semiconductor is zero and no interface and mobile
charges in the oxide is called an ideal MOS capacitor. Figure 6.2 shows the energy band diagram of an ideal MOS capacitor, with p-type semiconductor at thermal equilibrium ($V_G = 0$). $\Phi_m$-metal work function, $\chi$-electron affinity of the insulator, $\chi$-electron affinity of semiconductor, $E_g$-energy gap of semiconductor, $\Phi_B$-potential difference between the metal Fermi level and conduction band of the insulator, $\psi_B$-potential difference between the intrinsic Fermi level ($E_i$) and Fermi level ($E_F$) inside the bulk, $E_C$-conduction band edge and $E_V$-valance band edge of the semiconductor. These energy barriers prevent the free flow of carriers from the metal to the silicon or vice versa. Thus the application of a bias across the MOS capacitor does not result in current flow. Rather, an electric field is established in the oxide by surface charge layers that form in the metal and on the silicon-oxide interface [1,9,10].

For an ideal MOS system, when the applied gate voltage $V_G = 0$ the energy bands are flat and known as flat band condition. From figure 6.2, the work function difference can be written as follows [2,10]:

$$\phi_{ms} = \phi_m - \phi_a = \phi_m - \left( \chi + \frac{E_g}{2q} - \psi_B \right) = 0 \quad (6.1)$$
Where $\Psi_B$ is negative for p-type and positive for n-type substrates (equation 6.4).

When a gate voltage $V_G \neq 0$ is applied to an ideal MOS structure, the charges are distributed at the semiconductor-insulator or metal-insulator interface with equal amount and opposite polarities. It is assumed that under applied gate voltage $V_G$, there is no charge transfer throughout the insulator, which means that it has an infinite resistance. Depending on the polarity and magnitude of the gate voltage, the MOS can control the type and value of the current through MOSFET channel. There are mainly three working regions for a MOS capacitor depending upon whether applied gate voltage is positive or negative.

**Accumulation:**

We consider a MOS structure in which the semiconductor is p-type. When a negative voltage $V_G$ is applied to metal terminal of the MOS structure, it will develop an internal electric field in the oxide in the direction of semiconductor to metal. This electric field piles up holes of p-type semiconductor and accumulate near the interface. The change in the free carrier concentration at the interface bends the band diagram of the semiconductor at the interface as shown in Figure 6.3 (a).

Free electron and hole (n & p) concentrations of semiconductor at the oxide-semiconductor interface are given by:

$$p = N_v \exp \left[ -\left( \frac{E_F - E_V}{kT} \right) \right]$$

$$n = N_c \exp \left[ -\left( \frac{E_C - E_F}{kT} \right) \right]$$

Where $N_c$- effective density of states in the conduction band, $N_v$- effective density of states in the valence band $E_F$-Fermi level energy, $E_V$- valance band energy and $E_C$-conduction band energy. As the hole
concentration (p) increases at the interface, $E_F-E_V$ term must decrease. Therefore, the valance band, conduction band and intrinsic Fermi level bends up at the interface. MOS capacitor in accumulation behaves like a parallel plate capacitor and system capacitance becomes equal to that of oxide capacitance, $C_{ox}$.

![Energy band diagram of MOS capacitor in accumulation region](image)

Figure 6.3: Energy band diagram of MOS capacitor in accumulation region (a) Band bending at the interface and (b) Distribution of charges on the gate and semiconductor due to applied gate voltage $V_G < 0$.

**Depletion**

When a positive voltage $V_G$ is applied to metal terminal of MOS structure, there develops an internal electric field in the downward direction from metal to semiconductor and the holes at the interface of semiconductor are pushed towards the bulk silicon. As a result the majority carrier density is diminished at the oxide semiconductor interface. This surface region with decreased majority carrier density is called ‘depletion region’ or ‘space charge region’. Only negatively charged acceptor ions fixed to the silicon network remain in the depletion region. From Equation 6.2, the decrease of hole concentration at the interface causes an increase in $(E_F - E_V)$, which results in the bending down of bands at the semiconductor-oxide interface. Cross-section and energy band diagram of MOS capacitor under this condition are depicted in Figure 6.4.
Inversion

As we continue to increase positive gate voltage, bands continue bending down and conduction band edge $E_C$ gets closer and closer to the Fermi level $E_F$. At a certain point, intrinsic Fermi level $E_i$ reaches to the Fermi level $E_F$ where electron and hole concentration at the surface of the semiconductor becomes equal. At this voltage value of $V_G$, surface of semiconductor behaves like an intrinsic semiconductor with equal electron and hole concentrations.

As the gate voltage $V_G$ is increased further electron concentration on the surface of the semiconductor continues to increase. The value of $V_G$ at which the electron concentration at the surface become equal to the hole concentration in the bulk is called ‘Threshold voltage’ ($V_T$). At $V_T$ $E_i$ bend downward by twice the bulk potential. From the intrinsic surface condition upto this point the region is known as ‘weak inversion region’. Usually weak inversion region is considered to be the part of depletion region. The region of band bending for $V_G > V_T$ is called ‘strong inversion’ or just inversion.
Figure 6.5: (a) Energy band diagram of MOS capacitor in Inversion mode, (b) charge distribution on the metal and semiconductor due to applied gate voltage.

The three working regions of a MOS capacitor are usually described by bulk potential $\Psi_B$ and surface potential $\Psi_S$ (Equations 6.4 & 6.5). Bulk potential is the potential difference between the intrinsic Fermi level and Fermi level inside the bulk, whereas surface potential is the potential difference between the intrinsic Fermi level inside the bulk and at the interface.

$$\Psi_B = \frac{E_F - E_{ib}}{q} \tag{6.4}$$

$$\Psi_S = \frac{E_F - E_{is}}{q} \tag{6.5}$$

The internal parameter $\Psi_S$ can be controlled by the external voltage $V_G$ (Equation 6.6). By applying a varying gate voltage $V_G$, the charge concentration at the surface of the semiconductor can be changed and the surface potential of the system changes accordingly as per the polarity of the applied gate voltage.

$$V_G = V_{ox} + \Psi_S \tag{6.6}$$
Where $V_{ox}$ potential drop across the oxide

When applied gate voltage $V_G$ changes from negative values to zero and to positive values, the sign and magnitude of charge on the silicon surface will change. This change in surface potential will introduce a capacitance in series with the oxide capacitance.

### 6.3 Capacitance-Voltage (C-V) analysis of MOS capacitors

C-V analysis is considered as one of the most important tool for characterizing MOS systems [1]. In this the differential capacitance is the most essential property, because small-signal measurements determine the changing rate of the charge with voltage. To understand capacitance-voltage measurements properly one must first be familiar with its frequency dependence. The frequency dependence occurs primarily in inversion region, since a certain time is needed to generate the minority carriers in the inversion layer. High and low frequency C-V measurements are often useful among various methods to evaluate the MOS characteristics. Most of the capacitance measurements are performed with admittance bridges or capacitance meters.

By applying Gauss’ law, the small-signal equivalent circuit of the MOS capacitor was derived as follows [1,2]:

$$\frac{1}{c} = \frac{1}{c_s(p_A)} + \frac{1}{c_{ox}}$$  \hspace{1cm} (6.7)

Equation 6.7 gives the total capacitance of the MOS device as the sum of the silicon capacitance and the oxide capacitance, per unit area in series. The majority and minority carrier response times to ac gate voltages are different. The minority carrier response time is typically as long as 0.01-1s, which is much slower than the frequency of bias at high frequency and hence certainly not instantaneous over the frequency range of interest.

Figure 6.6 clearly shows the ideal C-V characteristics of a MOS capacitor with accumulation, depletion and inversion region. Normalized capacitance value is maximum at accumulation region and equal to the
oxide capacitance. For the depletion region, as the silicon capacitance increases by the formation of the depletion layer, the total capacitance decreases as they are in series with each other. Finally for the inversion region total capacitance is the series combination of oxide capacitance and inversion layer capacitance. Depending upon the frequency of the ac voltage applied it is possible to observe two different behaviors. First, if the frequency is low enough, minority carrier generation takes place efficiently and electrons form an inversion layer at the oxide-silicon interface [1]. Therefore, the total capacitance increases and reaches back to its maximum value for positive gate voltages. Second, if the applied frequency is high enough (1MHz) then the minority carriers cannot be generated fast enough and hence cannot form an inversion layer at the oxide-silicon interface. In this case, the capacitance reaches its minimum value and stays constant even if the applied gate voltage is increased to higher positive values.

![Figure 6.6: Ideal C-V curve for a MOS capacitor (a) low frequency (b) high frequency (c) deep depletion](image)

Usually C-V curve is measured by automatically sweeping gate bias. If sweep rate is too rapid for minority carriers to follow, the system no longer will be in thermal equilibrium with respect to gate bias and resulting
C-V curve will differ from thermal equilibrium curve. At room temperature, the minority carrier generation rate will be much smaller than the recombination rate. The sweep rates normally used are too rapid for generation to follow but are slow for recombination to follow. At room temperature the system usually is not in equilibrium when gate bias is swept in the direction of increasing inversion, but it is in equilibrium when gate bias is swept in the direction of decreasing inversion.

If response is too slow for minority carriers to follow the gate bias sweep into inversion, no inversion layer forms. Therefore the charge neutrality must be satisfied by increasing the width of depletion layer wider than the thermal equilibrium and under this condition the capacitance decreases below its thermal equilibrium saturation value. This non-equilibrium condition is known as deep depletion [1].

6.4 Non-ideal Effects

In actual MOS capacitors, there are several non-ideal effects that may result in deviation from ideal behavior. The work function difference between the metal and semiconductor due to variation in the doping level of semiconductor material is one such cause of non-ideal effect. To compensate this work function difference an external voltage should be applied to the MOS structure. For this bias condition, the energy bands of Si are flat up to the interface and do not vary with distance. This applied voltage to achieve flat band condition is called the flat band voltage and is represented by \( V_{FB} \) for the MOS capacitor. If the oxide material does not contain any oxide or interface trap charge. The \( V_{FB} \) can be written as.

\[
V_{FB} = \Phi_m - \Phi_s - \left( \chi + \frac{E_g}{e} - \Phi_p \right)
\]  

(6.8)

where \( \Phi_m \)-metal gate work function, \( \Phi_s \)-semiconductor work function, \( \chi \)-semiconductor electron affinity, \( E_g \)-semiconductor energy gap, and \( \Phi_p \)-position of semiconductor Fermi level above the valance band in the neutral semiconductor bulk. The difference in work functions represents the amount of band bending. The sign of the difference of the metal and
semiconductor work functions gives the polarity of applied voltage to be connected to the metal to obtain the flat band condition.

Other non-ideal effects are mainly due to charges present in the oxide and at the semiconductor-oxide interface. It has been established that there are mainly four general types of charges associated with the oxide/Si system as summarized in Figure 6.7. The total charge per unit area is represented by $Q$ (C/cm$^2$) and the number of charges per unit area (the number density) is represented by the symbol $N$ (number/cm$^2$).

![Figure 6.7: Various charges present in MOS structures.](image-url)

The first type of charge is named as the fixed oxide charge $Q_f$ which is primarily due to the structural defects (such as ionized silicon) in the oxide layer. The density of this type of charge is closely related to the oxidation process. Figure 6.8 shows a comparison of the energy band diagrams for ideal n and p type MOS structure. For these ideal structures, at zero applied voltage on the metal gate, it is a state of flat band. However, because of the difference between the gate metal work function ($\Phi_m$), and the semiconductor work function ($\Phi_s$) many dielectrics exhibit a charge at the silicon surface resulting in a required applied voltage $V_{FB} \neq 0$ to achieve a flat band condition.
Figure 6.8: Energy-band diagrams and associated high frequency C-V curves for ideal MIS diodes for (a) n-type and (b) p-type semiconductor substrates. For these ideal diodes, $V_G = 0$ corresponds to a flat band condition. For dielectrics with positive ($Q_f$) or negative ($-Q_f$) fixed charge, an applied voltage ($V_{FB}$) is required to obtain a flat band condition and the corresponding C-V curve shifts in proportion to the charge in dielectrics.

The simplest and most widely used method for measuring oxide charge density $N_{eff}$ is to infer this density from the voltage shift of C-V curves, caused by the existence of oxide charges, as shown in the right part of Figure 6.8. In both cases (p substrate and n substrate) positive $Q_f$ causes the C-V curve to shift to more negative values of gate bias with respect to the ideal C-V curve. If the oxide charge is negative then the entire C-V curve
is shifted to more positive value with respect to the ideal C-V curve, and
negative oxide charge cause the C-V curve to shift to more positive value
with respect to the ideal C-V curve. The bias shift of the C-V curve caused
by oxide charge Q can be explained by image charges.

Using a n-type substrate as an example, for a certain gate bias
without any charge, at depletion region, the ideal depletion layer width is
such that negative charge on the gate is balanced by the positive dopant ions
in the depletion layer. If positive charge is joined in the oxide as shown in
the upper-right side of Figure 6.7, the above charge balance is interrupted,
its image charge (actually electrons for this case) is introduced in the silicon
substrate. These additional electrons located at the depletion layer, partly
neutralize and reduce the depletion layer width. Because the capacitance of
Si ($C_s$) is inverse to the width of the depletion layer and in series connection
to $C_{ox}$, the actual capacitance with oxide charge Q becomes larger than for
the ideal capacitance without Q (Figure 6.8 right top Figure). At strong
accumulation, this influence of image charge is omitted because of the
accumulation of carriers at the surface of Si from the substrate and absence
of depletion region. At strong inversion, for low frequency measurements
capacitance value reaches the same saturation value as in the case of
accumulation and hence the effect of image charge is absent.

The second type of charges is the oxide trapped charge, $Q_{ot}$. These
are due to holes or electrons trapped in the bulk of the oxide layer and can
come from the ionizing radiation or avalanche injection. Thus, $Q_{ot}$ can have a
positive or a negative value. Third type of charge is called mobile ionic
charge, $Q_m$, which is mainly due to ionic impurities such as Li$^+$, Na$^+$, and K$^+$
etc.

The sum of these three different charges in the oxide layer is
represented by the effective oxide charge $Q_{eff}$ (and its number density $N_{eff}$)
as given in Equation 6.9.

$$Q_{eff} = Q_f + Q_m + Q_{ot}$$  \hspace{1cm} \text{(6.9)}
Finally, the fourth and the most important source of non-ideal effects is due to interface trapped charge $Q_{it}$. Its density per unit area per unit energy is denoted by $D_{it}$. They are usually located at the oxide-semiconductor interface. It has a positive or a negative value depending on the location with respect to the Fermi level. They originate from structural disorder, oxidation-induced defects, metal impurities and defects caused by radiation or similar bond-breaking processes. Various techniques like Terman’s method and simultaneous C-V methods are used to calculate the level of interface trap density. $D_{it}$ plays a major role in the operation of MOS devices causing an increased recombination of the free carriers in the conduction and valance bands. The levels of the $Q_{eff}$ and $D_{it}$ are the important parameters to be controlled during the manufacturing process of the MOS devices.

### 6.5 Conduction mechanism of insulator

The performance of MOS devices strongly depends on the breakdown properties and the current transport behavior of the gate dielectric films. Therefore the conduction mechanism of the gate dielectric film has attracted many scientists in the field of physics and material science. The conduction mechanisms of the gate dielectric films are found to be very sensitive to the film composition, film processing, film thickness, trap energy level and trap density in the films. However, the conduction behavior of a gate dielectric is generally dominated by one or two mechanisms.

The current conduction mechanisms through the insulating materials, which do not contain free carriers, can be distinctly different from those in doped semiconductors or metals. T. Hori and E. H Nicollian et al. described the conduction mechanism in details in their books [1,9] especially focusing on the conduction mechanism valid in SiO$_2$. Most introductions on conduction in insulators in this chapter is based on SiO$_2$, since thermal SiO$_2$ film could be considered basically an ideal insulator under moderate bias conditions. Although the oxide resistivity is very high, of the order of $10^{15}$ ohm-cm, it is not infinite. Hence current flows through an oxide at any given gate voltage. Most amorphous insulators at an electric field (E) in excess of $10^4$V/cm show a range of nonlinear current-voltage dependence,
and can be interpreted based on certain conduction mechanisms. In the following part we discuss Fowler-Nordheim (FN) tunneling, Poole-Frenkel (PF) emission, as well as direct tunneling transport, Schottky emission and ohmic behaviour. FN and direct tunneling are substantially independent of the temperature unlike other mechanisms, because of the dependence of tunneling phenomena only on the quantum state of the insulator.

![Figure 6.9: Schematic of Fowler-Nordheim tunneling](image)

Where $\Phi_B$ - barrier height, $E_{FM}$ - metal Fermi level, $E_{FS}$ - semiconductor Fermi level, $d_{ox}$ - oxide thickness, $d_{FN}$ - tunneling distance, $V_G$ - gate voltage

FN tunneling has been studied extensively in MOS structures where it has been shown to be the dominant current mechanism, especially for thick oxides (>40Å), such as in Figure 6.9. The basic idea is that quantum tunneling of carriers occurs through a triangular potential barrier in the presence of a high electric field. The barrier of the insulator is pulled down by the E-field so far that electron tunneling from the metal Fermi level into the oxide conduction band becomes possible. Once the carriers have tunneled into the insulator they are free to move within the valence or conduction band of the insulator. To check for this current mechanism, experimental I-V characteristics are typically plotted as $\ln(J_{FN}/E_{ox}^2)$ vs. $1/E_{ox}$, which is called Fowler-Nordheim plot. Provided the effective mass of the insulator is known (for $Al_2O_3$, $m_{ox}^*=0.42m_0$), one can fit the experimental
data to a straight line yielding a value for the barrier height under the valid \( E \) field.

FN tunneling implies that carriers are injected into the conduction band of the insulator and are free to move through the insulator. However, in deposited insulators, which contain a high density of structural defects, this is not the case. These structural defects cause additional energy states close to the band edges and restrict the current flow by capture and emission processes, thereby becoming the dominant PF emission mechanism. The existence of a large density of shallow traps in deposited films makes PF emission a well characterized mechanism. Field-enhanced thermal excitations of trapped electrons into the conduction band are frequently observed in such films. Other possible processes including ohmic conduction as well as trap assisted tunneling, can be found in the literature [9]. In the simple case for \( d_{ox} < 2 \) nm, direct tunneling dominates when the electrons pass through the full oxide thickness then the gate current is due to direct tunneling. Fowler-Nordheim tunneling and Pool-Frenkel emission with the corresponding \( J-E \) functions are described as follows:

\[
J = \frac{A}{4\Phi_B} E^2 \exp\left(-\frac{2}{E} \Phi_B^{3/2}\right) \quad (6.10)
\]

\[
J \propto E \exp\left(-\frac{\Phi_B - \sqrt{E/C}}{\Phi_t}\right) \quad (6.11)
\]

where \( J, E, \) and \( \Phi_t \) are current density, electric field, and thermal energy of about 26 meV at room temperature. \( \Phi_B \) is the potential barrier height, \( A, \) and \( C \) are constants. For a substrate in strong accumulation, where \( E_B > \frac{4\Phi_B^2}{3qB_{ox}} \), the direct tunneling leads to a similar formula as Fowler-Nordheim tunneling and can be simplified to following with additional constant terms \( B_1 \) and \( B_2 \):

\[
J_{dir} = \frac{q^2m_{eff}E^2}{8\pi\Phi_BmB_1} \exp\left[-\frac{4\sqrt{2m(q\Phi_B)^2B_2}}{\hbar qE}\right] \quad (6.12)
\]
6.6 Fabrication of MOS capacitor

MOS capacitors were fabricated on p-Silicon (100) substrate with ALD-$\text{Al}_2\text{O}_3$ as gate dielectric and Aluminum as metal electrode. Since any chemical contamination may ruin the entire device performance and reliability, wafer cleaning is an important and critical step in device fabrication. Prior to depositions substrates were cleaned by standard cleaning procedure which consists of the following steps.

- **Standard cleaning 1 (SC-1)** is performed with a 1:1:5 solution of $\text{NH}_4\text{OH}$ (ammonium hydroxide) + $\text{H}_2\text{O}_2$ (hydrogen peroxide) + DI water ($\text{H}_2\text{O}$) at a temperature of 75 °C for 10 minutes. SC-1 removes any organic contaminates by oxidation. This is followed by transferring the wafers into a DI water bath.

- **Dilute HF dip**: HF- DI water in composition of 1:10 is prepared and the wafers are dipped in it for 60 seconds after SC-1 process to remove the native oxide present on the wafer substrate.

- **Standard clean 2 (SC-2)** is performed with a 1:1:6 solutions of $\text{HCl}$ + $\text{H}_2\text{O}_2$ + $\text{H}_2\text{O}$ at a temperature of 75°C for 10 minutes. This treatment effectively removes the remaining metallic (ionic) contaminants on the wafer. The cleaning process is followed by dilute HF dip to passivate the Si dangling bond with hydrogen.

The native oxide formed on the back surface was etched by buffered HF (HF-DI water in a composition of 1:10). After the oxides etch the samples were cleaned with acetone and Isopropyl Alcohol (IPA).

Aluminum Back contact of MOS capacitor were deposited on back etched wafer by thermal evaporation with a thickness of 100nm. Top aluminum metal electrodes were also patterned by thermal evaporation through shadow mask. Thicknesses and area of the electrodes were measured using a surface profiler (Dektek) and optical microscope. About 50 devices were fabricated on a 1cm×1cm silicon substrate with circular gate of 400µm diameter

At Si/$\text{Al}_2\text{O}_3$ interface the periodicity of Si crystal terminates. The dangling bonds of Si lead to interface states; these bonds have to be
passivated. Passivation is done by forming gas annealing (a mixture of N\textsubscript{2}:H\textsubscript{2} :: 10:1). The H atoms being light diffuse through dielectric and passivate the dangling bonds, thereby reducing the interface trap states. The fabricated structures were annealed for two hours at 400°C with maximum ramp rate in forming gas at a flow rate of 5 lit/min. Figure 6.10 shows the flow chart of the fabrication process.

Figure 6.10: Steps involved in the fabrication of MOS capacitors
6.7 Results of electrical and dielectric studies of Al/Al$_2$O$_3$/p-Si MOS capacitors

6.7.1 Effect of frequency on Capacitance – Voltage and Conductance – Voltage characteristics

The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were carried out in the frequency range of 100Hz-1MHz and temperature range of 300K - 430K respectively. The conductance technique is based on the conductance losses resulting from the flow of majority carriers at the interface to the majority carrier band of the semiconductor when a small ac signal is applied to the metal-oxide- semiconductor (MOS) structures. When the MOS structure is in the depletion the applied ac signal causes the Fermi level to oscillate about the mean position governed by the dc bias [1,3].

In this present study we made use of both Agilent 4284 Precision LCR Meter and Fluke PM 6306 programmable RCL meter with varying test signal of 50 mV$_{\text{rms}}$ and hold time of 100 ms. To compensate the cable impedance, open correction were carried out prior to each measurements and the signal is given at the back contact to mitigate the effect of parasitic impedances. The deep depletion depends upon the sweep rate of the test signal, therefore sufficient hold time was selected. In order to avoid deep depletion usually the DC voltage is swept from inversion to accumulation. All measurements were carried out with the help of a computer through an IEEE 488 interface.

Figure 6.11(a) shows the normalized low frequency C-V characteristics of Al/Al$_2$O$_3$/Si-p MOS capacitors at a frequency of 1 kHz. Thickness of the sample was measured using an ellipsometer. Maximum capacitance has been observed in the accumulation region and has a value of 1.11nF, which yields a dielectric constant of 9.478. Oxide thickness is extracted from the accumulation capacitance also and has a value of 9.45nm. It was observed that as the thickness of the oxide layer becomes thinner the more rapidly the capacitance changes with gate bias.

At low frequencies ideally the MOS capacitor is in thermal equilibrium under small-signal ac excitation, provided that minority carriers
can respond to variation in the ac field. In practice there will be some hole and electron traps at the Si/Al₂O₃ interface and in the bulk silicon. The system including these traps still will be in thermal equilibrium if all these traps immediately respond to the ac voltage. That is MOS capacitor will be in thermal equilibrium at all values of gate bias below the oxide breakdown field at low frequencies.

![Normalized capacitance vs Voltage](image)

**Figure 6.11(a):** Normalized low frequency C-V characteristics of an Al/Al₂O₃/p-Si MOS capacitor.

The different regions of MOS capacitor at low frequency are identified as accumulation -20V to -3.29V, depletion between -3.29 to -0.587V and inversion region at voltages above -0.587V. Due to the presence of interface trap charges and other charges the flat band voltage $V_{FB}$ is deviated from the ideal value (-0.83V).

The experimentally obtained normalized high frequency (1MHz) C-V curve of Al/Al₂O₃/p-Si (MOS) is shown in Figure 6.11(b). Accumulation capacitance density obtained is $1.06 \times 10^{-6}$ F/cm² at an electrode area of $1.256 \times 10^{-3}$ cm². Depending upon processing condition and Al₂O₃ thickness dielectric constant of the samples varied from 6.2 to 10.7. The slope of the C-
V curve is less than that predicted by exact charge theory indicating less interface traps density [1].

![Figure 6.11(b): Normalized high frequency (1 MHz) C-V Characteristics of an Al/Al₂O₃/p-Si(p-type) MOS capacitor. Inset shows the experimentally observed flatband voltage](image)

In practice experimental C-V characteristics are always different from ideal characteristics due the presence of non-ideal effects like interface trap and bulk charges. For the determination of non-ideal effects, it is necessary to calculate theoretical capacitance-voltage behavior of MOS capacitor. For this reason, doping concentration, \( (N_A) \) and flat band voltage values of Al/Al₂O₃/p-Si MOS capacitor are extracted by using the experimental high frequency \( 1/C^2 \) versus \( V_G \) graph as shown in Figure 6.11(b). The measurements were performed over different devices fabricated on the same wafer for the reliable and reproducible data collection. Therefore, the results here represent an average of different measurements. The doping concentration was experimentally measured by means of four point probe meter (model 280) and has a value of \( 5 \times 10^{15} \) cm\(^{-3}\). The flat band voltage value was extracted from \( 1/C^2 \)-\( V \) plot. Theoretical flat band voltage of the MOS device was calculated by using the equation 6.8 and obtained a
value of (-0.83V). The flat band voltage vary with the presence of oxide charges in the insulator material and is represent by Equation 6.13.

\[ V_{FB} = \Phi_{MS} - \frac{Q_{eff}}{C_{ox}} \]  \hspace{1cm} (6.13)

\[ N_{eff} = \frac{Q_{eff}}{q} \]  \hspace{1cm} (6.14)

Where \( Q_{eff} \) - total oxide charge, \( N_{eff} \) - Number density of total oxide charge, \( q \) - electronic charge.

Inset of Figure 6.11(b) shows the experimentally extracted \( V_{FB} \) which has a value of -2.1V. The flat band voltage shift to a more negative value with ideal value indicates the presence of positive fixed oxide charges. The net oxide charge presented in the sample and its number density is calculated as \( N_{eff} = 1.23 \times 10^{10} \), which is in the limit of good quality oxide layer reported for native SiO\(_2\) layers.

Figure 6.12: C-V hysteresis curve. Inset shows the shift in flat band voltage.
Figure 6.12 shows CV hysteresis curve and a shift in $V_{FB}$ is observed. By measuring the shift we calculated the trapped oxide charges present in the sample ($Q_{ot}$) using the equation 6.15 [21] and obtained a value of $1.93 \times 10^{-9} \text{C}$.

$$Q_{ot} = -\Delta V_{FB} \times C_{ox} \quad (6.15)$$

![Diagram of equivalent circuits](image)

Figure 6.13:(a) Low frequency equivalent circuit of the MOS capacitor, (b) High frequency equivalent circuit of the MOS capacitor [1].

Figure 6.13(a) & (b) show the low and high frequency equivalent circuit of the MOS capacitor [1]. Where $C_{ox}$-oxide capacitance, $C_s$-silicon surface capacitance and $C_{it}$-interface trap capacitance. At lower frequencies, the interface traps respond to ac voltage change and yield an excess frequency dependent capacitance ($C_{it}$). In high frequency region since the interface traps cannot follow the ac signal, the contribution of interface trap capacitance to the total capacitance is negligibly small [1,11,12].

Figure 6.14 depicts the C-V and $G/\omega$-V characteristics for Al/$\text{Al}_2\text{O}_3$/p-Si structure at different frequencies. The overall behavior is indeed that of an MOS device, with distinct regions of accumulation, depletion and inversion. As can be seen in the figure the values of capacitance and conductance are dependent on the bias voltage and frequency. The measured values of $C$ and $G/\omega$ at accumulation and depletion
region decrease with increasing frequency. This is an indication of the presence of interface states ($N_{ss}$) localized at semiconductor/oxide interface. The capacitance of such an inhomogeneous charge layer at the semiconductor/oxide interface will contribute an additional capacitance $C_{it}$ with the oxide capacitance causing frequency dispersion [1].

Figure 6.14: The frequency dependence of (a) C-V, (b) (G/ω)-V characteristics of Al/Al$_2$O$_3$/p-Si MOS structure at room temperature.
6.7.2 Effect of frequency on series resistance

At a given frequency, most of the errors in the $C-V$ and $G/\omega-V$ characteristics due to series resistance ($R_s$) occur in the strong accumulation region and a portion of the depletion region. The error can be minimized by measuring the $R_s$ and applying a correction to the measured $C$ and $G/\omega$ values before the desired information is extracted [1]. When the MOS structure is biased into strong accumulation, the frequency-dependent properties of MOS devices can be described via the complex impedance and the series resistance is the real part of the complex impedance as [1, 12].

\[
R_s = \frac{G_m}{G_m^2 + (\omega^2 C_m^2)}
\]  

(6.16)

where $C_m$ and $G_m$ are the measured capacitance and conductance, The capacitance of the oxide layer ($C_{ox}$) is obtained as

\[
C_{ox} = C_m [1 + (G_m/\omega C_m)^2]
\]

(6.17)

![Figure 6.15: Variation of $R_s$ of Al/Al₂O₃/p–Si structure as a function of the bias voltage at various frequencies.](image)
Figure 6.15 shows the variation of $R_s$ as a function of bias voltage in the frequency range of 50 kHz to 1 MHz. From the figure it is observed that $R_s$ shows a peak value and position of $R_s$ peak shift towards negative bias voltage from -0.4V to -0.9V when frequency increases from 50 kHz to 1 MHz. It can also be observed that as frequency increases peak value decreases and almost disappear at high frequencies (>500 kHz). Such behavior of $R_s$ is attributed to the particular distribution of localized interface states ($N_{ss}$) at Si/Al$_2$O$_3$ interface and the Al$_2$O$_3$ layer at the Al/p-Si interface. This type of behavior is reported in the case of Al/TiO$_2$/p-Si structures also [12,14].

### 6.7.3 Frequency dependence of dielectric properties

Dielectric constant ($\varepsilon$), dielectric loss ($\varepsilon''$), loss tangent (tan$\delta$) and ac electrical conductivity ($\sigma_{ac}$) were calculated from the values of capacitance and conductance measurements for Al/Al$_2$O$_3$/p-Si (MOS) structure in the frequency range of 1 kHz–1 MHz, at room temperature. The complex permittivity can be written [17,18] as

$$\varepsilon^* = \varepsilon' - i\varepsilon''$$

(6.18)

where $\varepsilon'$ and $\varepsilon''$ are the real and the imaginary parts of complex permittivity, and $i$ is the imaginary root of -1. The complex permittivity formalism has been employed to describe the electrical and dielectric properties. In this the following relation:

$$\varepsilon^* = \frac{Y^*}{j\omega C_0} = \frac{C}{C_0} - j \frac{G}{\omega C_0}$$

(6.19)

where, C and G are the measured capacitance and conductance of the dielectric material, $Y^*$-admittance and $\omega$-angular frequency ($\omega = 2\pi f$) of the applied electric field [18]. The real part of the complex permittivity, the dielectric constant ($\varepsilon'$), at the various frequencies is calculated using the measured capacitance values at the strong accumulation region from the relation [15,16]:


\[ \varepsilon' = \frac{C}{C_0} = \frac{C_{d_{ox}}}{\varepsilon_0 A} \]  

(6.20)

where \( C_0 \)-capacitance of the empty capacitor, \( A \)-electrode contact area, \( d_{ox} \)-oxide layer thickness and \( \varepsilon_0 \)-permittivity of free space \( (\varepsilon_0=8.85 \times 10^{-14} \text{ F/cm}) \). In strong accumulation region, the maximum capacitance of the MOS structure corresponds to oxide capacitance \( (C_{ox}) \). The imaginary part of the complex permittivity-the dielectric loss \( (\varepsilon'') \) at various frequencies is calculated using the measured conductance values from the relation,

\[ \varepsilon'' = \frac{G}{\omega C_0} = \frac{G_{d_{ox}}}{\varepsilon_0 \omega A} \]  

(6.21)

The loss tangent \( (\tan \delta) \) can be expressed as follows [12,17,16].

\[ \tan \delta = \frac{\varepsilon''}{\varepsilon'} \]  

(6.22)

The ac electrical conductivity \( (\sigma_{ac}) \) of the dielectric material is be given by the following equation [12,17, 18, 19].

\[ \sigma_{ac} = \omega C \left( \frac{d_{ox}}{A} \right) \tan \delta = \varepsilon'' \omega \varepsilon_0 \]  

(6.23)

The frequency dependencies of the \( \varepsilon' \), \( \varepsilon'' \) and \( \tan \delta \) of Al/Al\(_2\)O\(_3\)/p-Si structure vs. applied gate voltages are presented in Figure 6.16 a, b and c respectively. The values of \( \varepsilon' \), \( \varepsilon'' \) and \( \tan \delta \) calculated from the measured capacitance and conductance were found to be strong functions of applied voltage especially at low frequencies. Also, it is evident from Figure 6.16 that the values of \( \varepsilon'' \) and \( \tan \delta \) are almost independent of voltage at high frequencies. In principle, at low frequencies, all the four types of polarization processes, i.e., the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the values of \( \varepsilon' \) and \( \tan \delta \) [3,22,23].
Figure 6.16(a): The frequency dependence on dielectric constant of Al/Al₂O₃/p-Si structure at room temperature.

Figure 6.16 (b): The frequency dependence on dielectric loss of Al/Al₂O₃/p-Si structure at room temperature.
At accumulation region the values of $\varepsilon'$ and $\varepsilon''$ were found as 9.85 & 58.03, 8.19 & 13.08 and 5.85 & 3.81 at 10kHz, 100kHz and 1MHz respectively. On increasing frequency, the contributions of the interfacial, dipolar or the ionic polarization become ineffective leaving behind only the electronic part. As it can be seen from these figures $\varepsilon'$, $\varepsilon''$ and tan$\delta$ decrease as the frequency is increased. It is explained by the fact that as the frequency is raised, the interfacial dipoles have less time to orient themselves in the direction of the alternating field [14,24,25]. In high frequency range, the values of $\varepsilon'$ become closer to the values of $\varepsilon''$. This behavior of $\varepsilon'$ and $\varepsilon''$ may be due to the inability of interface states to follow the ac signal at such frequencies. The lifetime of interface trapped charges (τ) are much larger than $1/\omega$ at very high frequencies ($\omega$). Similar behavior is observed in several dielectric materials [1, 12].

Figure 6.16 (C): The frequency dependence on tangent loss of Al/Al$_2$O$_3$/p-Si structure at room temperature.
Figure 6.17: The frequency dependence of ac conductivity of Al/Al₂O₃/p-Si structure at room temperature

Figure 6.17 shows the dependence of ac electrical conductivity ($\sigma_{ac}$) on frequency [20,26-32]. $\sigma_{ac}$ is independent of frequency up to about 100kHz and thereafter increases sharply. $\sigma_{ac}$ depends on dielectric loss according to Equation 6.23. As observed in figure 6.16(b) dielectric loss decreases with increasing frequency and this explains the increase in $\sigma_{ac}$ with frequency. This result is in agreement with the literature [20].

**6.7.4 Temperature dependence of capacitance, conductance and dielectric properties**

Figure 6.18(a) and (b) show the temperature dependant C –V and G/ω –V characteristic of Al/Al₂O₃/p-Si MOS capacitor at 1MHz frequency. Comparing with the ideal characteristics the experimentally obtained one has some flatband shift along the voltage axis. As temperature increases shift in voltage axis decreases and move closer to ideal value. We can observe in the figure that the depletion regions of all curves are nearly parallel, without any stretch out. This is because at 1MHz frequency the interface charges which cause stretch out have already ceased to contributing to the total capacitance.
Hence as temperature varies from 300 to 430k the change in any of the charges ($Q_f$, $Q_M$ or $Q_{ot}$) or combination of these only may cause shift in flat band voltage.

![C-V characteristics of Al/Al$_2$O$_3$/Si capacitor at 1MHz.](image1)

![G-V characteristics of Al/Al$_2$O$_3$/Si capacitor at 1MHz.](image2)

Figure 6.18: Temperature dependent (a) C-V, (b) G-V characteristics of Al/Al$_2$O$_3$/Si capacitor at 1MHz.
In Figure 6.19 we have found that $\Delta V_{FB}$ decreases as temperature rises. This means the C-V curve shifts towards right side along the voltage axis (Figure 6.18(a)). Hence at any particular measurement voltage in the depletion region, the measured capacitance will increase with increase in temperature. At low frequencies the variation will be more because of the effect of interface trapped charge on capacitance. It implies that charges in the interface traps get de-trapped at higher temperature, which thus contribute to conductance $G$. The low frequency curve in Figure 6.22(b) supports this conclusion.

Flat band voltage for each temperature was experimentally calculated from C-V curve. The shift in Flat band ($\Delta V_{FB}$) from ideal value for each temperature was plotted against temperature as shown in Figure 6.19. Inset of Figure 6.19 shows flat band voltage of the fabricated capacitor at 300K. As temperature increases flat band shift decreases. This may be due to the reduction of the total oxide charge density and the interface-trap density at higher temperature [1].
Figure 6.20: The temperature dependence of (a) capacitance, (b) conductance \( G/\omega \) of Al/Al\(_2\)O\(_3\)/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1 MHz).

Figure 6.20(a) and (b) shows the measured C–T and G/\( \omega \)–T characteristics of the Al/Al\(_2\)O\(_3\)/P-Si MOS structure at various frequencies.
(5kHz, 100kHz, 1MHz) in depletion region. It is clear that the C–T and Gm/ω–T curves are quite sensitive to frequency and temperatures especially at low frequency and high temperature. The values of C and G/ω increase with increasing temperature.

The results of the temperature dependences of ε', ε'' and tan δ for the Al/Al₂O₃/p-Si are plotted in the Figure 6.21(a),(b) and (c) in the temperature range of 300 to 430K and at various frequencies (5kHz, 100kHz and 1MHz). At low frequency (5kHz), on increasing the temperature from 300 to 390K, the ε' value increases rapidly from 2.3 to as large as 10.17. The tanδ value decreases from 7.3 at 300K to 3 at 390K and then increases with increasing temperature. At high frequencies (100kHz, 1 MHz) it has been observed that the variation of ε' and ε'' is negligible up to 390K and then increases with temperature. Tanδ is almost independent of temperature at high frequencies.

![Figure 6.21: Temperature dependence of dielectric properties (a) dielectric constant (ε').](image-url)
Figure 6.21: Temperature dependence of dielectric properties (b) dielectric loss ($\varepsilon''$)

Figure 6.21: (c) Temperature dependence of dielectric loss tangent ($\tan\delta$).
The explanation of Figure 6.21(a) can be same as that of Figure 6.20(a). Here as capacitance \( C \) varies in certain way, naturally \( \varepsilon' \) will follow the curve of \( C \). By increasing temperature, the number of charge carriers increase and thus produces further space charge polarization and hence leads to a rapid increase in the capacitance and hence dielectric constant. Of course, both types of charge carriers \( n \) and \( p \) contribute to the polarization. However, the \( n \)-type contribution is negligible, where the dominant charge carriers are holes [18,20]. This increase in carrier concentrations is verified by conductance measurement and results are shown in Figure 6.22 b.

Furthermore, the increase in temperature induce an expansion of molecules which causes some increase in the electronic polarization [12,33–35]. The temperature causes a loosening of the rigid structure and hence results in an increase in dipole orientation and an increase in \( \varepsilon', \varepsilon'' \) and \( \tan\delta \). Since \( \varepsilon'' \) proportional to \( G \) it follows the same nature of \( G \). These results show that this MOS structure possess better dielectric properties at temperatures higher than room temperature.

6.7.5 Effect of temperature on series resistance

Frequency and temperature dependence of series resistance can be obtained from the measurements of \( C-\omega-T-f \) and \( G/\omega-T-f \) data plotted in Figure 6.22 (a) and is clear that the series resistance has an inverse relation with frequency and temperature. The major parameters which affect series resistance are the presence of interface states and its particular distribution of \( N_{ss} \). At high frequencies the interface trapped charges cannot follow the ac signal and consequently cannot contribute to the total capacitance and conductance. Similarly at high temperature the contribution of majority carriers and charges released from the interface states cause the decrease in \( R_s \) values. From figure 6.22(a) it is clear that at high frequency (1MHz) series resistance is almost independent of temperature. This implies trapping of charges at low temperature get reflected on low frequency \( R_s \) values.
Figure 6.22(a): Variation of series resistance with temperature of Al/Al$_2$O$_3$/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1MHz).

Figure 6.22 (b): Variation of conductance with temperature of Al/Al$_2$O$_3$/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1MHz).
Figure 6.23: Temperature dependence of ac conductivity at frequency of 1MHz.

Figure 6.24: Arrhenius plot of Al/Al$_2$O$_3$/p-Si MOS structure at a frequency of 1MHz.
Figure 6.23 & 6.24 show the temperature dependence of ac conductivity at a frequency of 1MHz. According to literature report [20,36], the increase in the electrical conductivity at low temperature is attributed to the impurities, which reside at the grain boundaries of Al₂O₃. These impurity levels lie close below the bottom of the conduction band and thus it has a small activation energy.

A linear relationship between the total conductivity and the inverse temperature could be written as

\[ \sigma_{ac} = \sigma_0 \exp\left(-\frac{E_a}{kT}\right) \]  \hspace{1cm} (6.22)

By analyzing the temperature dependence of ac conductivity, the activation energy can be determined from the slope of Arrhenius plot (\(\sigma_{ac}\) vs.1000/T) [20,36-39]. From Figure 6.24 it is clear that the ac conductivity begins to change rapidly above 380K. From Arrhenius plot we get activation energy values as 110.6meV at temperature <390K and 321meV at temperature >390K respectively.

6.7.6 Current –Voltage (I-V) analysis

![I-V Characteristics of Al/Al₂O₃/p-Si MOS capacitor](image)

Figure 6.25: J-V Characteristics of Al/Al₂O₃/p-Si MOS capacitor
Figure 6.25 shows J-V the (current density - voltage) characteristics of Al/Al₂O₃/p-Si capacitor with a physical thickness of 24nm measured using a Keithley 485 pico ammeter and an ALSPC-02 data acquisition card. In negative bias condition (accumulation) the gate current is mainly conducted by the electron injected from the metal gate to the conduction band and consequently increases with increasing gate voltage. The current level in the negative bias condition depends on the oxide thickness, which increases with decreasing oxide thickness.

In substrate injection region (inversion), conduction is basically by the minority carrier generation from back contact, interface states and bulk traps [41,42]. At room temperature current component due to this minority carrier diffusion from back contact can be neglected, while it dominates at higher temperature. Thus the gate current in depletion region at room temperature is mainly due to by the minority carrier generation from the interface states and bulk trap. The amount of charge carriers from interface states should be invariant under deep depletion. Therefore gate current shows a nearly saturation tendency under deep depletion [39-41].

![Figure 6.26: Temperature dependent J-V Characteristics](image)
The leakage current densities were obtained in the order of $10^{-6}$ A/cm$^2$ at an applied gate voltage of 1V corresponding to a resistivity of $1.5 \times 10^{13}$ Ohm-cm. Temperature dependent I-V were studied (Figure 6.26) and it was found that as temperature was increased leakage current also increased.

From J-V characteristics the dc conductivity was extracted (Figure 6.27). It is clear that as temperature increases dc conductivity increases.

![Figure 6.27: Temperature dependent dc conductivity](image)

Figure 6.27 is J-E plot of Al$_2$O$_3$ film having 24nm thickness and shows very low current density in the order of $10^{-7}$A/cm$^2$ at low applied fields. This current is attributed to a combination of leakage current and charging current due to capacitive charging. The values of current density is lower at lower field and saturated at a field of 0.5 MV/cm to 3MV/cm and then increased. This behavior is observed in the case of SiO$_2$ thin film also. This may be due to phonon assisted tunneling in neutral traps or series resistance in measurement structure. The sudden increase in current at low field may be due to the breakdown at defects or weak spot in the dielectric and followed by self healing. It is possible that localized current surges evaporated small regions of the Al metal contact from the surface thus preventing further conduction [40,42]. Thin Al$_2$O$_3$ films exhibit low stress induced leakage current effect. Very good transistor properties were reported.
for films having low stress induced effect. Breakdown is observed at a field of 3.8 MV/cm, which is higher than the reported value of sapphire (0.5 MV/cm) [40].

![J-E characteristics of Al/Al₂O₃/p-Si MOS capacitor](image)

**Figure 6.28**: J-E characteristics of Al/Al₂O₃/p-Si MOS capacitor

### 6.8 Conclusions

MOS capacitors were fabricated successfully using nano layers of Al₂O₃ as dielectric, which is deposited by Atomic Layer Deposition. Frequency and temperature dependence of electrical and dielectric properties of Al/Al₂O₃/p-Si (MOS) capacitor have been studied in detail in the wide range of frequencies (5kHz to 1MHz) and temperature (300–430K) respectively. It was observed that the values of capacitance (C) and conductance (G/ω) decrease with increasing frequency and decreasing temperature. Experimental results verified that the frequency, temperature and bias voltage dependence of ε', ε'', and tanδ. The ac conductivity increases with increasing frequency and temperature for each bias voltage. The increase in capacitance with temperature at low frequency can be attributed to a shift in flat band voltage and effects of interface trap charges present in the oxide material. The observed high values of ε' and ε'' at low frequencies are attributed to flat band voltage shift and conductivity which is directly related to the increase in the mobility of localized charge carriers at
interface states. Also interface traps can easily follow the ac signal at low frequencies and yield an excess capacitance and conductance. Series resistance of the structure decreases with increasing frequency and temperature. Thus we can draw a conclusion that the electrical and dielectric properties of Al/Al$_2$O$_3$/p-Si structure depend on the quality of the oxide layer, the density of interface traps and series resistance of the structure. These three are closely related to applied gate voltage, frequency and temperature.

References


