CHAPTER 6

DDCC AND DX-DDCC BASED ACTIVE FILTER

This chapter deals with the two new current mode devices, Differential Difference Current Conveyor (DDCC) and Dual-X Differential Difference Current Conveyor (DX-DDCC). The applications of DDCC and DX-DDCC are discussed in this chapter. DDCC is used to realize a notch filter, while DX-DDCC is used for the realization of universal filter. These circuits offer high input and output impedances, low sensitivity to parameter variations. The realized universal filter is having on chip tunability.

The following sections present the basic structure of DDCC, its application as notch filter followed by structure of DX-DDCC and its application as universal filter.

6.1 DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR

Current mode circuits such as current conveyors and current feedback operational amplifiers are receiving much attention as compared to voltage mode circuits due to higher bandwidth, low power consumption and wider dynamic range. Considering these advantages of current mode circuits, several current mode and voltage mode filters have been realized. In 1970 Sedra [115] introduced second generation current conveyor (CCII) having very high input and output impedances. Since then several applications such as amplifier, integrator, differentiator, filters, oscillators and signal processing circuits using CCII have been proposed in the literature.

Since CCII has only one input voltage terminal, it cannot be employed in applications such as automatic control systems and instrumentation systems where differential voltage signals are commonly employed. Further, conventional CCII cannot be used in continuous time analogue signal processing which require differential or floating inputs. For such applications, circuit may have to be designed with two or more CCIIIs. The differential difference amplifier (DDA), proposed by Sakinger and Guggenbuhl [60], has been used in applications such as switched capacitor circuits, common mode detection, telephone line adaptation, multiple-weighted input comparator and continuous-time filters. Lesser number of passive components is necessary for realizations of circuits employing DDA rather than with CCIIIs.
Chiu et al. [156] proposed a new versatile building block, referred as differential difference current conveyor (DDCC), which combines the advantages of both the CCII and DDA. The DDCC is a five terminal device with electrical symbol, shown in Figure 6.1.

![Figure 6.1: Symbolic representation of DDCC](image)

The terminal relations for this device are described by the equation 6.1.

\[
\begin{bmatrix}
V_x \\
I_{y1} \\
I_{y2} \\
I_{y3} \\
I_z
\end{bmatrix} =
\begin{bmatrix}
0 & 1 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
\pm 1 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_x \\
V_{y1} \\
V_{y2} \\
V_{y3} \\
V_z
\end{bmatrix}
\]

(6.1)

The plus and minus signs in equation 6.1 represents the configuration of current conveyor being positive or negative. These configurations are referred as CCII+ and CCII− respectively.

Positive DDCC can be realized by the commercially available Operational Transconductor Amplifier (LM13700) and monolithic Op-amp (AD844) as shown in Figure 6.2.
Considering equal bias current to both operational transconductance amplifiers, the output voltage \( V_o \) at the node 3 can be expressed as

\[
V_o = [V_{y1} - V_{y2} + V_{y3}]
\]  

(6.2)

The monolithic Op-amp Ad 844 is used in the open loop mode. In open loop mode it acts as current conveyor. Thus potential at node 3 is available at node 2 named as X terminal. The current flowing through the X terminal will be as same as current flowing through the terminal 5 of the AD844 named as Z terminal. Thus complete circuit realizes the property of DDCC.

Chiu et al. [144] have employed DDCC to realize various linear and non-linear circuits such as differential squarer, multiplier, biquad etc. Several voltage-mode notch filters using various active devices have also been reported [145]-[160]. The notch filter, shown in Figure. 6.3, proposed by Temizyurek and Myderrizi [150] in 2004 employ two DDCC, two resistance and two capacitances.
Figure 6.3: Notch filter realization by Temizyurek and Myderrizi using DDCC

The transfer function of the filter is given by:

\[
\frac{V_{out}}{V_{in1}} = \frac{s^2 + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \left( \frac{1}{R_1 C_1} + \frac{1}{R_1 R_2 C_1 C_2} \right)}
\]  

(6.3)

The notch frequency and the quality factor of their filter are respectively given by:

\[
\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}
\]  

(6.4)

\[
Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}}
\]  

(6.5)

This circuit has low sensitivity to parameter variation of passive components. Both the input and output impedances of the circuit are high.

In 2007, Chiu and Horng [155] realized high input and low output impedance notch filter using three DDCC, two resistances and two grounded capacitance, shown in Figure 6.4.
The transfer function of the filter is given by:

\[
\frac{V_{out}}{V_{in}} = \frac{s^2 + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s \left( \frac{1}{R_1 C_1} + \frac{1}{R_1 R_2 C_1 C_2} \right)}
\]  

(6.6)

The notch frequency and the quality factor of their filter are respectively given by:

\[
\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}
\]  

(6.7)

\[
Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}}
\]  

(6.8)

This circuit is good for the cascading, but it uses more number of passive components.

The circuits discussed above use more than one active component and several passive components. In the following section proposed voltage mode notch filter circuit and the simulation results based on the analysis of the circuit are discussed.
6.2 PROPOSED VOLTAGE MODE NOTCH FILTER CIRCUIT

Figure 6.5 shows the proposed voltage mode notch filter employing one DDCC+, two resistors and two capacitors.

Nodal analysis of the circuit shown in Figure 6.5 yields the following transfer function:

\[
\frac{V_o}{V_i} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{6.9}
\]

where \(Z_1 = (sR_1C_1 + 1)/(sC_1)\) and \(Z_2 = R_2/(1 + sR_2C_2)\),

Substituting the values of \(Z_1\) and \(Z_2\) in equation (6.11), we obtain:

\[
\frac{V_o}{V_i} = \frac{s^2R_1R_2C_1C_2 - s(R_1C_1 + R_2C_2 - R_2C_1) + 1}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 + R_2C_1) + 1} \tag{6.10}
\]

With \(R_2 = 2R_1\) and \(C_2 = 2C_1\), the biquad transfer function reduces to the following transfer function of a notch filter.

\[
\frac{V_o}{V_i} = \frac{s^2 + \frac{1}{4R_1^2C_2^2}}{s^2 + \frac{2s}{R_1C_2} + \frac{1}{4R_1^2C_2^2}} \tag{6.11}
\]
The notch frequency \( \omega_0 \) of the filter is

\[
\omega_0 = \frac{1}{2R_1C_2}
\]  

(6.12)

The \( \omega_0 \) sensitivities of the proposed circuit notch filter are

\[
S_{R_1}^{\omega_0} = 1
\]  

(6.13)

\[
S_{C_2}^{\omega_0} = 1
\]  

(6.14)

### 6.2.1 PERFORMANCE ANALYSIS WITH NON IDEAL DDCC

Considering non-ideal behavior of DDCC, the analysis of the circuit may be carried out using the following terminal relations

\[
\begin{bmatrix}
V_x \\
I_{y_1} \\
I_{y_2} \\
I_{y_3} \\
I_z
\end{bmatrix} =
\begin{bmatrix}
0 & \alpha_1 & \alpha_2 & \alpha_3 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
\pm \beta & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_x \\
V_{y_1} \\
V_{y_2} \\
V_{y_3} \\
V_z
\end{bmatrix}
\]  

(6.15)

where \( \alpha_k = 1 - \varepsilon_{vk} \) and \( \beta = 1 - \varepsilon_i \) for \( k = 1, 2, 3 \).

### 6.2.2 ZERO ACTIVE PARAMETER SENSITIVITY NOTCH FILTER REALIZATION USING FREQUENCY INSENSITIVE VOLTAGE AND CURRENT TREKKING ERROR PARAMETERS \( \varepsilon_v \) AND \( \varepsilon_i \) OF DDCC

The parameters \( \varepsilon_{vk}, \varepsilon_i \) (\( |\varepsilon_{vk}|, |\varepsilon_i| \ll 1 \)) are respectively referred as the voltage and current trekking error of DDCC. Considering non-ideal behavior of DDCC, defined by equation (6.15), the analysis of the filter circuit yields the following modified transfer function
\[
V_i = \frac{1}{\alpha_3} \times \frac{sR_z C_z (1 + \alpha_2 - \alpha_1) - \alpha_1 (s^2 R_z R_z C_z C_z + s (R_z C_z + R_z C_z) + 1)}{s^2 R_z R_z C_z C_z + s (R_z C_z + R_z C_z + R_z C_z) + 1}
\] (6.16)

Under the constraint \( R_z C_z (1 + \alpha_2 - \alpha_1) = \alpha_1 (R_z C_z + R_z C_z) \) or equivalently with the ratio of time constants,

\[
\frac{R_z C_z}{R_z C_z} = \frac{\alpha_1}{(1 + \alpha_2 - 2\alpha_1)}
\] (6.17)

We obtain the transfer function of the notch filter with the notch frequency

\[
\omega_n = \frac{1}{\sqrt{R_z R_z C_z C_z}}
\] (6.18)

which is independent of voltage/current trekking error.

With the constraint \( R_z = 2R_z \) and \( C_z = 2C_z \), the notch frequency given by equation 6.18 for the realization with non-ideal DDCC remains unaffected and turns out to be same as that available for the notch filter realization with ideal DDCC.

The sensitivity to variations in active components of the filter is zero as shown by equation

\[
S_{\alpha_1} = S_{\alpha_2} = S_{\alpha_3} = 0
\] (6.19)

### 6.2.3 Analysis Based on Frequency Sensitive Voltage and Current Trekking Error Parameters \( \varepsilon_{v_k} \) and \( \varepsilon_i \)

Considering the non-idealities of the DDCC by assuming both the current and voltage trekking errors are frequency dependent, \( \alpha_k \) and \( \beta \) can be modeled as

\[
\alpha_k (s) = \frac{\alpha_{0k}}{1 + s \tau_{v_k}}
\] (6.20)
\[ \beta(s) = \frac{\beta_0}{1 + s \tau_i} \]  

(6.21)

where

\[ \tau_{i_k} = \frac{1}{2\pi f_{i_k}} \]  

(6.22)

\[ \tau_i = \frac{1}{2\pi f_i} \]  

(6.23)

where \( \alpha_0k \) and \( \beta_0 \) for \( k = 1,2,3 \) denote their lower frequency values, \( f_i \) and \( f_{i_k} \) denotes the 3dB bandwidths of the current and voltage transfer functions respectively. Reanalysis of the filter circuit yields fourth order transfer function as follows:

\[ \frac{V_0}{V_i} = \frac{1}{\alpha_{03}} \begin{bmatrix} \alpha_{02} \tau_{i1} - \alpha_{01} \tau_{i2} & + R_C \tau_{i2} \left( 1 + \alpha_{02} \right) - R_C \alpha_{01} \left( 1 + \alpha_{02} - \alpha_{01} \right) + 1 \\ \alpha_{02} \tau_{i1} - \alpha_{01} \tau_{i2} & + R_C \tau_{i2} \left( 1 + \alpha_{02} - \alpha_{01} \right) - R_C \alpha_{01} \left( 1 + \alpha_{02} - \alpha_{01} \right) + 1 \\ \alpha_{02} \tau_{i1} - \alpha_{01} \tau_{i2} & + R_C \tau_{i2} \left( 1 + \alpha_{02} - \alpha_{01} \right) - R_C \alpha_{01} \left( 1 + \alpha_{02} - \alpha_{01} \right) + 1 \\ \alpha_{02} \tau_{i1} - \alpha_{01} \tau_{i2} & + R_C \tau_{i2} \left( 1 + \alpha_{02} - \alpha_{01} \right) - R_C \alpha_{01} \left( 1 + \alpha_{02} - \alpha_{01} \right) + 1 \end{bmatrix} \]

(6.24)

It is obvious that the extra poles appear in the filter characteristics. Routh-Hurwitz stability criterion shows that no stability problem is caused by the new poles. However, the transfer function may be simplified if the effect of the far off pole could be neglected for specific values of the trekking parameters.

6.2.4 SIMULATION RESULT

The DDCC has been realized on bread board using two LM13700 and Op-amp AD844 with a supply voltage of ±5V and bias current of 0.215mA. With pre-selection of resistors and capacitors \( R_2 = 2R_1 = 2 \, k\Omega \) and \( C_1 = 2C_2 = 2 \, nF \), having a spread of two, a notch frequency \( (\omega_0) \) of 79.57kHz is realized by the DDCC based filter circuit shown in Figure 6.3. PSPICE has been used for simulation of the proposed circuit. The simulation results are shown in Figure 6.6.
match the designed specifications. By measuring the non linearity in the DDCC $\alpha_{o_1} = 0.9941, \alpha_{o_1} = 0.9941, \alpha_{o_1} = 0.9941$ and $\tau_{v1} = \tau_{v2} = \tau_{v3} = 24.76\,ns$, the poles are found to be in the negative half plane and the response of the transfer function shown in equation no. 6.24 matches with equation no. 6.11.

**Figure 6.6 (a):** Magnitude response of proposed notch filter using DDCC

**Figure 6.6(b):** Phase Response of proposed notch filter using DDCC
6.3 DUAL-X DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR (DX-DDCC)

Zeki and Toker [157] proposed a new active device dual-X current conveyor (DXCCII) for continuous time filtering. This device achieves tunability by employing triode MOSFETs, while maintaining linearity with large input signals. It also reduces the required number of active devices and MOSFET resistors in a MOSFET-C continuous time filters. It does not require any matching of component. Based on DXCCII, Yamach and Kuntman [158] proposed DX-DDCC, an extension of the DDCC having two X terminals as compared to DDCC. They have realized a Kerwin-Huelsman-Newcomb (KHN) filter using DX-DDCC. The electrical symbol of DX-DDCC is shown in Figure 6.7.

![Electrical Symbol of Dual X- Differential Difference Current Conveyor (DX-DDCC)](image)

**Figure 6.7:** Electrical Symbol of Dual X- Differential Difference Current Conveyor (DX-DDCC)

The terminal relations for this device are described by the equation (6.27):

\[
\begin{bmatrix}
V_x \\
I_{y1} \\
I_{y2} \\
I_{y3} \\
I_z^+ \\
I_z^-
\end{bmatrix}
= \begin{bmatrix}
0 & 1 & -1 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\begin{bmatrix}
I_x \\
I_{y1} \\
I_{y2} \\
I_{y3} \\
I_z^+ \\
I_z^-
\end{bmatrix}
\tag{6.27}
\]

In the following subsection proposed resistance less multifunction circuit and simulation results are discussed.
6.3.1 PROPOSED RESISTANCELESS MULTIFUNCTION CIRCUIT

The proposed circuit comprising two DX-DDCC, two MOSFETs and two capacitors is shown in Figure 6.8.

![Proposed circuit](image)

**Figure 6.8:** Proposed resistance less multifunction circuit using DX-DDCC

The nodal analysis of the circuit yields the following transfer function:

\[
V_{\text{out}} = \frac{s^2 y_2 y_4 V_{\text{in2}} + s y_1 y_4 V_{\text{in3}} + y_1 y_3 V_{\text{in1}}}{s^2 y_2 y_4 + s y_1 y_4 + y_1 y_3}
\]  

The low pass, high pass, band pass, notch and all pass filter configuration can be obtained by using proper selection of input voltages as shown in the Table 6.1.

<table>
<thead>
<tr>
<th>Filter Type</th>
<th>(V_{\text{in1}})</th>
<th>(V_{\text{in2}})</th>
<th>(V_{\text{in3}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low pass</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High pass</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Band pass</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 6.1: Various filter responses using DX-DDCC
The natural frequency and the quality factor of the filters are obtained as:

\[
\omega_0 = \frac{y_1 y_3}{\sqrt{y_2 y_4}}
\]

(6.29)

\[
Q = \frac{y_3 y_2}{y_1 y_4}
\]

(6.30)

where \( y_1 = y_3 = 1/R = 2\beta(V_{c} - V_{TN}) \), \( y_2 = sC_1 \) and \( y_4 = sC_2 \). Substituting the above values in equation (6.29) and (6.30), we obtain:

\[
\omega_0 = \frac{2\beta(V_{c} - V_{TN})}{\sqrt{C_1 C_2}}
\]

(6.31)

\[
Q = \frac{C_1}{\sqrt{C_2}}
\]

(6.32)

As per equation (6.31) and (6.32), \( \omega_0 \) and \( Q \) are orthogonal. By simply changing the control voltage \( V_C \) the cutoff frequency of the filter can be changed while keeping the same \( Q \) factor. The sensitivities of \( \omega_0 \) and \( Q \) to the passive elements are:

\[
S_{\omega_0}^{C_1, C_2} = -\frac{1}{2}
\]

(6.33)

\[
S_{Q}^{C_1, C_2} = \frac{1}{2}
\]

(6.34)

These sensitivities are independent of the network parameters and are low.

**6.3.2 SIMULATION RESULTS AND PERFORMANCE ANALYSIS**

Theoretical analysis is verified by the PSPICE simulation of the given circuit realized with MIETEC 0.5\( \mu \)m CMOS technology process parameters. The CMOS model of DX-DDCC is shown in Figure 6.9. The aspect ratio of the MOS transistor is given in Table 6.2. The passive elements of the filter are selected as \( C_1 = C_2 = 2 \) pF for the cutoff frequency 10MHz. The drain and source supply voltages \( V_{DD} \) and \( V_{SS} \) of 2.5V and -2.5V have respectively been employed which are same as those used in the realization of DDCC. The circuit has been
designed with a biasing voltage of $V_{B1}$=1.67V, $V_{B2}$=1.4V and $V_{B3}$=1.4V. The results obtained from the lowpass, highpass, bandpass, notch and all pass filters by considering control voltage 1.4V are shown in the Figure 6.10 match with the designed specifications.

**Table 6.2:** Transistor dimension of the CMOS DX-DDCC circuit shown in Figure 6.9

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(µm)</th>
<th>L(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>1.6</td>
<td>1</td>
</tr>
<tr>
<td>M5-M6</td>
<td>28.8</td>
<td>1</td>
</tr>
<tr>
<td>M7-M8</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>M9-M10</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>M11-M12</td>
<td>90</td>
<td>1</td>
</tr>
<tr>
<td>M13</td>
<td>86</td>
<td>1</td>
</tr>
<tr>
<td>M14</td>
<td>8.1</td>
<td>3.5</td>
</tr>
<tr>
<td>M15</td>
<td>15</td>
<td>1.2</td>
</tr>
<tr>
<td>M16</td>
<td>5</td>
<td>1.2</td>
</tr>
<tr>
<td>M17-M20</td>
<td>30</td>
<td>1</td>
</tr>
</tbody>
</table>
Figure 6.9: CMOS realization of DX-DDCC

Figure 6.10(a): Frequency response of HP, LP and BP filter employing DX-DDCC
6.4 CONCLUSION

This chapter considers the concept of Differential Difference Current Conveyor (DDCC). A Notch filter is realized using single DDCC and two resistors and two capacitors with a component spread of two. Subsequently for on chip tuning a modified DDCC called Dual-X Differential Difference Current Conveyor is discussed. By employing the DX-DDCC a universal filter is proposed with a minimum number of passive elements i.e. only 2. It requires two DX-DDCC, two MOSFET along with two capacitors. The circuit has the following features: on chip automatic tuning of cutoff frequency, realization of all filters, less passive components, low sensitivity, $\omega_0$ and $Q$ are orthogonally adjustable.