CHAPTER 3

JITTER OPTIMIZATION OF SELF BIASED PLL

The traditional self biased PLL when proposed, was designed with loop parameters optimally chosen mainly to minimize input tracking jitter. Accordingly the loop bandwidth of the system was chosen as wide as possible and the system was designed to be over damped. This work follows a similar choice in its loop parameters for minimum jitter and also discusses the possible alternative choices in its system parameters that can minimize jitter performance. The impact of these chosen system parameters in jitter performance is described using Noise Transfer Functions (NTFs) in this chapter. Even though the traditional self biased PLL discusses the choice of its loop parameters for optimum jitter performance, an optimum choice in its circuit parameters for various functional blocks that impact jitter performance was not derived. The present work thus attempts to derive these circuit parameters optimally. The adopted methodology in choosing the circuit parameters is discussed. Using the optimally derived circuit parameters, circuit simulations were carried out and the results are presented.

3.1 IMPACT OF SYSTEM PARAMETERS ON JITTER PERFORMANCE

The jitter performance of the traditional self biased PLL can be normally studied by considering the NTFs and the noise Power Spectral

Densities (PSDs) of the various functional blocks of the PLL. The overall PLL output noise PSD $\overline{\Phi^2_{out,\,n}}$ is given by (as given in Robert Nonis et al (2005) for e.g.),

$$\overline{\Phi^2_{out,n}} = \overline{\Phi^2_{out,cp,n}} + \overline{\Phi^2_{out,lpf,n}} + \overline{\Phi^2_{out,vco,n}} + \overline{\Phi^2_{out,div,n}} .$$

$$= |H_{CP}|^2\overline{i^2_{cp,n}} + |H_{LPF}|^2\overline{v^2_{lpf,n}} + |H_{VCO}|^2\overline{\Phi^2_{vco,n}} + |H_{DIV}|^2\overline{\Phi^2_{div,n}} . \qquad (3.1)$$

In the above expression, $\overline{\Phi^2_{out,cp,n}}$, $\overline{\Phi^2_{out,lpf,n}}$, $\overline{\Phi^2_{out,vco,n}}$ and $\overline{\Phi^2_{vco,n}}$ represent the output phase noise PSD due to charge pump, loop filter, VCO and divider. H_{CP}, H_{LPF}, H_{VCO} and H_{DIV} represent the NTFs of the blocks CP_1, LPF, VCO and Prescalar blocks respectively. The quantities $\overline{i^2_{cp,n}}$, $\overline{v^2_{lpf,n}}$, $\overline{\Phi^2_{vco,n}}$ and $\overline{\Phi^2_{div,n}}$ represent the PSD's of the corresponding noise sources. The expressions for the NTFs of the various functional blocks as described in Robert Nonis et al (2005) are given in (3.2), (3.3), (3.4) and (3.5). The purpose of these Equations being reproduced here is to identify the key parameters that contribute to jitter and to suggest a methodology to reduce jitter.

$$H_{cp}(s) = \frac{N.F_{lpf}(s).2\pi K_{VCO}}{N.s + I_{cp}.F_{lpf}(s).K_{VCO}} \qquad (3.2)$$

$$H_{LPF}(s) = \frac{N.2\pi K_{VCO}}{N.s + I_{cp}.F_{lpf}(s).K_{VCO}} . \qquad (3.3)$$

$$H_{VCO}(s) = \frac{N.s}{N.s + I_{cp}.F_{lpf}(s).K_{VCO}} . \qquad (3.4)$$

$$H_{DIV}(s) = \frac{N.I_{cp}.F_{lpf}(s).K_{VCO}}{N.s + I_{cp}.F_{lpf}(s).K_{VCO}} . \qquad (3.5)$$

If one considers the system parameters K_{VCO}, I_{cp}, and the loop filter cutoff frequency, it is well known that and as discussed in Robert Nonis et al (2005), Van de Beek et al (2004), they strongly influence the NTFs as well the noise PSDs (though the latter dependence is not explicitly shown). Further, the random noise contribution alone is captured in the above equations. Overall jitter also has a systematic component in it, and this is also a function of I_{cp} and K_{VCO} as described in Chembiyan Thambidurai et al (2010). Further, these latter quantities themselves are intricately related through constraints on loop natural resonant frequency ω_n and damping constant ζ given by

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{cp}.K_{VCO}.C}{N}}. \tag{3.6}$$

$$\omega_n = \sqrt{\frac{I_{cp}.K_{VCO}}{N.C}}. \tag{3.7}$$

Given all the above dependencies, the selection of optimum values of K_{VCO} and I_{cp} for minimizing overall jitter is a non trivial task. Further minimizing overall jitter implies reducing the noise PSDs as well as the NTFs of the various blocks.

Considering first the possibility of the reduction of the noise PSDs of the individual blocks, the dominant noise sources within the key blocks like charge pump and the VCO have to be identified, and then suitably altered to the extant permissible without disturbing the PLL loop dynamics. Hence, given the overall PLL loop characteristics, the device dimensions of VCO and charge pump circuits are carefully chosen such that their reduced

noise PSD leads to overall minimum jitter. These design aspects are described below.

3.2 DESIGN OF PLL FUNCTIONAL BLOCKS FOR MINIMUM JITTER

The VCO and charge pump circuits are generally considered to have the predominant contributions to the overall jitter (Robert Nonis et al (2005) & Van de Beek et al (2004)) and are mainly analyzed for minimum noise contribution from these functional blocks. Description on the design of VCO functional block for minimum jitter is given first and following is the discussion on the design of charge pump circuit.

3.2.1 Design of VCO functional block for minimum jitter

In the ring oscillator based VCO, the delay element that decides oscillator frequency is designed for minimizing overall jitter. In the previous chapter, a feasible range for device dimensions that satisfies functional specifications of the traditional self biased PLL was derived. The present work selects the jitter sensitive devices in the delay element and chooses the dimensions of these devices within the derived range through simulation, in a manner that minimizes the noise PSD contribution to overall jitter.

The devices that adversely affect jitter performance are the switch transistors M_2-M_3 and the symmetric load transistors M_4-M_7 of the delay element circuit shown in Figure 2.5, whereas the transistor M_1 contribution is negligible since its impact on phase noise performance is at twice the VCO operating frequency as described in Ali Hajimiri et al (1999).

The VCO phase noise characteristic is plotted by progressively increasing these jitter sensitive device dimensions of M_2-M_7 within the derived permissible range (2.29). The phase noise characteristic is obtained for the two extreme sets of dimensions defined in the constraint of (2.29) and another device dimension set chosen within the range defined by the constraint. The simulation settings used for plotting VCO phase noise characteristics is shown in Figure 3.1. Appropriate control voltage for an operating frequency of 2100MHz is fed as input to the bias generator. The phase noise characteristic of VCO output V_{out} is plotted using PNoise simulation in Cadence, and the obtained characteristic is shown in Figure 3.2.

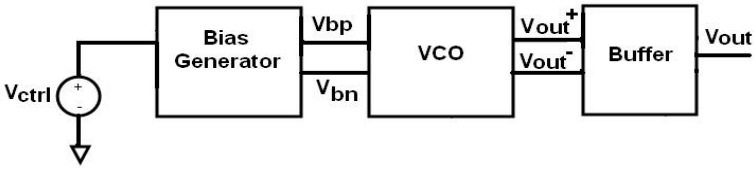

Figure 3.1 Simulation Settings for Obtaining VCO Phase Noise Characteristic

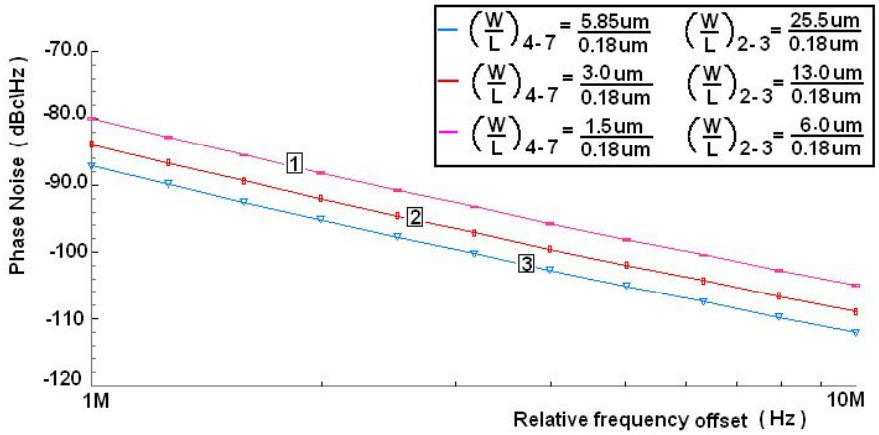

Figure 3.2 VCO Phase Noise Plot at 2100MHz Frequency

The noise PSD plots show improvement with increase in device dimensions. This obeys the fact that the resistance of the switch transistors

and symmetric load transistors reduces with increase in device dimensions, and hence is the improvement in the noise PSD characteristics. Having discussed the VCO noise PSD characteristic, the charge pump design and its noise PSD characteristics are described below.

3.2.2 Design of Charge Pump Circuit for Minimum Jitter

Similar to the scenario in VCO, the jitter sensitive devices in charge pump are the current source transistors M_7-M_{14} and the switch transistors M_3-M_6 of the charge pump circuit shown in Figure 2.3b. The output noise current PSD of charge pump circuit is obtained for the device dimensions that are related to the device dimensions used for characterizing the phase noise of the VCO circuit. In this case it is the extreme device dimension defined by the constraint (3.14) and another dimension within the constraint defined in (2.30).

The simulation settings used for characterizing the output noise current PSD of charge pump circuit is shown in Figure 3.3. Appropriate bias voltage V_{bn} required for VCO frequency of 2100MHz is used in this setting to bias the charge pump circuit. The input of charge pump circuit was driven by a PFD with two in-phase clock sources of frequency 131.25MHz to emulate the phase lock condition obtained with a divider value of 16. The simulation settings thus include PFD noise sources also. The output of charge pump is connected to a DC voltage source by means of a current probe. The value of the DC voltage is chosen to be the control voltage that corresponds to the VCO frequency of 2100 MHz.

From the current measured using the current probe i_{probe}, the noise current PSD is plotted using PNoise simulation in Cadence. The noise PSD

plots obtained are shown in Figure 3.4. From the noise PSD plots it can be observed that the lowest noise PSD characteristic corresponds to the lowest device dimensions from the feasible device dimension set. Since these minimum dimensions set the current source transistors $M_{7\text{-}14}$ with minimum transconductance g_m, the output noise current PSD is the smallest.

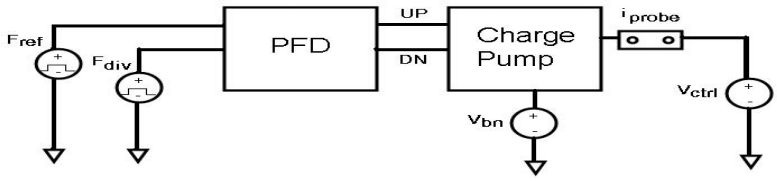

Figure 3.3 Simulation Settings for Obtaining Charge Pump Output Noise Characteristic

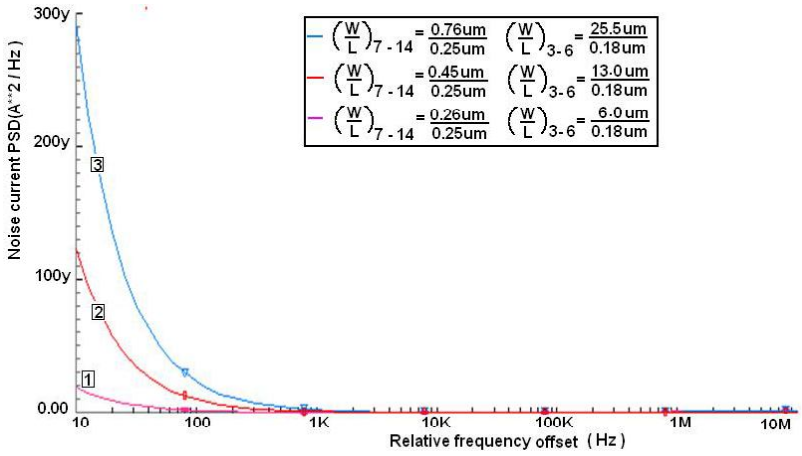

Figure 3.4 Output Noise Current PSD of Charge Pump Circuit

3.2.3 Choice of Device Dimensions for Overall Minimum Jitter

Since the device dimensions of VCO and charge pump are related, for every noise PSD plot of VCO in Figure 3.3 there is a related noise PSD characteristic of charge pump shown in Figure 3.6 which are labeled similarly as 1,2 and 3. As discussed earlier, choosing one of the noise PSD plot will fix

the device dimensions in both the circuits. The noise PSD characteristic is thus chosen by determining output jitter from the PLL designed with these three sets of device dimension pertaining to the plots labeled 1,2 and 3 in both Figure 3.2 and Figure 3.4 .

The peak to peak jitter is measured from the eye diagram plotted from the output clock of the PLL designed with these three device dimension which is shown in Figure 3.5. Since the buffer used with VCO in the PLL is an ideal buffer, finite rise and fall time is not observed in the plotted eye diagram. An ideal buffer is intentionally chosen in this simulation setting since this exercise also targets in identifying the dominant noise contributor to output jitter between the VCO and charge pump functional blocks.

The computed jitter from the eye diagram for the three device dimension sets are tabulated in Table 3.1. The tabulation shows that the minimum jitter obtained pertains to the noise PSD plot labelled1. This set corresponds to the minimum output noise current PSD from charge pump and the worst case noise PSD of VCO. This set is chosen for design in the traditional self biased PLL which is considered as the reference system and is subjected to modifications for further improvement in its performance which will be discussed in the subsequent chapters.

This simulation exercise also judges the predominant noise contributor functional block in the PLL, which in this case is the charge pump circuit. This is in agreement with the fact that the PLL loop bandwidth if chosen as wide as possible, the charge pump noise sources becomes the predominant noise sources when compared with the VCO noise sources as concluded in Van de Beek et al (2004).

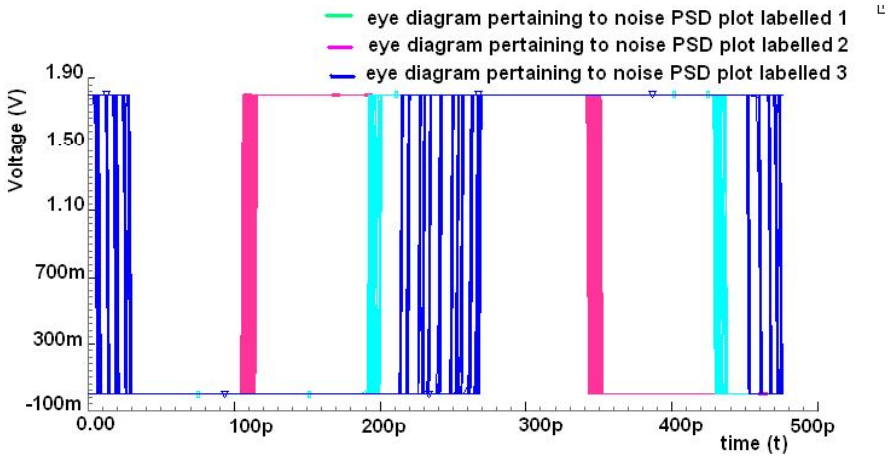

Figure 3.5 Eye Diagram Plot of Output Clock

Table 3.1 Overall Jitter for Different Choices of Device Dimension Combinations

VCO Device Dimensions		Charge Pump Device Dimensions		Label of noise PSD Plot	Peak to Peak Jitter Measure (ps)
Load Transistor $(W/L)_{4-7}$	Switch Transistor $(W/L)_{2-3}$	Load Transistor $(W/L)_{7-14}$	Switch Transistor $(W/L)_{3-6}$		
1.5µm/ 0.18µm	6µm/ 0.18µm	0.3µm/ 0.25µm	6µm/ 0.18µm	1	8.7
3.0µm/ 0.18µm	13µm/ 0.18µm	0.5µm/ 0.25µm	13µm/ 0.18µm	2	10.9
6.0µm/ 0.18µm	26µm/ 0.18µm	0.76µm/ 0.25µm	26µm/ 0.18µm	3	54

Having discussed the design of the functional blocks for minimum random noise contribution, the following is the discussion on the impact of systematic noise on jitter performance.

3.3 IMPACT OF SYSTEMATIC NOISE ON PLL PHASE NOISE

The imperfections in charge pump circuit leads to periodic disturbance in control voltage. The imperfections namely current mismatch in UP and DN current, difference in rise and fall time of UP and DN signals,

delay differences in controlling UP and DN switches, these imperfections lead to current pulses at the output of charge pump even under phase locked condition. In this scenario of phase locked condition, the average current drawn from charge pump is made zero by the PLL. Hence the output of the charge pump appears with UP and DN current pulses with asymmetric pulse width such that its average current becomes zero and these pulses appears periodically at reference frequency and introduces spur at the PLL output. Approximating the resultant control voltage, as ripples of train of pulses as shown in Figure 3.6, the impact of the systematic noise on the output phase noise is analyzed as described in Noorfazila Kamal et al(2012).

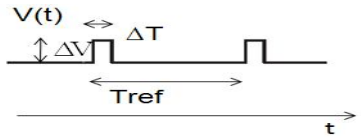

Figure 3.6 Control Voltage Ripple

The control voltage $V_{ctrl}(t)$ being periodic with period T_{ref}, amplitude ΔV and width ΔT can be expressed by its Fourier series representation and the representation is given as below

$$V_{ctrl}(t)= V_t' + \frac{\Delta V \Delta T}{T_{ref}} + \frac{2\Delta V}{T_{ref}\omega_{ref}} \sum_{k\neq 0} \frac{\sin(k\omega_{ref}\Delta T)\exp(jk\omega_{ref}t)}{k} \quad (3.15)$$

Here $V_t' + \frac{\Delta V \Delta T}{T_{ref}}$ represents the DC offset voltage of $V_{ctrl}(t)$.

The resultant VCO frequency ω_{VCO} is given by the following expression

$$\omega_{vco} = K_{vco}V_t' + K_{vco}\frac{\Delta V \Delta T}{T_{ref}} + K_{vco}\cdot\frac{2\Delta V}{T_{ref}\omega_{ref}} \sum_{k\neq 0} \frac{\sin(k\omega_{ref}\Delta T)\exp(jk\omega_{ref}t)}{k} \quad (3.16)$$

As ΔV appears very small, the effect of this ripple voltage appears very similar to narrow band Frequency Modulation. Its modulation index β can be expressed as

$$\beta = \frac{K_{vco}\Delta V}{\omega_{ref}} \tag{3.17}$$

The system parameters involved in β are K_{VCO} and the ripple magnitude ΔV. These parameters if minimized can reduce the impact of this systematic noise on the resulting spur at the output. The present work thus attempts to reduce K_{VCO} by incorporating a dual loop PLL which is described in chapter 4. The ripple magnitude ΔV is minimized in the present work by modifying single ended control voltage of traditional self biased PLL to differential self biased PLL.

The above discussions dealt with minimizing the noise PSD considering random and systematic noise of the functional blocks. Noise transfer functions can also be altered to minimize the PLL output phase noise. The impact of NTFs on jitter performance and a suitable modification in the NTF is discussed below.

3.4 ANALYSIS OF NTFS ON JITTER PERFORMANCE

Considering the NTFs expressed in (3.2)-(3.5), a careful analysis of all the dependencies leads to the following set of assumptions/observations which can aid in suitable modification of the reference, traditional self biased PLL for further improvement in jitter performance.

(i) Since the original PLL is wideband, it is observed that the dominant contributor to the overall jitter is the noise originating from the charge pump.

(ii) A reduction in K_{VCO} leads to a reduction in the charge pump contribution to overall jitter as observed in Akihide Sai et al (2012).

(iii) While reducing K_{VCO}, due consideration must be given to the fact that other factors that are related to it through the PLL loop equations could mitigate the possible improvement in jitter.

(iv) One possibility for reducing jitter is to reduce K_{VCO} without altering the denominators in (3.4), and this can be accomplished with a corresponding increase in I_{cp}. This approach is followed in Robert Nonis et al (2005). On the other hand, the work reported in Mark Ferriss et al (2013) notes this approach as that "..there are practical difficulties which should be kept in mind when employing this strategy in multipath PLLs". After considering the systematic noise sources like capacitor leakage and charge pump mismatch currents, it is concluded in Mark Ferriss et al (2013) that K_{VCO} cannot be reduced below a certain limit by following this approach.

(v) Alternatively, one can reduce K_{VCO} and also alter the denominator in Equation (3.4), which in turn would imply that the system would operate with altered loop parameter values of ω_n and ζ. In return for a reduction in overall jitter, these loop parameters can be altered to the extent that the conditions of PLL loop stability and lock time are not degraded significantly. This is the approach followed in the present work in its modification in the reference PLL and is iteratively

designed through simulation so that the reduced jitter does not degrades settling time performance. This approach of jitter reduction will be discussed in the following chapter.

While considering the reduction of K_{VCO}, one cannot reduce K_{VCO} without compromising capture range and settling time of the traditional self biased PLL. Hence the present work employs a dual loop scheme that allows one to reduce K_{VCO} without any trade off with capture range and settling time. The brief principle based on which the reference PLL is modified into a dual loop scheme to reduce K_{VCO} is discussed in the following chapter.

As another alternative, the architecture of the second order PLL is modified to a third order PLL that settles faster with large phase margin thus can show improvement in jitter performance. These modifications on the traditional self biased PLL and their results are summarized in Chapter 5.

3.5 SUMMARY

Optimization of the nominal traditional self biased PLL considered as a reference system for jitter performance was illustrated in this chapter. Optimization of jitter was studied through functional block noise transfer functions and their noise source PSDs. The procedure by which the impact of noise PSDs on ouput jitter was reduced, was discussed. The sources of systematic noise from charge pump circuits were explained. The possible alterations in the system that reduce the effect of these systematic noise sources were discussed and the respective alterations made in the self biased system are discussed in the subsequent chapters.