CHAPTER 2

SELF BIASED ADAPTIVE BANDWIDTH PLL

This chapter illustrates the system functionality of the traditional self biased PLL proposed by John Maneatis (1996), its salient features and the design aspects of its functional blocks. This self biased PLL is realized in the present work by following the guidelines described for the traditional self biased PLL and is considered as a reference PLL for analysis and further modifications. The design procedure adopted while realizing this self biased PLL is explained in this chapter. Though the design procedure is well established in literature, the emphasis in this chapter is on those aspects that are either less reported or not explicitly reported in literature.

2.1 TRADITIONAL SELF BIASED PLL FUNCTIONAL DESCRIPTION

The traditional self biased PLL is a charge pump based integer N PLL that generates a multiplied clock that is synchronous with the reference clock. The functional blocks of this PLL comprises of Phase Frequency Detector (PFD), Charge Pump (CP_1) and , Loop Filter (LF) comprising of capacitor C and resistor R derived from charge pump CP_2, bias generator, VCO and a divider as shown in Figure 2.1.

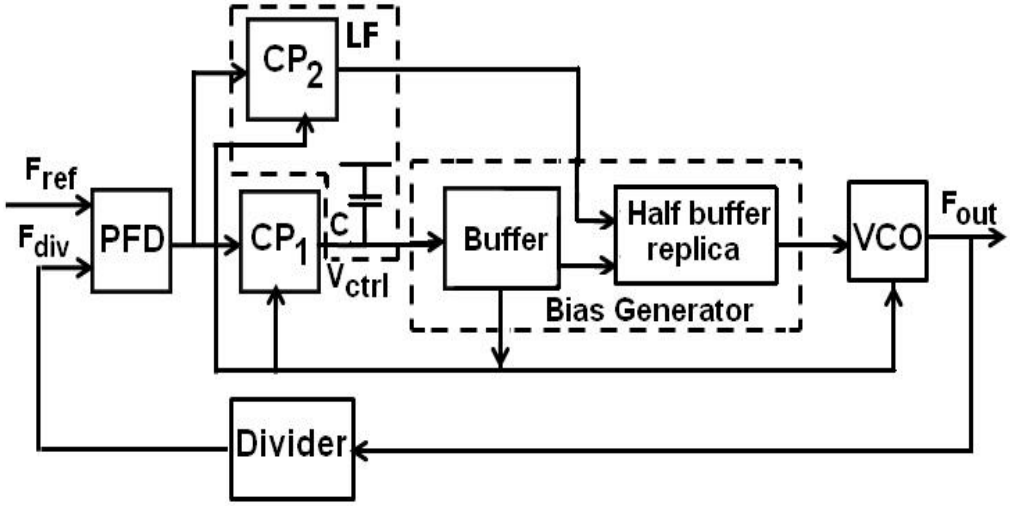

Figure 2.1 Functional block diagram of traditional self biased PLL

The PFD compares the reference clock F_{ref} and the divided version of the output clock F_{div}, and generates a train of rectangular voltage pulses with variable pulse width in proportion to the phase/frequency error. Proportional to these voltage pulses, the charge pump block CP_1 generates current pulses. These current pulses are integrated by a first order loop filter LF consisting of series connected capacitor C and a resistance. The resistance of the loop filter in traditional self biased PLL is derived from the charge pump block CP_2. This filter is a trans-impedance block that generates a control voltage V_{ctrl} integrated from the current pulses. This control voltage then drives the VCO through a bias generator. The VCO incorporated in this design is a symmetric load ring oscillator. The necessary bias voltages required for the oscillator are provided by the bias generator based on the control voltage V_{ctrl}. The output clock signal F_{out} generated by VCO is then divided by a factor N by the divider block to generate F_{div}. This divided clock signal F_{div} is then compared with F_{ref} in PFD to determine the phase/frequency errors. Under steady state operation, the system aligns this divided output clock with the reference clock reducing phase and frequency errors to zero.

The system then generates an output clock with a frequency N times that of the reference clock. Having completed the system level description, the block and circuit level descriptions are taken up in following section.

2.2 PLL SUB BLOCK DESCRIPTION

Functional description of the sub blocks that constitutes the traditional self biased PLL is explained in the following subsections. The design aspects of the individual blocks and its transfer functions are also derived in the respective sections. The circuit schematic of PFD used in the traditional self biased PLL of the present work deviates from that employed in traditional self biased PLL whereas the circuit schematic of all other functional block circuits are retained as proposed in traditional self biased PLL.

2.2.1 Description of PFD and charge pump

The PFD employed in the traditional self biased PLL is the tristate PFD. The circuit realization of this PFD used in the present work is shown in Figure 2.2. The two positive latches used in this PFD are designed using True Single Phase Clocked (TSPC) architecture. The reference clock F_{ref} and VCO divided clock F_{div} are used as clock signals in the first and second P-latch respectively. The *Reset* signal generated using NOR logic is used as data signal in the two latches. With the external system reset, *Reset_system*, the initial state of the reset signal generated by the NOR logic is low. The P-latch is transparent to the reset signal during the high phase of F_{ref} and F_{div} , hence with the rising edge of F_{ref} and F_{div}, the outputs $\overline{UP}$ and $\overline{DN}$ transit from high to low, and the NOR logic resets these two signals to high after a delay determined by the propagation delay of the NOR logic. Using these $\overline{UP}$ and

$\overline{DN}$ signals, their respective non inverting versions UP and DN are generated. The signals and their complementary versions are generated with matched delays. These UP and DN signals generated from PFD then drives the charge pump circuit. The architecture and operation of the charge pump circuit is explained next.

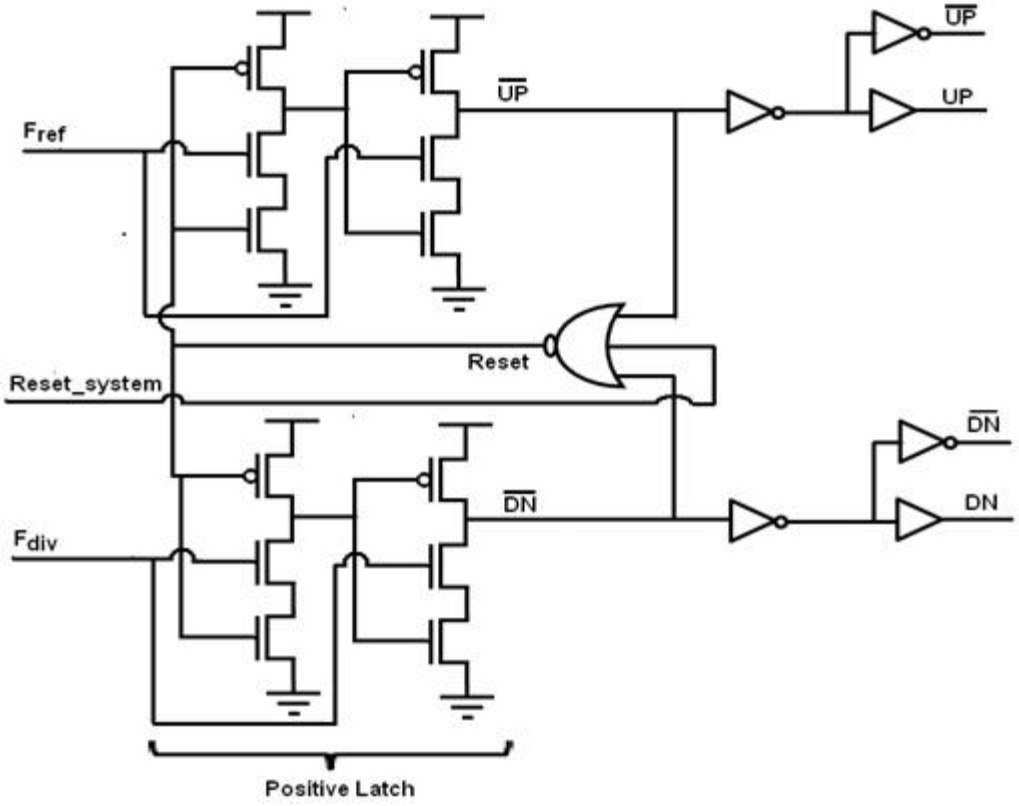

Figure 2.2 Circuit schematic of Tristate PFD

Architecture of charge pump circuit is shown in Figure 2.3a. The transistors M_3, M_4, M_5 and M_6 in this charge pump circuit act as on-off switches controlled by UP and DN signals. The transistors M_2 and M_1 define the required bias current in the circuit. The transistors $M_{7\text{-}14}$ behave as switched current sources dependent on the state of the UP and DN control signals.

Under phase lock condition, the possible state of the UP and DN signals are both either high or low, and, in either condition, ideally, the net charge delivered to the loop filter remains zero. When both UP and DN are in the low state, M_5 and M_4 being off, the output node which is marked as V_{ctrl} remains in high impedance state. The entire current defined by the tail transistors M_1 and M_2 steer in to the stages constituted by M_2, M_6, $M_{13,14}$ and M_1, M_3, $M_{7,8}$ respectively. This redundant stage helps in minimizing the charge sharing effect due to high impedance state of the output node. With the other condition on the PFD signal with both UP and DN being high, the current controlled by UP and DN switches will be equal, hence no current is delivered from the output of the charge pump circuit.

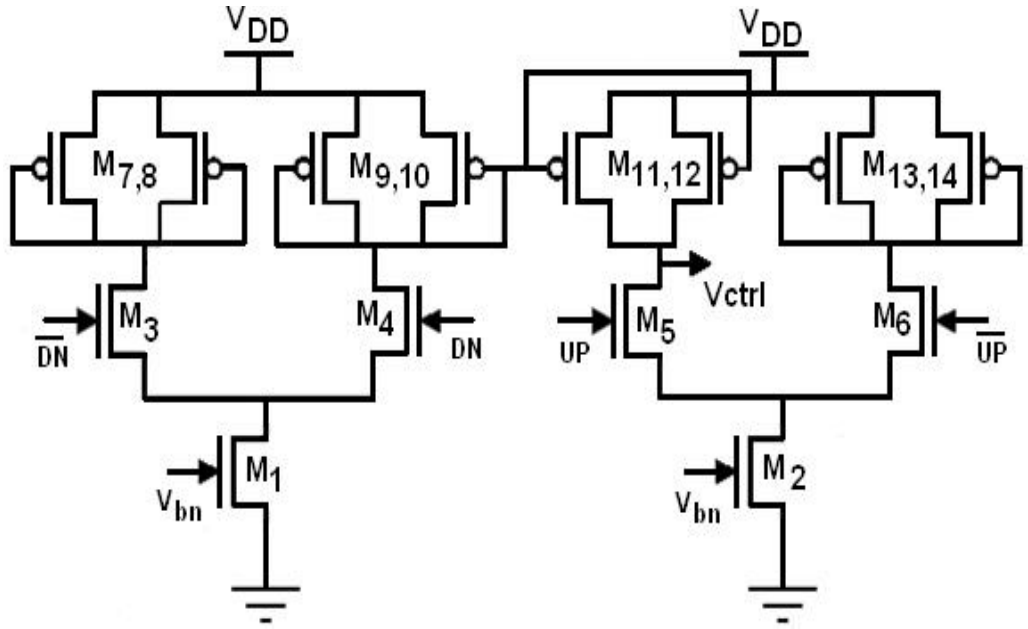

Figure 2.3 a. Charge pump circuit schematic

For very small phase errors, the circuits operate linearly and the gain of the circuit is expressed as follows. With the bias current of the charge pump denoted by I_{cp} which is the tail current defined in M_1 and M_2, the

average current I_{avg} delivered at the output of the charge pump for a phase error of θ_e is given by

$$I_{avg} = I_{cp}\frac{\theta_e}{2\pi} \tag{2.1}$$

Using this relation, the gain K_{PD} of the PFD and charge pump circuit which is the ratio of output average charge pump current to the phase error is given by

$$K_{PD} = \frac{I_{avg}}{\theta_e} = \frac{I_{cp}}{2\pi} \tag{2.2}$$

The transfer characteristic of this PFD with very small phase deviations under locked condition is linear, and the gain is found to be constant as given in Equation (2.2).

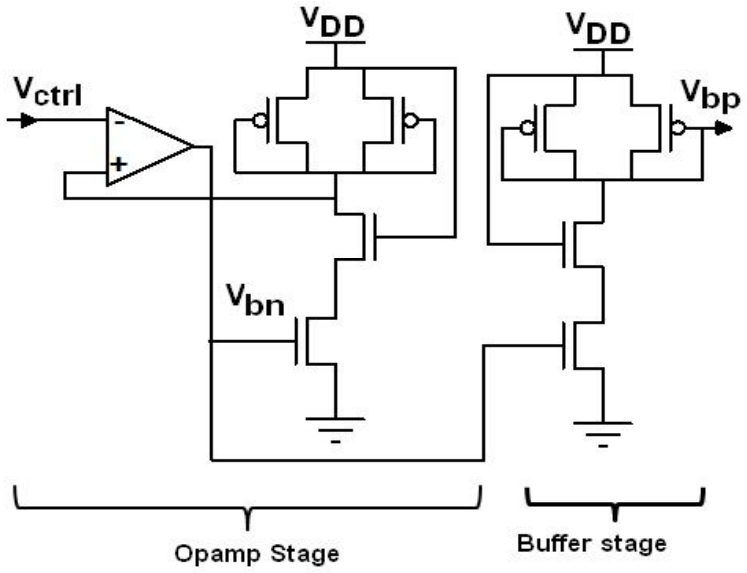

Figure 2.3b Bias Generator circuit schematic

The bias generator circuit shown in Figure 2.3b defines the bias current based on the control voltage V_{ctrl} by generating V_{bn}. This develops a condition that allows the bias current to vary with the operating frequency, and this nature enables the traditional self biased PLL to possess one of its salient features, the adaptive bandwidth characteristic (to be described in the subsequent sections).

2.2.2 Description of Loop Filter

The loop filter is a transimpedance section that consists of a first order series connected resistor R and capacitor C. The transfer function F(s) of the loop filter is given by

$$F(s) = \frac{sRC+1}{sC} \tag{2.3}$$

F(s) defines a pole at zero, and a zero at a frequency of 1/RC that defines the band width of the filter.

By design, the bandwidth of this loop filter in the self biased PLL architecture is made to track the reference frequency. The resistance R of the loop filter is therefore derived from charge pump CP_2 as shown in Figure 2.4, the bias current of which is derived from control voltage by means of the bias generator shown in Figure 2.3b. The principle by which the resistance is derived using CP_2 and bias generator is explained next.

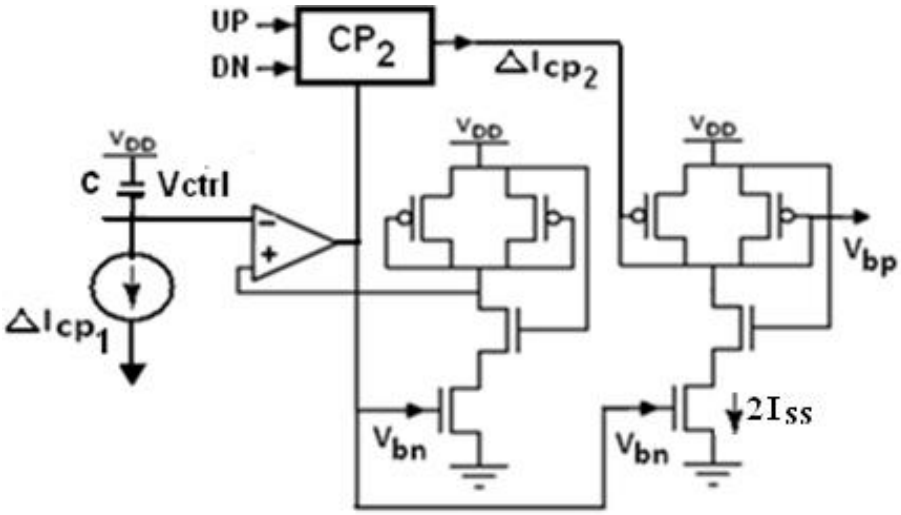

Figure 2.4a Circuit schematic of loop filter

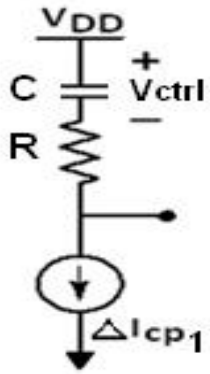

Figure 2.4b Conventional First order Loop filter

The bias generator circuit comprises of an opamp stage and a buffer stage. The voltage V_{ctrl} developed across the capacitor is buffered by the opamp stage of the bias generator. About this buffered V_{ctrl} in the buffer stage of the bias generator, the charge pump CP_2 develops an incremental voltage to generate the voltage V_{bp}. This incremental voltage developed by CP_2 is through its incremental current ΔI_{cp2} generated in proportional to the phase error sensed by it and this current is added with the bias current generated in the second buffer stage to develop V_{bp} at its symmetric load as output. The

ratio of the incremental voltage thus generated to the incremental current ΔI_{cp2} defines the resistance R of the loop filter, and in this case it is defined by the transconductance g_m of the diode connected load in the second buffer stage.

Deriving the resistor in this manner maintains the voltage developed across it to be the same as the voltage across the resistance R in the conventional loop filter shown in Figure 2.4b, as given by

$$\Delta I_{cp1} R = \Delta I_{cp2}.(1/2.g_m) \tag{2.4}$$

From the above relation, R can then be expressed as

$$R = \frac{\Delta I_{cp2}}{\Delta I_{cp1}}.\ (1/2.g_m)$$

$$= \frac{y}{2.\sqrt{2.k.2Iss}} \tag{2.5}$$

Here *y* is the ratio of current defined in the charge pump CP_1 that gets integrated by the capacitor (this charge pump is termed as integral charge pump in the traditional self biased PLL) to the current defined in the charge pump CP_2 that develops an incremental voltage proportional to instantaneous phase error (this charge pump is termed as proportional charge pump in the traditional self biased PLL).

The resistance expressed in Equation (2.5) is thus a function of buffer bias current I_{ss} that varies with V_{ctrl} and hence adapts to ω_{ref}.

2.2.3 Description of Self biased VCO

The VCO employed in the present work is a self biased ring oscillator with four delay elements as shown in Figure 2.5. The period of oscillation of this VCO is given by

$$T = 8t_p \tag{2.6}$$

Here t_p is the propagation delay contributed by the individual delay element.

The instantaneous change in phase θ_{out} of the VCO signal is given by

$$\theta_{out} = \int \Delta\omega_{out}\, dt$$

$$= K_{VCO} \int \Delta V_{ctrl}\, dt \tag{2.9}$$

In the above equation, the constant K_{VCO} represents the gain of VCO. With this linear representation in θ_{out} , its Laplace representation is given by

$$\theta_{out}(s) = \frac{K_{VCO}}{s} \Delta V_{ctrl}(s) \tag{2.10}$$

From the above relation, VCO transfer function $H_{VCO}(s)$ is given by

$$H_{VCO}(s) = \frac{K_{VCO}}{s} \tag{2.11}$$

The circuit schematic of the self biased VCO along with its delay element is shown in Figure 2.5. The transistors M_2, M_3 of the delay element acts as on and off switches. The load resistance of the delay element is the

symmetric load resistance contributed by transistors M_4-M_7. This resistance possesses symmetric voltage swing characteristic at its output node. The lower limit of the symmetric swing is the control voltage. This condition is ensured by the bias generator. The symmetric load resistance and its typical V-I characteristic is shown in Figure 2.6. Here x axis represents the typical value of voltage across the delay element and y axis represents the sum of the drain current in the two transistor $M_{4,5}$ or $M_{6,7}$ that constitutes symmetric load. The resistance contributed by the symmetric load is the average resistance

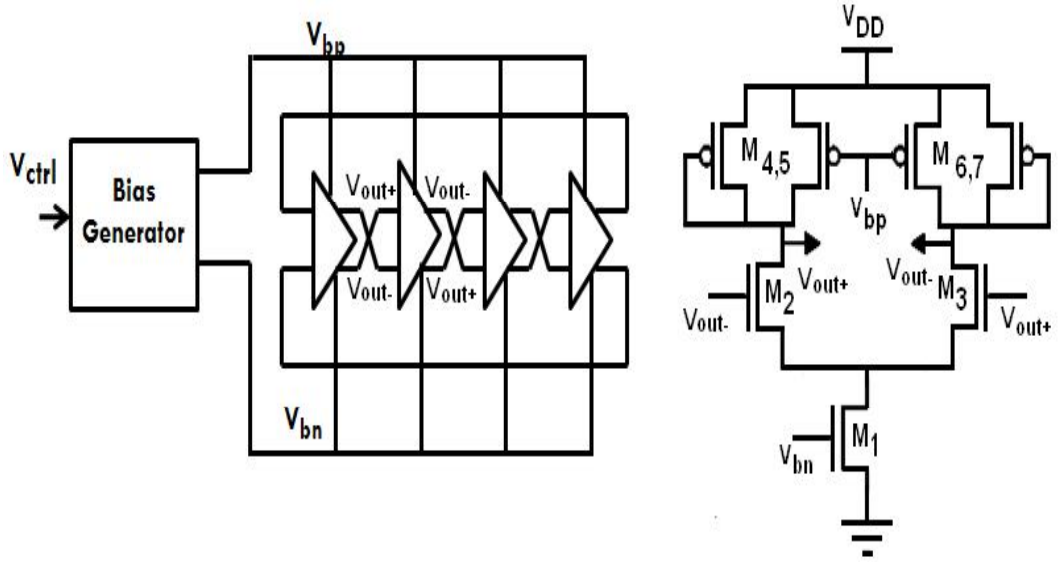

Figure 2.5 Circuit Schematic of Ring Oscillator Based VCO and its Delay Element

obtained from its V I characteristic as shown by the dotted line in the characteristic.This average resistance R_{on} is obtained from the transconductance g_m of M_4 or M_7 and is given by

$$R_{on}=1/g_m=1/k.(V_{ctrl}-V_{T0})=1/\sqrt{2.k.I_{ss}} \quad (2.12)$$

In the above equation *k* stands for the device transconductance of M_4 or M_7. As the bias voltages vary depending on V_{ctrl}, proportionally the

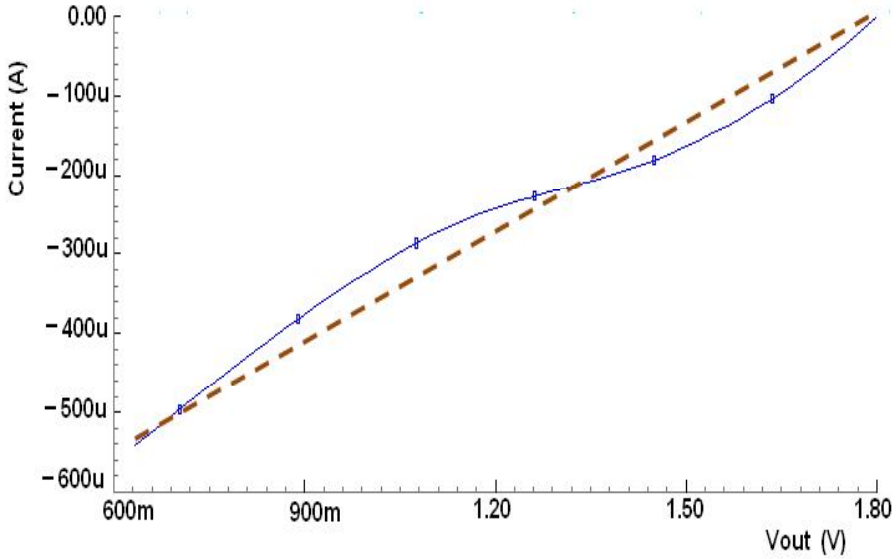

Figure 2.6 V I characteristic of symmetric load resistance

symmetric load resistance R_{on} varies and changes the operating frequency linearly.

Let C_B be the total capacitance at the output node of the delay element. Knowing R_{on} and C_B of the delay element, its propagation delay can be determined and hence the frequency of operation of the ring oscillator which is expressed as below.

$$f_{out} = \frac{1}{2.n.R_{on}.C_B} . \qquad (2.13)$$

Here *n* stands for the number of delay element stages in the ring oscillator. Using the expression for R_{on} from Equation (2.12) in Equation (2.13), f_{out} of the traditional self biased PLL is expressed as below

$$f_{out} = \frac{k.(V_{ctrl}-V_{TO})}{C_{eff}}. \qquad (2.14)$$

Here C_{eff} represents the effective capacitance derived from the oscillator and is given by

$$C_{eff} = 2.n.C_B. \quad (2.15)$$

In the above equation C_B represents the total capacitance at the output of the delay element.

The resistance in this architecture varies linearly with control voltage, hence K_{VCO} is maintained constant over the entire operating frequency range of the traditional self biased PLL. This K_{VCO} is expressed as below

$$K_{VCO} = \frac{df_{out}}{dV_{ctrl}} = \frac{k}{C_{eff}} \quad (2.16)$$

The bias generator provides the bias voltages V_{bn} and V_{bp} to the delay element derived from the control voltage V_{ctrl}. The bias current to the delay element is generated by M_1 transistor through V_{bn}. The same bias generator also biases the charge pump circuit as described earlier. The circuit schematic of the bias generator and its design is described next.

2.2.4 Description of Bias Generator

Bias generator employed in the traditional self biased PLL consists of four stages comprising of an amplifier stage, two replica buffer stages, and a bias circuit stage for amplifier. The amplifier stage and the first half buffer replica stage constitute an opamp stage. The circuit schematic of the bias generator is shown in Figure 2.7.

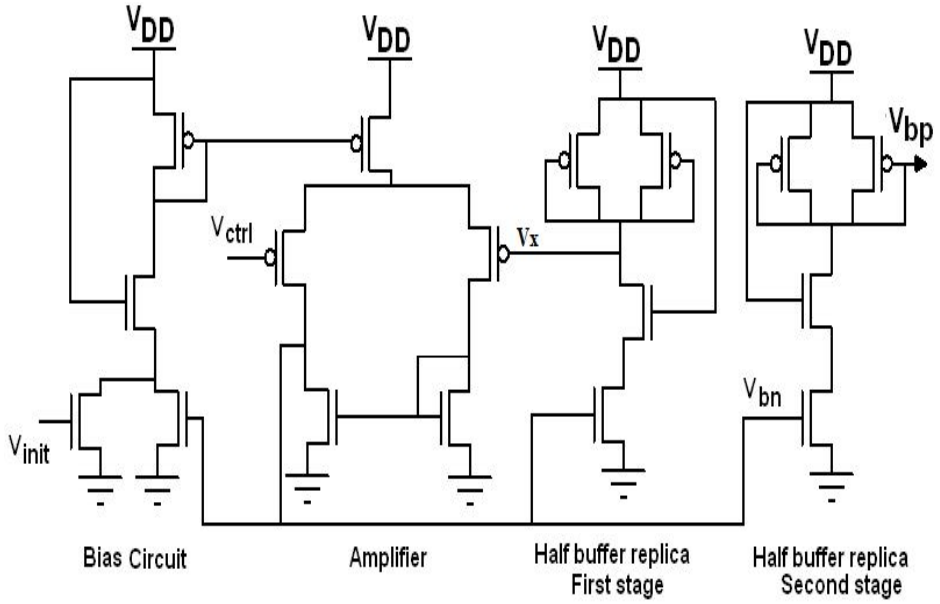

Figure 2.7 Circuit Schematic of Bias Generator

In the bias generator, the opamp adjusts the voltage V_{bn} and hence maintains the virtual node voltage V_x as V_{ctrl} . This V_{bn} controls the second buffer stage which is a replica of the first buffer stage and thus its output voltage V_{bp} is V_{ctrl} itself. The replica buffer stage is the replica of one half of the delay element and charge pump circuit. The V_{bn} that controls the current generated in the amplifier stage also controls the current in delay element and charge pump circuit. Thus the resulting voltage at the output of these circuits are also V_{ctrl}. This feature brings in three significant attributes of the traditional self biased PLL as explained below.

The first significant feature is that in delay element it ensures its load to be a symmetric load. The characteristic of this symmetrical load is that, its incremental resistance is equal at its differential output node. The delay elements thus present superior dynamic supply rejection characteristic. Moreover the bias generator also maintains its bias current fixed with static supply variation and hence aids the delay element to possess the second

significant feature of static supply rejection characteristic similar to that obtained from a cascode current source.

This replica in charge pump introduces the third feature that aids to minimize the static mismatch current by ensuring equal UP and DN current. This minimization is attained since the gate voltage settles to the output drain voltage (of M_{11} and M_{12} in Figure 2.3a) V_{ctrl}, thus makes the mirrored current controlled by DN voltage to be equal to the current (of M_5 in Figure 2.5a) controlled by UP voltage.

This bias generator is self biased, therefore a pulse (V_{init}) is used to start the self bias circuit and biases it to operate from its operating point even after the pulse is switched off.

2.2.5 Design description of Prescalar

The divider used in the prescalar is a ripple counter that uses four stages of True Single Phased Clock TSPC register to implement a division of output clock by the factor N equal to sixteen. The inverting stages in TSPC were appropriately ratioed to minimize glitches. Setup time and hold time issues of the flip-flop were taken care. The architecture of the ripple counter to realize clock divider is shown in Figure 2.8a and the circuit schematic of the negative edge triggered flip-flop is shown in Figure 2.8b.

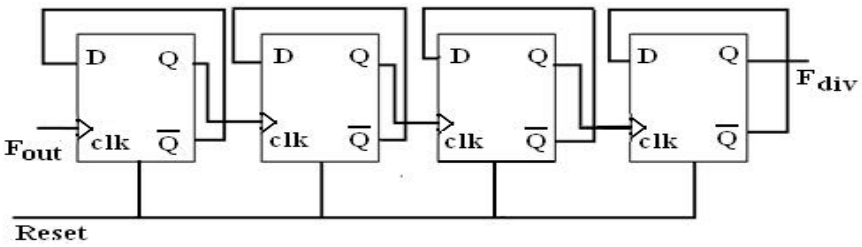

Figure 2.8a Functional block diagram of divider

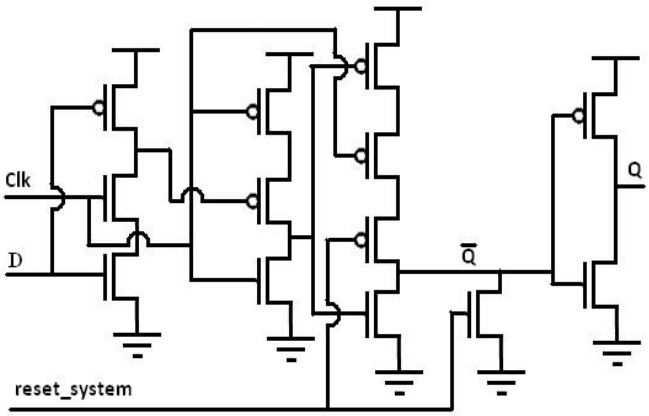

Figure 2.8b Circuit schematic of TSPC flip-flop

2.3 DESCRIPTION OF LOOP PARAMETERS

The various functional blocks of the self biased PLL possess linear operating characteristic very close to phase lock and under phase lock condition. The loop parameters of the system can thus be analyzed using Laplace Transform. The closed loop transfer function of the PLL can be analyzed using the transfer function of the individual functional block derived from the previous section as shown in the block diagram of Figure 2.9. The closed loop transfer function H(s) of this second order system is expressed below

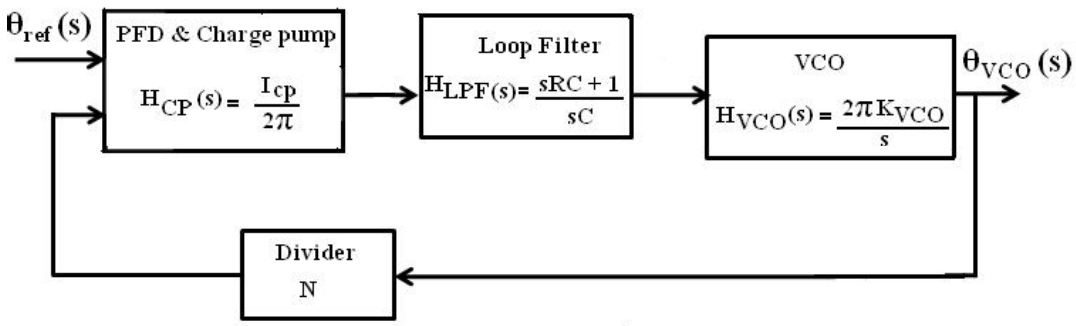

Figure 2.9 PLL block diagram representation

$$H(s) = \frac{I_{cp}.\frac{K_{VCO}}{s}\frac{sRC+1}{sC}}{1+\frac{I_{cp}.K_{VCO}}{N.s}\frac{sRC+1}{sC}}. \quad (2.17)$$

The above equation can be simplified as below.

$$H(s)=N.\frac{\frac{I_{cp}.K_{VCO}.R}{N}.s+\frac{I_{cp}.K_{VCO}}{N.C}}{s^2+\frac{I_{cp}.K_{VCO}.R}{N}.s+\frac{I_{cp}.K_{VCO}}{N.C}} \quad (2.18)$$

This equation can be rewritten in terms of the second order system's natural resonant frequency ω_n and its damping factor ζ.

$$H(s)=N.\frac{2.\zeta\omega_n s+\omega_n^2}{s^2+2.\zeta\omega_n s+\omega_n^2} \quad (2.19)$$

In the above equation ω_n and ζ are defined as given below.

$$\omega_n=\sqrt{\frac{I_{cp}.K_{VCO}}{N.C}} \quad (2.20)$$

$$\zeta=\frac{R}{2}\sqrt{\frac{I_{cp}K_{VCO}C}{N}} \quad (2.21)$$

The loop parameters ω_n and ζ decide loop stability, jitter performance as well as its settling time. In the traditional self biased PLL the resonant frequency ω_n and hence its loop bandwidth ω_{3dB} is made as wide as possible to minimize the input tracking jitter, limited by the PLL's stability since the $\omega_n << \omega_{ref}$ (as a guideline ω_n of the PLL has to be less than one tenth of the ω_{ref}). The ratio I_{cp} to c in Equation 2.20 has to be maximized to make ω_n wide since the factor K_{VCO} is generally set by the desired operating frequency range. Maximizing the ratio I_{cp} to c also permits one to decide the value of ζ

independently as expressed in Equation.2.21, by appropriately selecting the value of R.

The value of ω_n which is set optimal for one frequency may become suboptimal for other operating frequencies. Therefore ω_n is made to vary dynamically with ω_{ref} and the ratio of ω_n to ω_{ref} is maintained constant over the entire operating frequency range. This constant becomes independent of process parameter variation. The loop parameter ω_n is made to track ω_{ref} by making its integral charge pump current biased by control voltage and hence it is in certain ratio with delay element bias current. This ratio is expressed as below.

$$I_{cp1} = x.2I_{ss} \tag{2.22}$$

Using this relation the loop bandwidth to reference frequency ratio is derived and is expressed below.

$$\frac{\omega_n}{\omega_{ref}} = \frac{\sqrt{x.N}}{2\pi}\sqrt{\frac{C_{eff}}{C}} \tag{2.23}$$

The above expression shows ω_n to ω_{ref} ratio dependent on ratio of capacitances and hence the ratio remains constant for the entire linear operating frequency range and the ratio becomes process parameter independent.

The self biased PLL by using its proportional charge pump derives its loop filter resistance that gets adjusted with ω_{ref} and thus maintains ζ a constant independent of process parameters. Using this programmable resistance the expression for ζ is derived and the resultant expression is given below.

$$\zeta = \frac{y}{4}\sqrt{\frac{x}{N}}\sqrt{\frac{C}{C_{eff}}} \tag{2.24}$$

Having described the system functionality and the loop parameters of the traditional self biased PLL, the specifications of system parameters and design procedure of realizing the circuits of the functional subblocks of the traditional self biased PLL are discussed below. The circuits are realized using UMC's 0.18μm CMOS technology.

2.4 DESIGN DETAILS OF A NOMINAL SELF BIASED PLL

The traditional self biased PLL described in the above sections, is realized in the present work, by following the principles proposed by the traditional self biased PLL and hence termed to be a nominal self biased PLL. In the present work this nominally designed PLL is considered as a reference system for investigation and further modification. The loop parameters used in this reference design is described below.

2.4.1 Specifications of Loop Parameters

i. VCO operating frequency range was chosen as 800MHz to 3GHz as per the typical clock frequencies reported by Andrew Allen et al (2009). This along with the bias generator's linear operating range of 0.3V to 1.1V leads to K_{VCO} to be chosen as 3.6GHz/V.

ii. Divider factor N is chosen as 16 based on the choice of reference frequencies reported in Andrew Allen et al (2009). ζ is chosen to be 1 optimized for jitter performance as described by Mozhgan Mansuri et al (2002).

iii. With loop bandwidth chosen to be as wide as possible, the ratio ω_n to ω_{ref} is chosen as 1/15. This choice is made for jitter performance as described by Mozhgan Mansuri et al (2002).

iv. With ω_n to ω_{ref} chosen, and using the expression that defines the ratio ω_n to ω_{ref} as given in Equation (2.23), and by assuming the effective capacitance C_{eff} from the delay element as 240fF, the factor '*x*' that defines the ratio of integral charge pump's bias current I_{cp} to the current I_{ss} defined in the delay element and the loop filter capacitance C value can be decided. A smaller value of C can be chosen by using a very low '*x*' factor. In this case the capacitance value C is chosen as 5pF and with this value '*x*' was computed to be 0.2.

v. Using the expression for ζ given in Equation (2.24), the ratio '*y*' is computed to be 5. This factor thus sets the ratio of proportional charge pump current I_{cp2} to the integral charge pump current I_{cp1} that defines the loop filter resistance R.

Using these system specifications, the circuit functional blocks were designed. The design description of the key functional blocks namely VCO and charge pump are described below.

2.4.2 Design of Bias Generator

In the bias generator, the differential amplifier of the opamp is designed for a common mode voltage of 0.3V to 1.1V. The output of this amplifier drives ten replica stages. The device dimensions of the first and second half buffer replica stages of the bias generator are decided by the

dimensions required in the delay element. The bias generator is designed with a phase margin of 30°(worst case) and unity gain bandwidth of 10MHz (worst case). The frequency response of the bias generator biased for the highest frequency of operation, chosen as 2.7GHz with an input common mode voltage of 0.4V is shown in Figure 2.10. This response shows the bandwidth of bias generator as 10MHz and a phase margin of 86°. Therefore for the entire frequency range of operation the bias generator is stable.

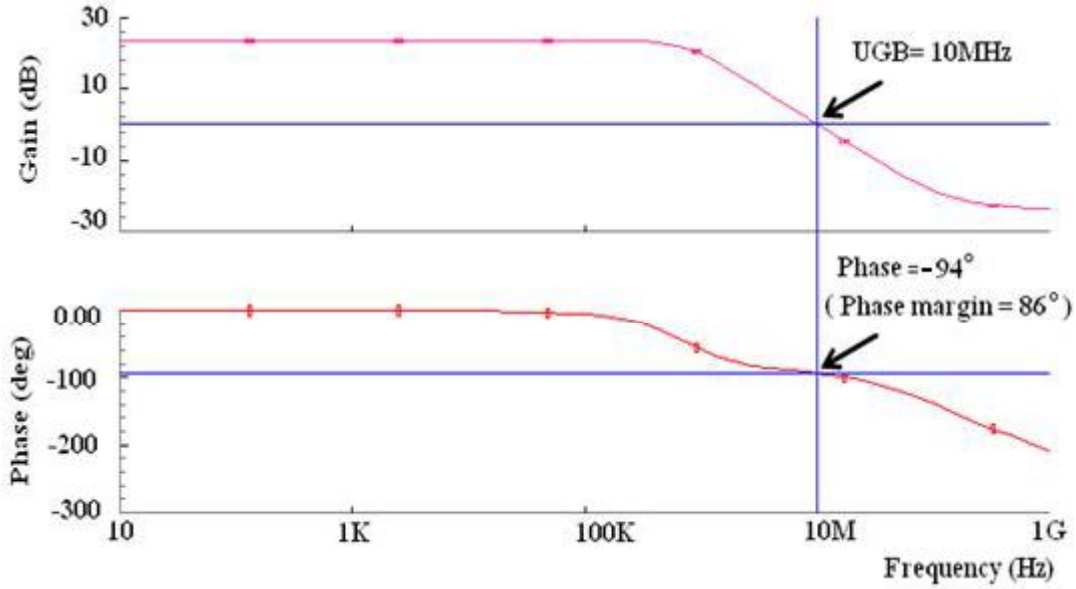

Figure 2.10 Frequency response of Bias generator

2.4.3 Design Description of VCO

The circuit schematic of the delay element employed is shown in Figure 2.5. The procedure with which the delay element is designed satisfying the required operating frequency range and gain, is described below

i. The expression for K_{VCO} derived by John Maneatis (1996) and as given in Equation (2.16) defines the ratio of device dimensions of $M_{4\text{-}7}$ to C_{eff} as given below

$$(W/L)_{M4\text{-}7}/C_{eff} > 4x\ 10^{13} \quad (2.25)$$

ii. With C_{eff} chosen as 248fF, it sets the constraint on dimensions $(W/L)_{M4\text{-}7}$ as given below

$$(W/L)_{M4\text{-}7} > 1.5/0.18 \quad (2.26)$$

Based on chosen C_{eff}, the above constraint defines the device dimensions for $(W/L)_{M2\text{-}3}$ as 6/0.18 since capacitance of $(W/L)_{M4\text{-}7}$ and $(W/L)_{M2\text{-}3}$ together contributes C_{eff}. This dimension also satisfies the gain condition for oscillation as described in Maneatis John (1994) which is given below

$$A > \sec^2(\pi/n) \quad (2.27)$$

With the factor *n* representing the number of delay elements, which in the present design is four, the condition on gain A is given by

$$A > 2 \quad (2.28)$$

The above constraint dictates the lower limit on the possible device dimension values to be used.

iii. The device dimensions of switch transistors $(W/L)_{M2\text{-}3}$ and symmetric load transistors $(W/L)_{M4\text{-}7}$ can be increased while meeting the ratio required to set K_{VCO} value. This inturn increases C_{eff} . Hence increasing the device dimensions beyond a range will affect its highest operating frequency. Thus the upper limit on the possible device dimensions that satisfies the operating frequency range is given by the constraint below

$(W/L)_{M4\text{-}7} < 6/0.18$

$(W/L)_{M2\text{-}3} < 26/0.18$ (2.29)

iv. The permissible values of device dimensions of $(W/L)M_{2\text{-}3}$ and $(W/L)M_{4\text{-}7}$, that satisfies K_{VCO} and operating frequency range are given as below

$1.5/0.18 < (W/L)_{M4\text{-}7} < 6/0.18$

$6/0.18 < (W/L)_{M2\text{-}3} < 26/0.18$ (2.30)

For these range of device dimensions, the VCO gain characteristic is plotted and is shown in Figure 2.11. The gain remains the same for the three plots and for the higher limit in the device dimensions, the highest operating frequency is observed to get limited. Therefore the constraints in Equation (2.30) define the possible choice of device dimensions of the delay element.

v. Device dimension of M1 of the delay element is chosen for the required bias current. At the highest frequency of operation the maximum bias current was computed to be 200μA dependent on the gain and band width value decided in the bias generator. Dependent on this bias current and the respective bias voltage V_{bn}, the device dimension (W/L) of the tail transistor M_1 is computed to be 32/1.

Therefore from the design constraints of Equation (2.30) from the traditional self biased PLL, a permissible range of device dimensions that satisfies the functional specification were derived.

2.4.4 Design of charge pump

The dimensions that are chosen in VCO also defines dimensions in charge pump circuit shown in Figure 2.3a, since the charge pump circuit in the traditional self biased PLL is a replica of the delay element architecture. Therefore for every feasible set of device dimensions in VCO, there is a related device dimension set for the charge pump circuit, which is appropriately scaled by the factor *x* by which the integral charge pump

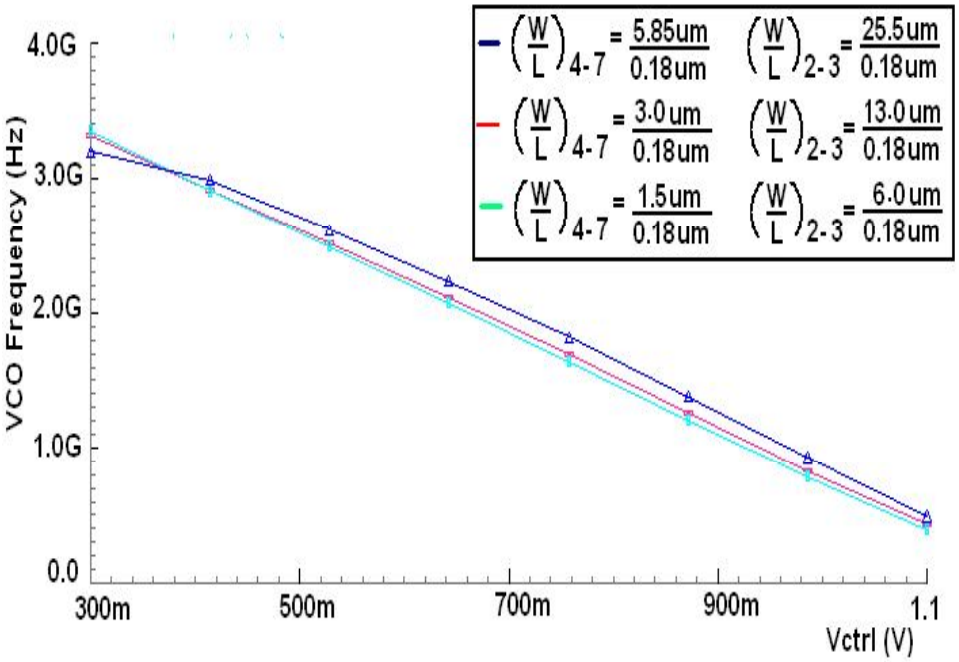

Figure 2.11 VCO Gain Characteristic for the Three Possible Choices of Device Dimensions

current is derived from the delay element bias current. The permissible range of device dimensions of charge pump circuit thus obtained is given below

$$0.3/0.25<(W/L)_{M7\text{-}14} < 0.8/0.25$$

$$6/0.18<(W/L)_{M3\text{-}6} < 26/0.18 \qquad (2.31)$$

Within the permissible range of device dimensions defined for charge pump and VCO, the nominal value of device dimensions is chosen for the design of reference PLL. This nominal value of device dimensions used in the VCO and charge pump circuits of the reference self biased PLL are tabulated below in Table 2.1.

Table 2.1 Nominal Device Dimensions Chosen in Charge Pump and VCO Circuits

Charge pump circuit Transistors	Device Dimensions	VCO Circuit Transistors	Device Dimensions
M_{3-6}	13 μm /0.18 μm	M_{2-3}	13 μm /0.18 μm
M_{7-14}	0.8 μm /0.25 μm	M_{4-7}	3 μm /0.18 μm

Using these device dimensions circuit simulations were carried out using Cadence® Spectre™ simulation. These circuit simulation results are presented in the following section.

2.5 CIRCUIT SIMULATION RESULTS OF REFERENCE PLL

The simulation results of reference PLL based on traditional self biased PLL architecture is presented for a nominal operating frequency of 2.1 GHz in the following sequence. The capture transients of the reference PLL during locking and under locked condition is presented first. Shown following is the measure of peak to peak jitter as obtained from an eye diagram plot of output clock signal.

The capture transients shown in Figure 2.12 depict two features. The first feature is the fast acquisition time in this case it is 110ns for a frequency step of 700MHz from its free running frequency. The second feature is that it exhibits significant capture transients, about 560MHz

frequency deviation from its final frequency of 2.1 GHz. The fast acquisition time is due to the adaptive nature of charge pump current with respect to control voltage that increments/decrements the bias current of charge pump in large step as the frequency/phase error is larger. The large capture transients present is the inherent characteristic of a second order PLL.

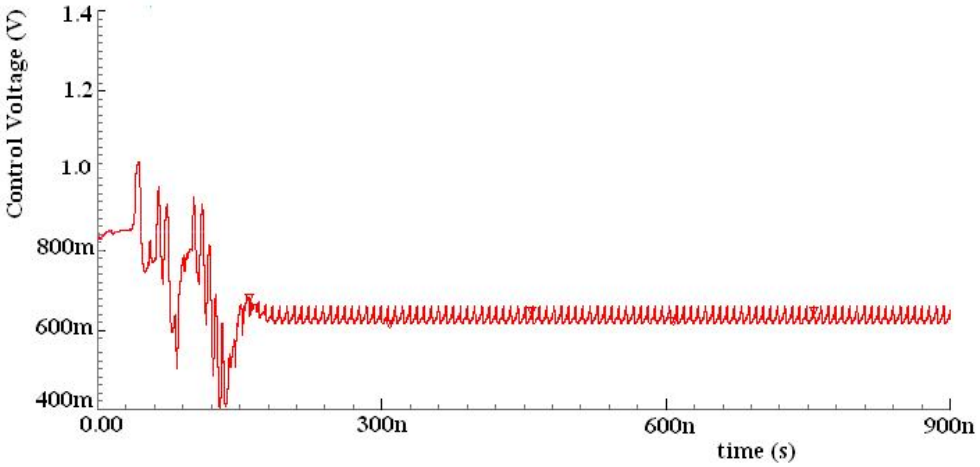

Figure 2.12 Capture Transients of Reference Self Biased PLL at a Nominal Frequency of 2.1 GHz

The Figure 2.13 shows the eye diagram plotted from the output clock signal under locked condition of the reference self biased PLL. The eye diagram measures peak to peak jitter of 12.4ps.

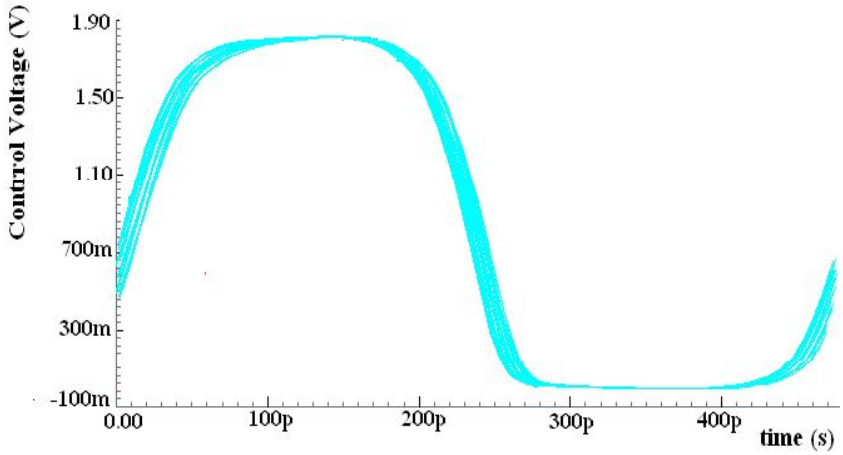

Figure 2.13 Eye Diagram Plot of Reference Self Biased PLL at a Nominal Frequency of 2.1 GHz

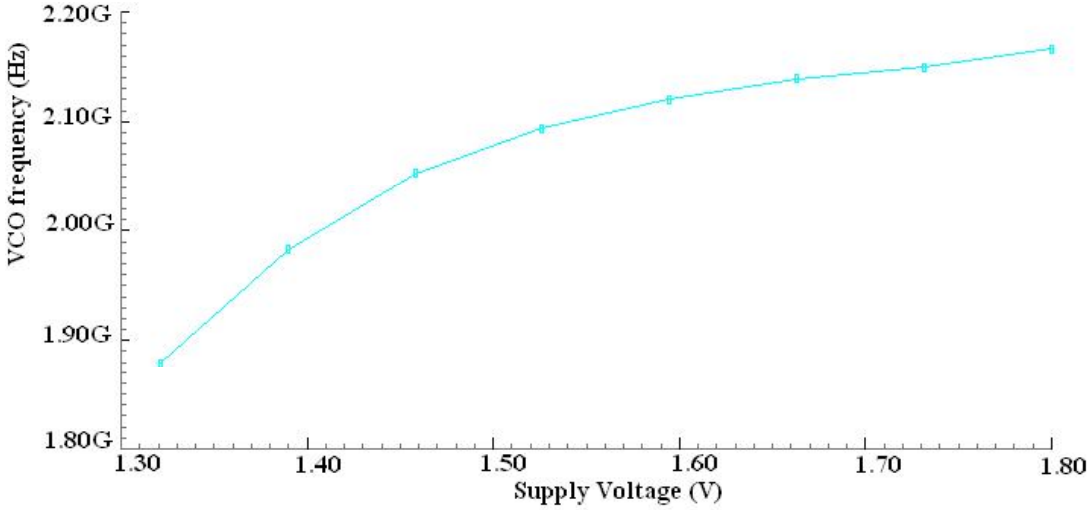

Figure 2.14 Static supply rejection characteristic of VCO

The static and dynamic supply rejection characteristic of the traditional self biased PLL is characterized at the nominal frequency of 2100MHz and is described below. The static supply rejection characteristic is computed by plotting the VCO output frequency for various the DC supply voltages. This characteristic is shown in Figure 2.14 and is observed to show a variation of 21MHz in 100mV variation of supply voltage, with a static supply noise sensitivity of 210MHz/V.

The dynamic supply rejection characteristic of traditional self biased PLL is studied by using a sinusoidal supply source with DC voltage of 1.8V, 10MHz frequency and 10mV peak to peak amplitude. The supply rejection characteristic of the bias generator and the VCO, with V_{bn} remaining static and V_{ctrl}, V_{bp} tracking supply variation is plotted under phase locked condition of PLL and is shown in Figure 2.15. The jitter of the output clock in this simulation was computed using the eye diagram plot. The peak to peak jitter measured, was found to be 33.6ps.

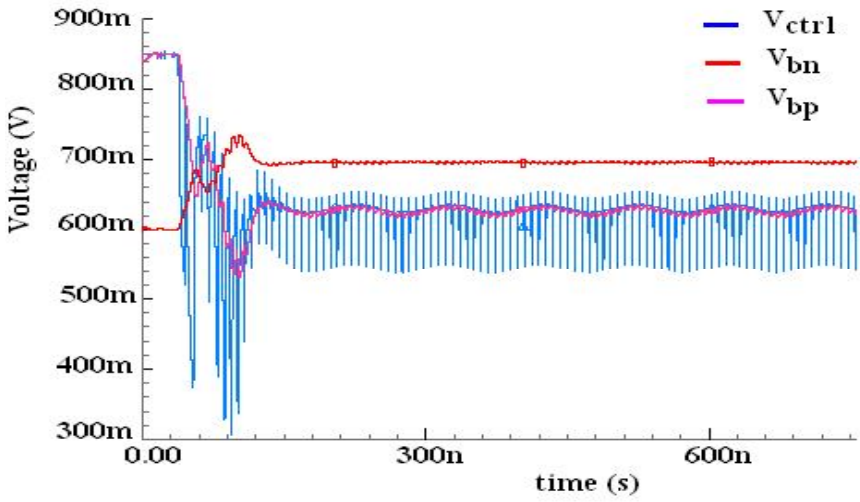

Figure 2.15 Bias voltages showing dynamic supply rejection characteristic

The performance measure obtained from this reference PLL is tabulated in Table 2.2. The settling time measure is obtained for a step frequency of 700MHz. Performance measure shown in this tabulation is used for comparison with the performance measure obtained from the modifications described in the subsequent chapters.

Table 2.2 Performance Measure at a nominal frequency of 2.1GHz

Performance Measure	Settling time (ns)	Undershoot/overshoot magnitude (MHz)	Peak to Peak jitter (ps)	Capture range (MHz)
Values obtained from simulation	110	560	12.4	1000 to 2700

The reference PLL thus designed uses a nominal value of device dimensions defined within the permissible range given by the constraint Equation (2.30) and Equation (2.31). However within this permissible range one can choose

the device dimensions optimally for minimum jitter performance. This optimal choice of device dimensions for jitter optimized performance of the reference self biased PLL was investigated and is described in the next chapter.

2.5 SUMMARY

The present chapter thus described the functionality of the traditional self biased PLL, its subblocks and its system loop parameters. The realization of this self biased system in the present work, by adopting the design guidelines of the traditional self biased PLL was described and its performance measure was benchmarked. Further Optimization of this reference design in the context of jitter minimization is described in the following chapter.