CHAPTER 1

INTRODUCTION

The present day multi core processor operates with a number of Phase Locked Loops (PLLs) that serve as clock generators for various processing modules namely cores, memory modules, interconnects and I/O interfaces. Moreover, these PLLs obtain their reference from a filter PLL in order to operate with clean reference clock signals, as discussed in the work proposed by Blaine Stackhouse et al (2009). Hence, each of these PLLs operates with different requirements and specifications. Therefore the PLL architecture incorporated in multi core architecture has to cater a wide variety of requirements and specifications. One such architecture is the self biased adaptive bandwidth PLL proposed by John Maneatis (1996), which has been widely used for more than a decade. However in the present day multi core scenario this architecture has been facing more and more severe design challenges.

The present research work undertakes a detailed study on the traditional self biased PLL and suggests modifications to enhance its performance in keeping with the requirements of present day multi core architecture. The traditional self biased PLL when proposed, was mainly designed by optimizing the loop parameters for minimum input tracking jitter contribution. These loop parameters that dictate jitter performance were maintained constant over the entire operating frequency range, independent of

supply voltage and process parameters, and this uniform condition for jitter performance was ensured through out its capture range. The traditional self biased PLL had also considered supply and substrate noise as the dominant sources of jitter, and had tailored its Voltage Controlled Oscillator (VCO) circuitry and its related bias generation circuitry to reject these noise sources. The charge pump circuits were designed to minimize their static mismatch currents and charge pump feed through effects. The architecture was thus designed to minimize static mismatch current but had significant dynamic mismatch current that had not been addressed.

This traditional self biased PLL in the present scenario operates in an environment in which the multi cores operate with widely varying operating frequencies and supply voltages. The operating frequencies and supply voltages are selected from a look up table, with the selections being switched at regular intervals (typically a microsecond or less). These selections are dictated by the computational load and enable the cores to operate at the optimum required frequency while meeting the power constraints. This requirement places severe constraints on the microprocessor clock PLL to have a short acquisition times, and also meet the design specifications at very low supply voltages. Also, since the operating frequencies of the cores have been increasing over the years, the margins available for timing uncertainties, and hence the jitter constraints on the clock PLL, has become progressively more stringent. Further, the clock generated from the PLL feeds a number of Delay Locked Loops (DLLs) and digital circuits, therefore the capture transients of the PLL can potentially unlock the DLL and violate the timing requirements for the digital circuits.

The present research investigates the possible modifications in the traditional self biased PLL, and a detailed study had been carried out to relook

at the traditional self biased PLL architecture with respect to jitter reduction, acquisition time and the reduction of the capture transients of the clock PLL and proposes modifications on the traditional self biased PLL to cater to these requirements.

1.1 PRESENT STATUS IN THE LITERATURE

The clocking architecture realized in the present day microprocessors, their typical specifications and their issues are important research areas that have been attracting a number of contributions in the literature.

The work reported in Blaine Stackhouse et al (2009) describes the clocking architecture of Quad core Itanium processor. The typical voltage frequency switching pairs are stored in a look up table, and the method by which the PLLs are switched for various operating frequencies are discussed in their work. The specifications and requirements of various PLLs namely system interface, I/O PLL, and core PLL have also been discussed. To minimize jitter, the self biased PLLs were always made to operate with highest possible signal swing.

The work reported by Nasser Kurd et al (2009) explains the Nahelem clocking architecture and describes their adaptive frequency system. Their work describes the method adopted to minimize capture transients so that the PLL architecture works at the highest operating frequency defined by VCO.

The work reported by Andrew Allen et al (2009) describes dynamic frequency switching of clock generators based on self biased PLLs for various Itanium processors. Their work reports the calibration flow that makes the

VCO operates at the best possible swing in order to optimize jitter, and hence adjusts its divider setting accordingly. This work also reports the typical reference clock frequency, range of output clock frequencies and the corresponding bandwidth of the various PLLs employed in their clocking architecture.

In the work reported by Jose Tierno et al (2010), a digital PLL is proposed for eight core processor clock that takes care of smooth frequency switching without any under shoot or overshoots in its capture transients, and thereby minimizing the impact of sudden changes in the current drawn from supply.

The present day processor cores, as reported in literature, are operated at very high frequencies and low supply voltages, and are also subjected to increasingly more acute jitter constraints. In spite of these severe constraints, the choice of the self biased PLL architecture for microprocessor clock generation is considered “unchallenged in the foreseeable future due to the wide frequency range required for product binning and power management” as described in Duarte D. et al (2010). In their work, the jitter induced by reference clock, feedback clock and VCO noise sources were considered as the predominant jitter contributing sources, and accordingly, modification in the traditional self biased PLL architecture to address the jitter induced by reference clock and charge pump circuits have been proposed. The modifications were targeted to operate the PLL with reduced VCO gain by means of an interpolated PLL architecture. The implemented design presents significant jitter reduction. All significant features of the traditional self biased PLL were retained except the symmetric load in the delay element, and thus this design lacks dynamic supply rejection capability.

Though there have been many papers appearing periodically in the literature addressing jitter issues, very few of these prescribe guidelines in choosing device dimensions in the various circuit blocks. It is noted in the work proposed by Mark Ferriss et al (2013), that the sizing exercise for noise can only be carried out with the help of simulations, as it does not lend itself to analytical solutions due to complicated interdependencies between VCO and charge pump noise contributions. Their work also provides guideline and discusses the methodology adopted in choosing VCO gain in a multi path PLL architecture.

The architecture of the self biased PLL was also modified and proposed by Song Ying et al (2008) by operating the self biased adaptive bandwidth PLL at various frequency sub bands covering a wide frequency range. In each operating sub band, the VCO gain is designed to be low, thereby ensuring a low jitter performance.

The principle of reduced VCO gain is widely applied in dual loop architecture for clock and data recovery circuits proposed by Seema Butala Anand et al (2001). In their work the possible sources of jitter were identified, and the impact of reference, feedback clock and charge pump induced jitter were minimized by operating with narrow bandwidth PLL. Jitter from VCO circuits was taken care in their work by operating their VCO with constant and high swing signals. Their circuits were entirely differential catering to the rejection of common mode noise sources. With all these features implemented, their work shows significant improvement in jitter performance.

Dual loop techniques using conventional oscillators operated with reduced VCO gain have recently been proposed by Akihide Sai et al (2012) and Dennis Michael Fischette et al (2010). The work proposed by Akihide Sai

et al (2012) considers the high gain VCO as source of jitter as it can amplify the noise originating from loop filter and charge pump circuits and proposes a dual loop PLL employing reduced VCO gain. Their work configures Type III PLL architecture by adding the low gain PLL path with the high gain PLL and addresses stability problems associated with type III PLL. The stability problem is addressed by operating their PLL with extremely narrow loop bandwidth. Their work reports significant reduction in jitter, but at the cost of compromising their settling time.

The PLL proposed by Dennis Michael Fischette et al (2010) meant for clocking processor I/Os, also operates with low gain VCO making their PLL narrow bandwidth. They apply this narrow bandwidth loop to filter noise from charge pump and loop filter circuits. Their work switches between an inductor based oscillator and ring oscillator based on their operating frequency range. Their work also shows significant improvement in jitter performance but with very long settling time.

A third order PLL is well known to optimize its performance in jitter, settling time and capture transients and can suit well for PLLs meant for multi core architecture. Analysis of third order PLL in deriving a stable architecture was studied by Habib Adrang et al (2009) by simulating the architecture in Matlab. The step response of their third order PLL was simulated that showed significant reduction in undershoot / overshoot transients with significant reduction in settling time, if the phase margin of the system is chosen optimally when compared with their second order PLL counterpart.

The independent control of overshoot / undershoot transients and settling time is described by Ken Gentile (2007) , suggesting in addition an

optimal choice of the phase margin. The realizable third order architectures and loop filter configuration that lead to stable third order PLL are derived in Donald Stephens et al (2002).

Adaptive bandwidth technique is also reported in the design of RF synthesizers incorporating LC VCO proposed by Ting Wu et al (2009). In this design the charge pump current is adjusted proportional to VCO frequency, in order to maintain loop bandwidth constant. This design however is not completely self biased and had not considered maintaining damping factor ζ constant.

Based on the above literature survey, it is concluded that

(i) The self biased PLL is an important architecture that will continue to play an important role in the context of microprocessor clock generation. There is also sufficient scope and demand in some of its key performance characteristics.

(ii) Many papers have addressed and attempted a variety of improvements in some of the relevant performance characteristics, but hardly any of these have been in the context of self biased PLLs for microprocessor clocks.

1.2 THESIS PROBLEM STATEMENT

Motivated by the status of the work reported in literature, the following are the problems taken up for investigation in the present work.

i. Systematic study of self biased PLL to choose the device dimensions optimally from a jitter standpoint.

ii. Adaptation of the self biased PLL to a dual loop PLL scheme to minimize jitter performance without any compromise in the salient features of the traditional self biased PLL.

iii. Investigations on the improvement that can obtained by adapting the self biased PLL into a third order system.

iv. Modifications of the self biased PLL to incorporate delay interpolation based VCO. This is expected to prevent degradation of VCO output swing as the operating frequency is varied and thus leading to an improvement in jitter performance.

The various chapters of this thesis discuss in detail all the modifications attempted and provide detailed simulation results in support of the various conclusions arrived at.

1.3 THESIS ORGANIZATION

Chapter 2 is devoted to the explanation of the functionality of traditional self biased PLL and presents the design / derivation of its loop parameters. The design of its functional blocks and their individual performances are described in this chapter. This complete design will serve as a reference PLL for the subsequent chapters.

Chapter 3 presents a systematic approach of designing the self biased PLL from a jitter minimization aspect. The simulation procedure through which the traditional self biased PLL was designed for minimum jitter is explained in detail, and the relevant simulation results are presented. The impact of noise transfer functions on the jitter performance of PLL, and

possible reductions in the contribution due to the noise transfer function are proposed and studied.

Chapter 4 primarily discusses the modification of the self biased single loop PLL into a dual loop PLL. This chapter describes the motivation for modification into a dual loop scheme, functionality of the architecture, and the derivation of its loop parameters. The chapter explains the method by which the gain of the VCO in this dual loop system is chosen and presents the circuit simulation results for the chosen gain. Finally the performance improvement of the modified dual loop system is compared with traditional self biased PLL.

Chapter 5 discusses two other attempted modifications. The first is that of adapting the second order self biased PLL in to third order self biased architecture, and the second is that of modification of the VCO architecture into a constant swing VCO with differential control voltage. The design of the third order PLL is described first, followed by the description of a constant swing VCO. The chapter illustrates the derivation of the loop parameters of both the systems and incorporation of self biased PLL principles into these. The simulation results of the realized systems and circuits are presented. Performance comparisons with the traditional self biased PLL are finally provided.

Chapter 6 concludes by comparing the performance of all the attempted modifications. It then discusses the key contributions of the present work. Finally the limitations of the present work and scope of further extensions are discussed.