

## TABLE OF CONTENTS

CHAPTER NO.	TITLE	PAGE NO.
	<b>ABSTRACT</b>	<b>iii</b>
	<b>LIST OF TABLES</b>	<b>xii</b>
	<b>LIST OF FIGURES</b>	<b>xiii</b>
	<b>LIST OF SYMBOLS AND ABBREVIATIONS</b>	<b>xvii</b>
<b>1</b>	<b>INTRODUCTION</b>	<b>1</b>
1.1	PRESENT STATUS IN THE LITERATURE	3
1.2	THESIS PROBLEM STATEMENT	7
1.3	THESIS ORGANIZATION	8
<b>2</b>	<b>SELF BIASED ADAPTIVE BANDWIDTH PLL</b>	<b>10</b>
2.1	TRADITIONAL SELF BIASED PLL	
	FUNCTIONAL DESCRIPTION	10
2.2	PLL SUB BLOCK DESCRIPTION	12
	2.2.1 Description of PFD and Charge Pump	12
	2.2.2 Description of Loop Filter	16
	2.2.3 Description of Self Biased VCO	19
	2.2.4 Description of Bias Generator	22
	2.2.5 Design Description of Prescalar	24
2.3	DESCRIPTION OF LOOP PARAMETERS	25
2.4	DESIGN DETAILS OF A NOMINAL SELF BIASED PLL	28
	2.4.1 Specifications of Loop Parameters	28
	2.4.2 Design of Bias Generator	29

<b>CHAPTER NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
	2.4.3 Design Description of VCO	30
	2.4.4 Design of Charge Pump Functional Block	33
2.5	CIRCUIT SIMULATION RESULTS OF REFERENCE PLL	34
2.6	SUMMARY	38
<b>3</b>	<b>JITTER OPTIMIZATION OF SELF BIASED PLL</b>	<b>39</b>
3.1	IMPACT OF SYSTEM PARAMETERS ON JITTER PERFORMANCE	39
3.2	DESIGN OF PLL FUNCTIONAL BLOCKS FOR MINIMUM JITTER	42
	3.2.1 Design of VCO Functional Block for Minimum Jitter	42
	3.2.2 Design of Charge Pump Circuit for Minimum Jitter	44
	3.2.3 Choice of Device Dimensions for Overall Minimum Jitter	45
3.3	IMPACT OF SYSTEMATIC NOISE ON PLL PHASE NOISE	47
3.4	ANALYSIS OF NTFS ON JITTER PERFORMANCE	49
3.5	SUMMARY	51
<b>4</b>	<b>DUAL LOOP SELF BIASED PLL</b>	<b>52</b>
4.1	DUAL LOOP PLL SYSTEM DESCRIPTION	53
	4.1.1 Modified VCO Functionality	54
	4.1.2 FLL System Functionality and its Loop Parameter Description	56

<b>CHAPTER NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
4.2	DESIGN METHODOLOGY FOR JITTER OPTIMIZATION USING REDUCED $K_{VCO}$	59
4.3	CIRCUIT SIMULATIONS OF DUAL LOOP PLL	62
4.4	SUMMARY	69
<b>5</b>	<b>DESIGN OF THIRD ORDER AND DELAY INTERPOLATOR BASED SELF BIASED PLL</b>	<b>70</b>
5.1	DESIGN OF THIRD ORDER PLL	70
	5.1.1 Third Order PLL System Description	71
	5.1.2 Description of Third Order PLL System Parameters	73
	5.1.3 Proposed PLL Design Specification and Simulation Results	75
5.2	DESIGN OF DELAY INTERPOLATOR BASED SELF BIASED PLL	82
	5.2.1 Adaptation of Delay Interpolator VCO to the Self Biased PLL	82
	5.2.2 Design of VCO	85
	5.2.3 Design of Bias Generator	88
	5.2.4 Proposed PLL System Design Description	88
	5.2.5 Charge Pump Circuit Design Considerations	89
	5.2.6 Proposed PLL Loop Parameter Description	89

<b>CHAPTER NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
	5.2.7 Proposed PLL Design Specification and Simulation Results	91
5.3	SUMMARY	96
<b>6</b>	<b>CONCLUSION AND FUTURE EXTENSION</b>	<b>97</b>
6.1	OVERALL SUMMARY AND OBSERVATION	97
6.2	CONTRIBUTION OF THESIS	100
6.3	LIMITATION OF THE PRESENT WORK	100
6.4	SCOPE FOR FURTHER WORK	101
	<b>REFERENCES</b>	<b>103</b>
	<b>LIST OF PUBLICATIONS</b>	<b>106</b>

## LIST OF TABLES

<b>TABLE NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
2.1	Nominal Device Dimensions Chosen in Charge Pump and VCO Circuits	34
2.2	Performance Measure Obtained from Circuit Simulation of Reference PLL	37
3.1	Overall Jitter for Different Choices of Device Dimension Combinations	47
4.1	Jitter Reduction as a Function of KVCO Reduction	61
4.2	Performance Comparison At Extreme Operating Frequency	68
5.1	Performance Comparison of Second Order PLL and Third Order PLL	81
5.2	Performance Comparison of the Traditional Self Biased PLL and the Proposed Self Biased PLL at the Extreme Operating Frequencies	95
6.1	Performance Improvements Provided By Different Modifications of Self Biased PLLs	99

## LIST OF FIGURES

FIGURE NO.	TITLE	PAGE NO.
2.1	Functional Block Diagram of Traditional Self Biased PLL	11
2.2	Circuit Schematic of Tristate PFD	13
2.3.a	Charge Pump Circuit Schematic	14
2.3. b	Bias Generator Circuit	15
2.4. a	Circuit Schematic of Loop Filter	17
2.4. b	Conventional First order Loop Filter	17
2.5	Circuit Schematic of Ring Oscillator Based VCO and its Delay Element	20
2.6	VI characteristic of Symmetric Load Resistance	21
2.7	Circuit Schematic of Bias Generator	23
2.8a	Functional Block Diagram of Divider	24
2.8b	Circuit Schematic of TSPC flip-flop	25
2.9	Frequency Response of Bias Generator	25
2.10	PLL Block Diagram Representation	30
2.11	VCO Gain Characteristic for the three Possible Choices of Device Dimensions	33
2.12	Capture Transients of Reference Self Biased PLL at a Nominal Frequency of 2.1 GHz	35
2.13	Eye Diagram Plot of Reference Self Biased PLL at a Nominal Frequency of 2.1 GHz	35
2.14	Static supply rejection characteristic of VCO	36

<b>FIGURE NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
2.15	Bias voltages showing dynamic supply rejection characteristic	37
3.1	Simulation Settings for Obtaining VCO Phase Noise Characteristic	43
3.2	VCO Phase Noise Plot at 2100MHz Frequency	43
3.3	Simulation Settings for Obtaining Charge Pump Output Noise Characteristic	45
3.4	Output Noise Current PSD of Charge Pump Circuit	45
3.5	Eye Diagram Plot of Output Clock	47
3.6	Control Voltage Ripple	48
4.1	Block Diagram of the Proposed Dual Loop System	54
4.2	Split Tuned VCO Showing the Modified Circuit of Delay Element and Half Buffer Replica Stage	55
4.3	Digital Control Circuit that Controls the Interaction Between FLL and PLL	58
4.4	Simulation setting used for measuring jitter for different $K_{VCO}$ settings	60
4.5	VCO Gain Characteristic of Split Tuned VCO	62
4.6	Capture Transients of Dual loop PLL at 2100MHz Output Frequency	63
4.7	Jitter Comparison of Traditional Self Biased PLL with Dual Loop PLL	64

<b>FIGURE NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
4.8	Process Corner Simulation at 1GHz Output	65
4.9	Process Corner Simulation at 2.5GHz Output	65
4.10	Comparison of static supply rejection characteristic	66
4.11	Bias voltages satisfying the requirement of dynamic supply noise rejection	67
5.1	Block Diagram of a Generic Third Order PLL	71
5.2	Block Diagram of the Proposed Third order PLL	73
5.3	Step Response of the Third Order PLL	77
5.4	VCO Gain of the Third Order PLL	78
5.5	Comparison of Control Voltage Transients of the Second and Third order PLL at 2.4GHz	79
5.6	Jitter Comparison at 2.4GHz	79
5.7	Control Voltage Transients of the Third Order PLL at Extreme Operating Frequencies	80
5.8	Control Voltage Transients of the Third Order PLL at Process Corners	81
5.9	Block Diagram of Self Biased PLL	83
5.10	Functional Block Diagram of the Proposed Self Biased VCO	84



<b>FIGURE NO.</b>	<b>TITLE</b>	<b>PAGE NO.</b>
5.11	Circuit Diagram of the Modified Delay Element	85
5.12	RC Equivalent Model of a Single Delay Element	86
5.13	Circuit Schematic of Bias Generator	87
5.14	Architecture of Charge Pump Circuit Generating Differential Control Voltage	89
5.15	VCO Gain of the Proposed Self Biased PLL	92
5.16.a	Traditional Self Biased VCO Swing	92
5.16.b	Proposed Self Biased VCO Swing	93
5.17	Capture Transients of Bias Voltages of the Traditional and the Proposed Self Biased PLL at 2.1GHz	93
5.18	Jitter Performance at 2.1GHz output frequency	94

## LIST OF SYMBOLS AND ABBREVIATIONS

### Symbols

$\omega_{3dB}$	-	3dB bandwidth
$\omega_{ref}$	-	Angular frequency of reference clock
$\omega_{VCO}$	-	Angular frequency of VCO
$I_{avg}$	-	Average Charge pump output current
$I_{ss}$	-	Bias current defined in one of the parallel transistor in delay element
$C_{cons}$	-	Capacitance of constant delay buffer stage
$I_{cp}$	-	Charge pump current
$I_{cp}$	-	Charge pump current
$k_{fast}$	-	Coefficient associated with fast path
$k_{slow}$	-	Coefficient associated with slow path
$V_{ctrl}$	-	Control voltage
$V_{ctrl\_FLL}$	-	Control voltage of FLL
$V_{ctrl\_PLL}$	-	Control voltage of PLL
$\Delta V$	-	Control voltage ripple magnitude
$\Delta T$	-	Control voltage ripple pulse width
$\zeta$	-	Damping factor
$A$	-	Delay element gain
$kp$	-	Device transconductance parameter of PMOS transistor
$F_{div}$	-	Divided feedback clock
$C_{eff}$	-	Effective capacitance of oscillator
$V_t'$	-	Ideal control voltage under locked condition
$\Delta V_{ctrl}$	-	Incremental change in control voltage
$\Delta \omega_{out}$	-	Incremental change in VCO angular frequency

$\Delta I_{cp}$	-	Incremental charge pump current
$F(s)$	-	Loop filter
$\mu_p$	-	Mobility of PMOS transistor
$\beta$	-	Modulation index
$\omega_n$	-	Natural resonant angular frequency
$H_{CP}$	-	NTF of Charge Pump
$H_{DIV}$	-	NTF of divider
$H_{LPF}$	-	NTF of loop filter
$H_{VCO}$	-	NTF of VCO
$C_B$	-	Output capacitance of delay element
$\overline{i_{cp,n}^2}$	-	Output noise current PSD of charge pump
$C_{ox}$	-	Oxide capacitance
$K_{PD}$	-	PD gain
$K_{PD}$	-	PD gain
$P$	-	Peak power
$\theta_e$	-	Phase error
$H(s)$	-	PLL closed loop transfer function
$F_{out}$	-	PLL output clock
$N$	-	Prescalar value
$t_p$	-	Propagation delay
$\overline{v_{lpf,n}^2}$	-	PSD of loop filter noise voltage
$\overline{\Phi_{cp,n}^2}$	-	PSD of Output phase noise of PLL due to noise source in charge pump
$\overline{\Phi_{div,n}^2}$	-	PSD of Output phase noise of PLL due to noise source in divider
$\overline{\Phi_{out,n}^2}$	-	PSD of Output phase noise of PLL due to noise source in divider
$\overline{\Phi_{lpf,n}^2}$	-	PSD of Output phase noise of PLL due to noise source in loop filter

$\overline{\Phi_{vco,n}^2}$	-	PSD of Output phase noise of PLL due to VCO noise sources
$y$	-	Ratio of current defined in integral charge pump to the current defined in delay element
$x$	-	Ratio of current defined in proportional charge pump to the current defined in delay element
$z$	-	Ratio of current defined in transconductance stage to the current defined in delay element
$F_{ref}$	-	Reference clock
$T_{ref}$	-	Reference period
$R_{slow}$	-	Resistance of constant delay buffer stage
$R_{fast}$	-	Resistance of fast path delay element stage
$R_{cons}$	-	Resistance of slow path delay buffer stage
$\sigma_t$	-	RMS jitter
$V_{bp}$	-	Symmetric load bias voltage
$R_{on}$	-	Symmetric load resistance
$V_{bn}$	-	Tail current bias voltage
$V_{bn\_FLL}$	-	Tail current bias voltage of FLL in dualloop
$V_{bn\_PLL}$	-	Tail current bias voltage of PLL in dualloop
$V_{TO}$	-	Threshold voltage of MOS transistor
$\tau_{fast}$	-	Time constant of fast path
$\tau_{slow}$	-	Time constant of slow path
$g_m$	-	transconductance
$W/L$	-	Transistor aspect ratio
$\theta_{out}$	-	VCO instantaneous phase
$V_x$	-	Virtual node voltage of opamp

## Abbreviations

BG	-	Bias Generator
BSIM	-	Berkley Short Channel Insulated Gate Field Effect Transistor Model
CMFB	-	Common Mode Feed Back
CMOS	-	Complementary Metal Oxide Semiconductor
CP	-	Charge Pump
DLL	-	Delay Locked Loop
FD	-	Frequency Detector
FLL	-	Frequency Locked Loop
FoM	-	Figure of Merit
NTF	-	Noise Transfer Function
PFD	-	Phase Frequency Detector
PLL	-	Phase Locked Loop
PSD	-	Power Spectral Density
RMS	-	Root Mean Square
TSPC	-	True Single Phase Clocked
UGB	-	Unity Gain Bandwidth
UI	-	Unit Interval
UMC	-	United Microelectronics Corporation
UP / DN	-	Up / Down
VCO	-	Voltage Controlled Oscillator