CERTIFICATE

1. This is to certify that all corrections and suggestions pointed out by the Indian /Foreign Examiner(s) are incorporated in the Thesis titled "Investigations on possible modifications of Maneatis PLL for microprocessor clock generation " submitted by Mr./MsJ.Dhurga Devi.

Signature of the Supervisor

Place: Chennai

Date: 06/08/14

CENTRE FOR RESEARCH
ANNA UNIVERSITY, CHENNAI – 600 025

PROCEEDINGS OF THE Ph.D VIVA-VOCE EXAMINATION OF MS. J.DHURGA DEVI HELD AT 2-00 P.M. ON 05-08-2014 IN THE MINI AUDITORIUM OF ECE DEPT. CEG CAMPUS, ANNA UNIVERSITY

The Ph.D. Viva-Voce Examination of Mr./Ms.J.Dhurga Devi (Reg. No.2006419116) on her Ph.D. Thesis Entitled "Investigations on possible modifications of Maneatis PLL for microprocessor clock generation" was conducted on 05-08-2014 at 2-00P.M. in the Department of Dept. of ECE, CEG Campus, Anna University.

The following Members of the Oral Examination Board were present:

1.	Dr. Shouri Chatterjee	Indian Examiner
2.	Dr. S.Aniruddhan	Subject Expert
3.	Dr.P.V.Ramakrishna	Supervisor & Convener

The research scholar, Ms.J.Dhurga Devi presented the salient features of her Ph.D. work. This was followed by questions from the board members. The questions raised by the Foreign and Indian Examiners were also put to the scholar. The scholar answered the questions to the full satisfaction of the board members.

The corrections suggested by the Indian/Foreign examiner have been carried out and incorporated in the Thesis before the Oral examination.

Based on the scholar's research work, her presentation and also the clarifications and answers by the scholar to the questions, the board recommends that Ms.Dhurga Devi be awarded Ph.D. degree in the Faculty of Information and Communication Engineering

1.	J.Chatterjee	Indian Examiner
2.	S.Aniruddhan	Subject Expert
3.	Ramakrishna	Supervisor & Convener
4.		Joint Supervisor (if any)

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CHENNAI-600 025

CERTIFICATE

The research work embodied in the present thesis entitled **"INVESTIGATIONS ON PERFORMANCE IMPROVEMENTS OF SELF BIASED ADAPTIVE BANDWIDTH PLLs"** has been carried out in the Department of Electronics and Communication Engineering, CEG Campus, Chennai. The work reported herein is original and does not form part of any other thesis or dissertation on the basis of which a degree or award was conferred on an earlier occasion or to any other scholar.

I understand the university's policy on plagiarism and declare that the thesis and publications are my own work, except where specifically acknowledged and has not been copied from other sources or been previously submitted for award or assessment.

Counter Signed by

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