CHAPTER 6

CONCLUSION AND FUTURE EXTENSION

The present research work had demonstrated possible alterations in the architecture of traditional self biased PLL without compromising its salient features. The overall summary of the modification carried out in the present work, the contribution made by this research work and limitations of the present work is presented here. Finally the future scope of extension of the present wok is described here.

6.1 OVERALL SUMMARY AND OBSERVATIONS

With the goal of optimizing its jitter performance this work has proposed a design procedure to choose the device dimensions of the self biased PLL. This jitter optimized PLL was derived from the traditional self biased PLL was described in Chapter 3 and was considered as a reference system against which further improvements can be benchmarked.

As a first modification of the self biased PLL, the dual loop architecture incorporated with a reduced VCO gain architecture was discussed in Chapter 4. This reduced gain dual loop PLL architecture was effective in reducing the impact of systematic noise on jitter performance. The circuit simulations of the dual loop architecture showed significant improvement in jitter performance, and it also improves performance in terms of capture transients and frequency acquisition time. Since the PLL operates with low gain, the phase acquisition was observed to get degraded when

compared with traditional self biased PLL but was observed to be superior to the recently reported work in literature.

The second modification considered was that of a third order self biased PLL and was described in Chapter 5. The optimal choice of loop parameters were derived such the phase margin was maximized leading to minimum settling time and overshoot/undershoot magnitudes. The third order PLL introduced an additional transconductance gm and capacitance C in the traditional second order self biased PLL and improved the loop gain by the factor of gm/C. Hence it operates with narrower bandwidth compared with the traditional self biased and thus had the capability to filter inband noise leading to significant jitter improvement.

Chapter 5 also discusses the other modification that retained constant swing in the VCO output signal, and also used a differential control voltage showing significant jitter reduction. This is due to reduced VCO noise (large swing thoughout), and rejection of systematic noise in the control voltage (differential). The other performance characteristics namely settling time and capture transient magnitudes remained the same as in the traditional self biased PLL.

The performance of the three modifications attempted in the architecture of the traditional self biased were compared with the traditional self biased PLL and are consolidated and presented in Table 6.1. The dual loop PLL shows improvement in its jitter and capture transients but shows degradation in its settling time due to its low gain PLL. This need not be considered as a drawback since the PLL in the dual loop only carries out fine acquisition of the frequency and its acquisition time may not be detrimental in microprocessor applications. The performance of the third order PLL showed improvement in its jitter and capture transients without any degradation in its settling time, whereas the jitter performance in its lower frequency range

(lower 800MHz range), which is not listed in the tabulation, is observed to get degraded. This is because of the fixed resistance used and hence its phase margin (is not adaptive) gets altered one of the extreme frequencies. Jitter performance of the PLL employing delay interpolator based VCO shows improvement in jitter performance without any degradation in its settling time. Thus the improvement in performance in all the modified architectures was observed.

Table 6.1 Performance Improvements Provided by Different Modifications of Self Biased PLLs

	Traditional self biased PLL	**Dual loop Self Biased PLL**	**Third Order Self Biased PLL**	**Delay Interpolator Based Self Biased PLL**
Output Frequency (MHz)	2720	2500	2700	2720
Reference (MHz)	170	170	170	170
Tuning Range (GHz)	0.8-3.2	1-2.5	1-2.7	0.9-2.7
K_{VCO} (MHz/V)	3600	470	3600	3600
Lock Time (μS) (Frequency step in MHz)	0.16 (1400)	<1 (710)	0.19 (1000)	0.188 (1300)
RMS Jitter (pS) (UI %)	1.6 (0.43)	0.45 (0.11)	1.1 (0.3UI)	0.8 (0.21UI)
Peak Undershoot magnitude (MHz)	557	32	0.0023	-----
Power (mW)	35.0	35.8	40	26

6.2 CONTRIBUTION OF THESIS

The following briefly are the contributions of the present work:

i. With the goal of improving jitter performance, a simulation based systematic design methodology has been proposed for choosing the device dimensions of the traditional self biased PLL.

ii. The dual loop self biased PLL was derived by preserving all the salient features of the traditional self biased PLL and the resulting performance was demonstrated.

iii. The second order self biased PLL was also modified into a third order scheme and improvements were demonstrated.

iv. The self biased PLL was also modified by adopting a VCO that is based on the delay interpolation principle. It was demonstrated that the use of this constant (large) swing VCO leads to improvements in jitter performance while still retaining all the other salient features of the self biased PLL.

6.3 LIMITATIONS OF THE PRESENT WORK

i. In the dual loop modification, the frequency detector has a limited linear operating range as the maximum frequency deviation it can detect is its input frequency. This is because this FD cannot distinguish between its input and its harmonics. Hence to make the dual loop PLL operate over the entire linear range of the traditional self biased PLL, the operating

frequency range was divided in to two frequency bands of 1.7GHz to 2.7GHz and 2.7GHz to1GHz and the control voltage was externally forced to switch the free running frequency to the centre frequency of these two frequency bands.

ii. In the third order PLL, a larger capacitance has to be used when compared with the traditional self biased PLL in order to maintain stability of the PLL over a wide capture range.

iii. In the delay interpolation based architecture, the principle of operation was demonstrated, therefore an ideal Common Mode Feed Back (CMFB) circuit was used to retain the common mode of the differential control voltage signals.

iv. The main weakness of the present work is lack of substantiation with actual device fabrications and measurements, but given the original objective, it is believed that the gross conclusions about the orders of improvements expected for the various modifications proposed would still remain valid.

6.4 SCOPE FOR FURTHER WORK

This research work can be extended by incorporating the constant swing VCO in the dual loop PLL architecture, thereby the VCO signal swing dependence on operating frequency in the dual loop can be eliminated.

Also, the delay interpolator VCO architecture can be incorporated into the third order PLL architecture, and this in turn can minimize the capture

transients present in the delay interpolator based PLL architecture can be minimized, and further improvement in jitter performance can be obtained.

Also, the delay element with a differential architecture can be replace the inverter based delay elements, without compromising the salient features of traditional self biased PLL architecture. This modification can thus enable the architecture to suit well in lower supply voltages and can also make the VCO operate with increased signal swing.