

Chapter 2

LITERATURE SURVEY

2.1 Introduction

An efficient parallel operation of distribution communication system can be achieved by using Re-configurable co-processor techniques it can be carried out by an instruction status of the sectionalizing switching device and changing the code rate.

The switching must be performed in such way that accuracy of data transmission and reception is increases and reliability of original data of the communication system global network is maintained and the entire load is energized. It clearly shows the greater the numbers of switches, the greater probability of Re-configurable communication operation and better efficiency. The Re-configurable communication system network has been implemented to achieve goals as the load balancing or voltage stability, reduction of power loss, in normal operation conditions and simultaneously improve accuracy and reliability of a communication system by reducing the impact of potential contingencies.

Chin-Liang Wangt and Ching-Hsien Chang have developed a new VLSI architecture for computation of N-point DFT of real data and the corresponding IDFT based on discrete Hartley transform. Here N is a power of two. The architecture developed has two real multipliers, six memory-based buffers, three real adders, two ROM's few simple logic circuits. The architecture evaluates one DFT sample or one IDFT sample for every $(\log(2N+1))/2$ clock cycles on an average. the design proposed is capable of operating at a clock rate of 100Mkz to achieve a throughput of 20M transform samples for every second for N=512 under 0.35 μ m CMOS technology [8].

Chen huang et.al [9] has developed an online algorithm which is capable of managing co-processor loading. The AG algorithm makes use of aggregated gains in order to guide co-processor load, its placement, replacement and also wait decisions. Many experiments have been conducted using embedded system applications, for biased random and also periodic input application sequences wide range of re-configuration times and variety of FPGA types with

different number of partial re-configurable regions have demonstrated the fact that AG algorithm is very robust for a range of situations. The results of the experiments carried out are with 15% of unlimited-size Field-Programmable- Gate-Array on an average and it has 1.4 times of speed up as compared to loading of a static co-processor , 3 times of speed up in execution on microprocessor only solution. The draw backs of the above architecture include more cost compared to custom silicon, slow, zero dynamic logic. In addition it requires more space (i.e. transistors) on the chip and also application runs slower on FPGA.

Vuletic, M. Sch et.al [10], has introduced a virtualization layer. This virtualization layer will allow re-configurable application specific co-processor to have access on the user space virtual memory and also have sharing of memory address space with user applications. The difficulty here lies in limited effectiveness with certain codes line I/O bound, memory bound) using L2 Cache memory.

Kumar, A Raman, et.al [11] have proposed a Re-configurable FFT which can be used to design Vedic mathematics, Vedic multiplier developed by them is the best algorithm for multiplication compared to other popular algorithms for multiplication. Using this algorithm, partial generated product can be obtained in parallel sequence.

Sung D. Kim et,al [12], has proposed a DSP that employs Bit manipulation unit (BMU) which support parallel shift and also Exclusive-OR operation and also bit insertion or bit extraction operations on multiple data. The architecture is modeled by VHDL and SEC 0.18 μ m standard cell library is used for its synthesis. The BMU has only 17000 gate counts. [13][14].

Hongjiang He et.al [15] has described two approaches to implement FFT. One of them is implemented as Field-Programmable- Gate-Array co-processor. The other approach makes use of only an external digital signal approach. Various tests have been conducted to examine the advantage and Disadvantage with respect to power consumption, performance cost and also case of implementation perspective.

Oike, Y. et,al [16], has presented a concept for high speed and low voltage co-processor which makes use hammer distance ordering . The circuit implementation for this concept is also done. The designed circuit provides unlimited capacity for data base. It also has advantage of low voltage operation (<1V) for system on chip application. The co-processor fabrication is a 0.18 μ m 64-bit and 32-word associative co-processor. This co-processor can operate at frequency of 411.5 MHz at 1.8V and 40MHz at 0.75 V respectively [17].

Takashi Miyamori, Kunle Olukotun et al [18] has proposed computer architecture to combine a Re-configurable Co-processor with general purpose microprocessor. A study has been made on multimedia applications of Re-configurable Co-processor. Re-configurable multimedia array Co-processor makes use of a 16-bit simple processor.

It is larger compared to configurable logic block of a Field programmable gate array. Simulations performed on Re-configurable Multimedia Array Co-processor (REMARC) shows that there is a speedup from a factor of 2.3 to 7.3 on all the applications. A simulator has been developed. A programming environment has been designed and multimedia applications of the two Co-processors.

2.2 Different types of Re-configurable Co-processor for Communication Systems are

- (a) Static Partial Reconfiguration
- (b) Dynamic Reconfiguration
- (c) Self-Reconfiguration
- (d) Evolution type

The static partial Re-configurable device is not active mode during the Re-configurable process while partial data sent into the Field-Programmable-Gate-Array (FPGA). the rest of the device is stop working (in the shutdown mode) and brought up after the configurable is completed.

There are two type of static partial Re-configurable of FPGA devices are:

- i) Module –based partial Re-configurable
- ii) Difference-based partial Re-configurable.

2.2.1 Module-based partial reconfiguration

Trailokya Nath Sasamal, Rajendra Prasad has made a study and review of existing partial Re-configurable methods, steps, partial Re-configurable medium and application of it on Xilinx FPGA. Swapping in and swapping out on the fly is possible by partial Re-configurable modules from operating environment control.

Distinct modular parts of the design can be Re-configured by module based partial Re-configuration. Arrangement of special bus macros have to be made in order to ensure communication across Re-configurable module boundaries.

The Re-configurable module is connected with rest of the design by special bus macro. A set of specific guidelines has to be performed by module-based partial Re-configurable at the design specification stage.

Advantages of module-based partial Re-configurable are Modular Design Methodology, High storage cost, Long Re-configuration Latency, Systematic design of larger systems, Area-constrained placement and routing process, No hardware support to guarantee successful P and R, Communication between modules is done through tri-state buffers, Care should be taken that tri-state buffers are not being reconfigured.

Disadvantage of Module-based partial Re-configuration are the increased component count and Process Control Block (PCB) requirements necessary to accommodate an external device, Module-based partial Re-configuration used in Embedded FPGA Applications in that application they require external controller presents undesirable drawbacks, for these results there is a needlessly high data transfer, If entire device is fully reconfigured more useful data is lost.

2.2.2 Difference-based partial reconfiguration

R.V.Kshirsagar and S. Sharma have addressed main aspects of difference based partial Re-configuration upon Xilinx FPGAs .Small on the fly-change with respect to design parameters such as logic equations, I/O standards, filter parameter can be made with the help of difference based partial Re-configuration has been discussed by the authors. VHDL has been used to model full adder/full subtractor and up/down counter. It is implemented on Xilinx SPARTAN 2SXC30tq144 FPGA board using difference based Re-configuration. The equation on FPGA gets rearranged which results in time reduction and generation of bits which have to be loaded on the chip [19]

Advantage of difference-based partial Re-configuration is Suitable for very small designs, the Re-configuration storage and time cost are proportional to number of frames that are different, Very inefficient for large designs, Compares the circuit description of two novel designs, note the different frames between the two designs and creates a partial bit stream that only modifies the frames that are different, Both the designs have to be same at the layout level.

Disadvantage of difference-based partial Re-configuration are Design time and NRE costs may be high, Flexibility is low, Routing Issues.

2.2.3 Dynamic Reconfiguration

Vincent Talbot & Ilham Benyahia have defined a methodology which enables applications to adapt to sudden changing environments. Here the dynamic architecture Re-configuration is based upon multiple criteria decision making which uses to find finest combination of architecture components pareto evolutionary algorithm adapting penalty which is one of the evolutionary computing techniques is adopted to handle time consuming online process which are essentially required by E C like genetic algorithms. Traffic management is one of the major tasks where continuous monitoring of traffic and the routes is necessary.

Different scenarios of road safety like minimizing the consequence of injury during accidents and avoiding congestion that causes crashes have been discussed where dynamic architecture Re-configuration is required.

A simulation tool known as simulation of urban mobility (abbreviated as SUMO) is selected to connect with ITS framework.

The simulation result on road safety cases have depicted benefits of MCDM in avoiding congestion as well as minimizing delay of ambulances or any other emergency vehicles.

Devices like Xilinx XC-6200 series which allow high-speed partial Re-configuration have helped in feasibility of Dynamic Re-configuration of FPGAs. System software is used to perform Dynamic Re-configuration on a regular basis. This system software decides when to re-program a part of the FPGA and the information for re-programming. A pre-compiled circuit will be selected by run-time software and the programming data is transmitted directly to the field programming gate array [20]

Advantages of Dynamic Re-configuration are the dynamic Re-configuration is save both power and area and it Reduced time to market. With minimum requirements, Dynamic Re-configurable Design can be sent to market for use and at a later stage, the user can add more features without any change in route of system. Thus Re-configurable computing allows incremental design flow. An intelligent run time system is needed to ensure that power is saved and that timing constraints are meet when using partial Re-configuration for real time systems. Measuring power consumed during dynamic Re-configuration supports to determine the feasibility and the design of the run time system of a device.

Certain issues contribute to the disadvantage of dynamic Re-configuration. Some of them are listed below.

- Placement issues: whenever a new hardware component has to be Re-configured, sufficient space is required to place this new hardware component. This issue of component placement becomes more complicated if the component has to be placed closer to special resources such as DLLs on FPGA memory (i.e. built in memory) or I/O pins.
- Timing issues: the timing requirement has to be met by the hardware configured so that the device operates efficiently. If longer wires are used to connect the hardware components, the timing might be affected. It may also result in over timing or under timing errors. Erroneous results might also occur by newly added design.
- Routing issues: if newly Re-configured hardware components have to be connected to existing hardware components, there must be availability of ports to interface the new hardware components.
- Consistency issues: the design's computational consistency should not be ignored by the device's dynamic Re-configuration. If a partially Re-configured FPGA is made to interface with an existing design, then the problem becomes very critical. The existing design should not be modified or erased when new hardware components are added to the device with the Re-configurable fabric. The development tools for commercial dynamic Re-configurations are yet to be completely established. There is a lack of availability of tools for specification level to implementation level of the design. The tools available commercially need a lot of human interference for complete system implementation.

2.2.4 Self-Re-configuration

Aranca Casal, Mark Yim, et.al, have considered a special case of Re-configurable robots which are made up of hundreds or even thousands of identical modules which have the capability to Re-configure into required various shapes as per the task at a given period of time. [21]

A divide – and – conquer strategy has been proposed which is a Re-configuration solution for a class of problems which is termed as closed chain Re-configuration solution for a class of problems which is termed as closed chain Re-configuration . the class of problems considered includes Re-configurable robots which have topology defined by 1D (one dimension) combinational topology.

The topology of robot is first decomposed into a series of small sub-structures which is part of a finite set. The operational steps of basic Re-configuration in between the sub-structures are a set of previously computed, optimized and saved in look-up table. Next the Re-configuration process will have a well-organized series of very simple, previously computed sub-reconfigured which happens locally within the sub-structures. The three classes of Re-configuration discussed are mobile substrate and closed chain Re-configurations.

A topological space and a re-configuration algorithm suitable for the requirement have been presented for the class of closed-chain Re-configuration.

A hierarchical substructure decomposition (HSD) method has been introduced. This method divides the configuration of robot into a hierarchy of sub-structures. The simulation shows satisfactory results from two algorithms which are based upon HSD.

2.3 Dynamically Re-configurable Cache for High Performance and Low Power

Alan Turing develops a device that could perform all computable functions but he could not able to build one chip. Given enough memory and time, a general-purpose, a digital computer can emulate a turing device over the past few decades digital system developer have built larger memories and faster processor in an attempt to create turing's device however, some tasks still not able execute within a reasonable period of time. For this reason, computer science engineers continually develop new concepts and techniques to improve processing performance.as the performance of processors begun to exceed the capabilities of memory structures, computer science architects developed a memory hierarchy to improve performance. Usually, the processor requests data from the memory hierarchy, computer depends on memory hierarchy to hide the latency of accessing large memories and the memory hierarchy tries to respond with the data as quickly as possible [22].

Disadvantage of Dynamically Re-configurable cache for High performance and low power:

- There is an increase in accessing time. Time is because cache access time is dependent on the depth of memory. As memory depth increases time for accessing also increases.
- Increases requirement of on-chip caches for better performance of modern processors.

- An assumption made is that there is no slack available w.r.t. cache access time however if any small modification is made in base cache, it results in minimum one-extra-cycle-access-penalty.

2.4 Coarse-Grained Re-configurable Architectures

R. Hartenstein has compared fine grained FPGA's and coarse grained Re-configurable architectures.

Fine granularity Re-configurable architecture has certain disadvantage. Usage of this architecture leads to low-silicon-area-efficiency of FPGA computation solutions. Also the wires for switched routing make use of more power compared to hard-wired connections. Another disadvantage is that if large number of routing switches and processing units are present configuration data [23].

The coarse grained Re-configurable architecture tries to overcome the disadvantage faced with FPGA based computation solutions. It provides multiple bits wide data paths and also complex operators in comparison to bit level configuration. Also connections between different processing elements are multiple-bit wide, so there is high usage of area for single line.

Disadvantage of coarse-grained Re-configurable architecture:

- As the number of operational block increases, the Coarse-grained Re-configuration Architecture needs more clock cycles.
- As the number of block increases, the area of Coarse-grained Re-configuration Architectures also increases.

2.5 DP-FPGA (Data path FPGA)

D.lewis and D.cherepacha have introduced a new FPGA architecture reduce the gap in density between mask-programmable gate array (MPGA) and field programmable gate array (FPGA) for data-path oriented circuits. The network interconnection includes unique and different sets of resources for data signals and routing control. The circuit area is reduced by sharing of the programming bits among the 4-bit slices which reduces the requirement of total number of storage cells.

The requirements of routing structures and logic blocks which can be made use of for implementation of typical circuit's contain a large number of regularly-structured data paths of different sizes and also their irregularities.

A set of logic-block architecture has been proposed by the authors and analyzed empirically. Furthermore, estimation of implementation area predict that area of design's data path will be reduced by a factor which is approximately two compared to the existing conventional method FPGA architecture by using programming bits sharing method [24][25].

Disadvantage Data path FPGA method:

- Usage of instruction pipelines in modern CPU's instruction for the process of execution based on one input and one output only concept.
- If multiple execution units are present, the CPU cannot predict which instruction can be executed because of pipelining branching difficulty.
- As the pipelining increases, the efficiency decreases and it also reduces the number of instructions executed for one cycle by the processor.

2.6 The CHESS Array

Marshall, tony et.al, have discussed about architecture choices used for CHESS. It increases density of arithmetic computations. It also increases bandwidth and capacity of memory (internal) beyond current FPGA capabilities. Benefits of CHESS in application areas include improvements in memory bandwidth, computational density flexibility and rapid reconfiguration. CHESS can be used to build data paths, controlling FSMs, using on-chip memory. Achievement of high computational density is done by using 4-bit bus (or buses) for routing. Adoption of a chessboard kind of layout is achieved. [26]

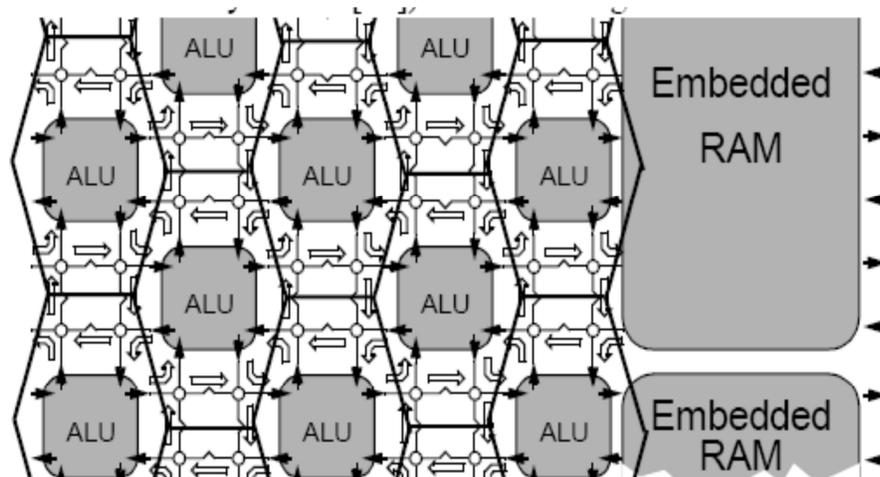


Figure 2.1 chess array

An ALU data output may feed into the configuration input of another ALU. This might result in change in its functionality on a cycle per cycle basis at runtime. This occurs without uploading of data. But uploading by partial configuration cannot happen, as shown in Figure 2.1.

Disadvantage of CHESS array

- The first problem that even a beginning programmer should identify is that to access any square of the chess board.
- The second problem about testing procedure on each newly generated square number to make sure we don't step off the edge of the board in any direction
- In one-dimensional array when we implement it as given, it really saves very little source since a good super-scalar processor will execute the multiply/add/subtractor while waiting on the branch to complete.

2.7 Integrated Protection and Re-configuration Design for the All-Electric Ship

Yanfeng Gong, Mississippi State Univ., Starkville, MS, Yan Huang, Schulz, and N.N. The shipboard power device for the all-electric ship creates a unique set of challenge in protective system design. Traditional fast fault isolation may not be enough to maintain system stability after a server fault. Here they developed a special protection system that combines fast remedial actions and protection functions [27]

The dynamic-zone-selection based differential protection system is adapted to power system Re-configuration in addition to this it provides a continuous reliable protection. The special Protection device was implemented in programmable digital relays to protect a 4 generator ship-board power system and tested using a real time digital simulation device. Tests results prove that the designed first phase protection system design performance is satisfactory.

Disadvantage of integrated protection and Re-configuration design for the all-electric ship board:

- In ship-board can withstand only a limited number of write and erase cycle before failure.
- A drawback to the small size is that they are very easily misplaced for this particular problem if the data they contain are sensitive is lost