ABSTRACT

There has been an increasing demand on the quality of data transmission and reception. As a result, there has been an increase in bandwidth on demand and quality of service. These results in increase of data traffic which results in information loss, accuracy reduction and reliability reduction. A co-processor is designed to overcome this drawback which can be used for communication operation, which is highly reliable and more accurate with less delay. The research high speed reconfigurable coprocessor can be easily implemented using various standard operations such as Bit shuffle operation, convolutional encoding, fast Fourier transform, interleaving, modulation, scrambling, Shift-XOR array, viterbi decoding and many other functions which make use of the research design. The high speed Re-configurable Co-processor for scrambler and de-scrambler system is used in a communication system with more number of data that will be transmitted through a media and that transmitted data will be more secure and authenticated. With the help of the scrambler device, user will be adding some unknown data's to the original-data's or by changing some important sequence of the original-data's so that it will be difficult for an unauthorized person to identify original data. If we want to identify the original data we need to use appropriate descrambler system. As data transmission gradually increases it causes noise due to which some incorrect information will be received at destination, which reduces the reliability and accuracy of the data. To overcome this overhead we develop a reconfigurable convolution encoder and Viterbi decoder which reduce the effect of Noise in digital data transmission. Convolution codes are used to implement forward error correction (FEC). The Decoder complexity is directly proportional to constraint length K. The convolution encoder and Viterbi decoder influence FEC technique. The main objective of this work is to improve the fabrication techniques in terms of nano meter with multimillion gate densities, to increase the redundancy by using co-processor and perform many parallel operations without any overhead and also performance of FPGA is compared with existing DSP chip .The coprocessor has been modeled using VHDL and synthesis has been performed on model-sim. The critical path about 0.16 nm technology and gate count of about 40000. This performance shows that number of operation / cycle can be reduced about 58% for scrambler at transmitter side, 94% for convolutional encoding, Multiply Research 4 Operation/Cycle, Addition And Subtraction 4 Operation/Cycle, MAC 4.5 Operation/Cycle, Complex Multiply 1.5 Operation/Cycle, FFT Butterfly 2 Operation/Cycle and 61% for de-scrambler at receiver side. It shows the research reconfigurable co-processor is having the better performance compared to existing conventional DSP in terms of number of operation/ cycle.