Chapter 8

CONCLUSIONS AND FUTURE SCOPE

8.1 Conclusion

The research work provides the design of high speed re-configurable co-processor for next generation communication system and its implementation. Various algorithms and various communication standards can be supported using the proposed re-configurable co-processor. The re-configurable techniques help in achieving efficient operation of distribution communication system. The proposed co-processor is capable of performing convolution-encoding, scrambling viterbi-decoding, interleaving, FFT which find extensive applications in communication systems. The re-configuration of communication system has been implemented by code rate change and an instruction status of sectionalizing switches. VHDL has been used for modelling of the co-processor. Xilinx ISE 14.1 is used for its synthesis and waveform at each stage is observed using model-sim. The comparison of performance between proposed co-processor and existing DSP's show that requirement of number of clock/cycles can be reduced to about 84% for convolutional-encoding and about 48% for scrambling process. The performance results show that the proposed co-processor is better compared to convention DSP (example sc-140) respect to number of clock per cycle. For example, sc-140 has a capability to perform 2-trellis –butterfly calculation per one cycle whereas the proposed co-processor can perform 3-trellis-butterfly calculation per one cycle. Comparing the performance results of bit shuffle unit, with star-core (sc-140), the novel architecture of the proposed co-processor has the ability to bring a reduction of about 67% in clock/cycles for convolutional encoding and about 78% reduction for in clock/cycles block interleaving. Comparison of the proposed architecture with TC62X shows that the proposed architecture is capable of bringing about 48% reduction in clock/cycle for scrambling process and about 84% reduction in clock/cycle for convolutional encoding.

8.2 Future Scope

- The proposed co-processor can be made applicable for wireless communication which finds tremendous application in Radio communication system, Broadcasting, Amateur radio. The cellular networks like 0G, 1G, 2G, 3G, 4G and future wireless networks like 5G can make use of the proposed co-processor.
- The standard-cell-library designed using the proposed architecture will be more compact and have more number of layouts. The fabrication technique will be more effective. At present, standards-cell-library used is of 0.16 nm, which can be improved to pico-metre range.
- As the gate count increases, number of instructions executed in one cycle increases and in turn increases the switching speed. The gate count used is 40,000 which can be increased in future.
- The increase in the number of trellis butterfly calculations per cycle will reduce the forward error correction time at a faster rate in convolutional encoding and Viterbi decoding. In the proposed design, the number of trellis butterfly calculations per cycle is three which can be further increased.