Chapter 4

A novel Capacitor Array based Digital to Analog Converter

We present a novel capacitor array digital to analog converter (DAC) architecture. This DAC architecture replaces the large MSB (Most Significant Bit) capacitor of the conventional capacitor array DAC with 3 unit capacitors, thus reducing the area, power dissipation and the settling time. The novel DAC does not demand an additional reference voltage, nor an additional switching circuit. The architecture is verified by drawing a layout and doing post layout simulations using a CADENCE UMC180 technology. An 8-bit DAC with this architecture occupies 26 $\mu m^2$ area, consumes 6.34 $nW$ at 3 V and has a settling time of 69 ns, which makes it smaller, faster, and less power consuming than a conventional capacitor array DAC. In UMC 180 nm technology, there are built-in NMOS(nmos3V) and PMOS(pmos3V) devices which can be operated at 3 V. This work employs those devices.

The new architecture is shown in Fig 4.1. A conventional capacitor array DAC uses a total capacitance of $2^nC_0$ for converting an n bit digital input into its equivalent analog value, where $C_0$ is the unit capacitance value. The new architecture uses only $2^{n-1}C_0$ for converting an n-bit digital input, and additional $3C_0$ capacitors. Thus the saving in the capacitance is $2^{n-1}C_0 - 3C_0$. For large n, this amounts to a significant saving in chip area. Also, since the settling time of the DAC is proportional to the largest capacitance used, the settling time of the proposed architecture is also reduced. The power consumption of the DAC depends upon the switching schemes used [29]. The switching schemes employed in conventional architectures can be used for this new architecture. Since the power consumption is directly proportional to the total capacitance, power consumption in this architecture is less than the conventional DAC architecture, for any given switching scheme. Moreover, in this architecture, the LSB switches from GND to a value less than VDD, hence the
switching power will be less than the corresponding switching in conventional circuit. For a higher number of bits, the saving in power, area and settling time are also higher. In a conventional architecture, optimization is done by changing the switching schemes, which require more clock phases and switches and thus increase the area and reduce speed. Since the new architecture uses a conventional switching scheme, there is no sacrifice in either area or speed. If we employ the other switching schemes in this architecture, power consumption can be reduced further.

4.1 Working Principle

This section explains the difference between the conventional capacitor array DAC and the novel architecture, and also explains how the $3C_0$ capacitors replace the MSB capacitor. In an n-bit conventional capacitor array DAC, which requires $2^nC_0$, whenever an input bit is 1, the corresponding capacitor’s bottom plate would be connected to $V_{ref}$ and all other capacitors would be connected to ground. The difference between an n bit and (n-1) bit DAC in terms of output voltages is that an (n-1) bit DAC generates voltages in the range of $\frac{mV_{ref}}{2^{n-1}}$, where $m = 0, 1, 2, ..., n-2$, whereas the n-bit DAC generates voltages in the range of $\frac{mV_{ref}}{2^n}$, where $m = 0, 1, 2, ..., n-1$. So the output voltage of an
(n-1) bit DAC is a subset of the output of an n bit DAC. Hence instead of an n-bit DAC with the LSB as zero, we could use an (n-1) bit DAC by ignoring the LSB bit. For example, for a 4-bit DAC the output voltages for the input sequence of 0000 to 1111 are 0, \( \frac{V_{ref}}{16} \), \( \frac{2V_{ref}}{16} \), \( \frac{3V_{ref}}{16} \), \( \frac{4V_{ref}}{16} \), \ldots, \( \frac{15V_{ref}}{16} \), whereas the output voltages for a 3-bit DAC, for the input sequence 000 to 111 are 0, \( \frac{V_{ref}}{8} \), \( \frac{2V_{ref}}{8} \), \( \ldots \), \( \frac{7V_{ref}}{16} \). Half the number of output voltages of a 4-bit DAC (like \( \frac{2V_{ref}}{16} = \frac{V_{ref}}{8} \), and \( \frac{4V_{ref}}{16} = \frac{2V_{ref}}{8} \)) could be generated using a 3-bit DAC.

In such a scheme, when LSB = 1, we need extra capacitors to generate the other n/2 outputs. In a conventional capacitor array DAC the MSB capacitor does this job. In the novel architecture we use 3 unit capacitors to generate those outputs. The working principle of the novel DAC can be explained as follows.

During the sampling phase, the bottom plates of all the capacitors are connected to \( V_{in} \) and the top plates are connected to \( V_{mid} \). The voltage across the capacitors then is

\[
V_x = V_{mid} - V_{in} \tag{4.1}
\]

During this phase, switch \( S_d \) is ON and \( S_{d1} \) is OFF (see Fig. 4.1). When the LSB bit is high and all other bits are low, switches \( S_{d1} \) and \( S_d \) are both on and the last two unit capacitors are connected to \( V_1 \). The equivalent circuit is as shown in Fig. 4.2. The corresponding analog output will be
\[ V_x = V_{\text{mid}} - V_{\text{in}} + \frac{(2m + lm + l)}{2(m + l + k) + l(m + k)} V_{\text{ref}} \]  

(4.2)

where \( m \) is the sum of capacitances connected to \( V_{\text{ref}} \), and is given as

\[ m = 2^{n-2} D_{n-1} + 2^{n-3} D_{n-2} + \cdots + D_1 \]  

(4.3)

\( k \) is the sum of capacitances connected to ground:

\[ k = 2^{n-2} \bar{D}_{n-1} + 2^{n-3} \bar{D}_{n-2} + \cdots + \bar{D}_1 + \bar{D}_0 S_d \]  

(4.4)

and

\[ l = D_0 + D_0 S_d \]  

(4.5)

where \( n \) is the number of bits, \( D_{n-1} \ldots D_0 \) are the digital inputs, \( \bar{D}_{n-1} \ldots \bar{D}_0 \) are their complements, and \( S_d \) is 1 when the switch \( S_d \) is closed, and it is zero when the switch is open. By substituting the values of \( l,m,k \), equation (4.2) can be reduced to

\[ V_x = \left( \frac{2^{n-2} D_{n-1} + 2^{n-3} D_{n-2} + \cdots + D_1}{2^{n-1}} + \frac{D_0}{2^{n-1}(1 + D_0)} \right) V_{\text{ref}} \]  

(4.6)

Note that switches \( S_d \) and \( S_{d1} \), are controlled by \( D_0 \). Switch \( S_d \) provides an extra capacitance, necessary when the \( \text{LSB} \) is \( \text{HIGH} \). Switch \( S_d \) takes care that the node \( V_1 \) is charged accordingly. For example, if the input bit sequence is 1010, then \( l = 0 \), and \( V_x = V_{\text{mid}} - V_{\text{in}} + \frac{m}{m+k} V_{\text{ref}} = V_{\text{mid}} - V_{\text{in}} + \frac{8}{5} V_{\text{ref}} \), which is the output for a conventional 3-bit DAC with input bits as 101. When the input is 1011, the equivalent circuit would be as shown in Fig. 4.3. For which \( l = 1 \) and

\[ V_x = V_{\text{mid}} - V_{\text{in}} + \frac{(2m + lm + l)}{2(m + l + k) + l(m + k)} V_{\text{ref}} = V_{\text{mid}} - V_{\text{in}} + \frac{11}{10} V_{\text{ref}}. \]

As the above discussion explains, \( V_x \) in Fig 4.1 is the analog equivalent voltage of the digital input signal, thus demonstrating that this circuit is, in fact, a digital-to-analog converter.

### 4.2 Simulation results

The circuit was laid out and simulated in a 180nm technology, with a \( V_{DD} \) of 3 V and a unit capacitor of 100 \( fF \). The layout for an 8-bit DAC is shown in Fig 4.3. Post-layout simulation results are shown in Fig 4.4: A monotonically decreasing digital bit sequence was applied, and the analog output plotted as a function of time.

The magnified version of the simulation results with trace markers is shown in Fig 4.6. From the
trace markers, it is evident that the step sizes are uniform and their value is $V_{DD}/2^8$.

This 8-bit DAC architecture occupies 26 $\mu m^2$ area, consumes 6.42 $nW$ at 3 V and has a settling time of 69 $ns$ as opposed to 51 $\mu m^2$, 11.8 $nW$ and 136 $ns$ with a conventional DAC architecture with single step switching [31].

The simulated differential non-linearity (DNL) and integral non-linearity (INL) versus input codes are shown in Fig 4.7 and Fig 4.8, respectively. It can be seen that both INL and DNL are smaller than 0.68 LSB for the entire range of the input code.

The dynamic characteristics of the proposed DAC is shown in Fig 4.9. For measuring the dynamic characteristics such as Signal to Noise Ratio (SNR), Spurious Free Dynamic Range (SFDR) and Signal to Noise And Distortion (SINAD), an output from an 8-bit ADC is given as the input. SNR and SFDR were simulated with a 240 Hz input sine wave. The corresponding SNR and SFDR were 48.1 dB and 52.3 dB.

### 4.3 Comparison with conventional DAC for different switching schemes

Table 4.1 shows a comparison of the novel architecture with conventional DACs for power, area and settling time, with different switching schemes discussed in [32]. In the table, $a_{sw}$ is the area of switch and $t_{sw}$ is the switching time for a single transition. The first four rows in the table show the conventional architecture with different switching schemes, employed for reducing...
Figure 4.4: Layout of novel DAC Architecture.

Figure 4.5: Post Layout Simulation results.
Figure 4.6: Magnified version of simulation results.

Figure 4.7: Simulated INL versus input codes.
Figure 4.8: Simulated DNL versus input codes.

Figure 4.9: Simulated dynamic performance vs. input.
power dissipation. The last row of the table shows the power dissipation, area and speed of the new architecture. The table clearly shows that the new architecture reduces power, area, as well as settling time.

A conventional single step switching has been used with the novel architecture. Other switching methods have not been tested with this architecture. Employing other switching methods may improve its performance further.
4.4 Comparison with the Existing capacitor Array DAC Architectures

Three architectures, namely Conventional Binary Weighted Capacitive Array (CBW), Binary Weighted Capacitive Array with attenuation Capacitor (BWA) and Split Binary Weighted Capacitive Array (SBW), taken from [ref 1] are compared with the proposed architecture. To have a better comparison between the architectures, the value of the average power consumption, maximum standard deviations of the INL and DNL, and the total capacitance required for each architecture are summarized in table.

Standard deviation of INL and DNL for the proposed architecture is calculated using [30] and [47].

<table>
<thead>
<tr>
<th>Architectures</th>
<th>Average Power</th>
<th>Standard Deviation of INL</th>
<th>Standard Deviation of DNL</th>
<th>Total capacitance required</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBW</td>
<td>$0.662^N\frac{f_{clk}C_0V_{ref}^2}{N+1}$</td>
<td>$\left(2^\frac{N}{2} - 1\right) \frac{\sigma_0}{C_0}$</td>
<td>$\left(2^\frac{N}{2}\right) \frac{\sigma_0}{C_0}$</td>
<td>$2^N C_0$</td>
</tr>
<tr>
<td>BWA</td>
<td>$1.252^N/2\frac{f_{clk}C_0V_{ref}^2}{N+1}$</td>
<td>$\left(2^{\frac{3N}{4}} - 1\right) \frac{\sigma_0}{C_0}$</td>
<td>$\left(2^{\frac{3N}{4}}\right) \frac{\sigma_0}{C_0}$</td>
<td>$2^{N/2} C_0$</td>
</tr>
<tr>
<td>SBW</td>
<td>$0.412^N\frac{f_{clk}C_0V_{ref}^2}{N+1}$</td>
<td>$\left(2^\frac{N}{2} - 1\right) \frac{\sigma_0}{C_0}$</td>
<td>$\left(2^\frac{N}{2}\right) \frac{\sigma_0}{\sqrt{2}C_0}$</td>
<td>$2^N C_0$</td>
</tr>
<tr>
<td>Proposed DAC</td>
<td>$0.59 \left(2^{(N-1)} + 3\right) \frac{f_{clk}C_0V_{ref}^2}{N+1}$</td>
<td>$\approx \left(2^\frac{N}{2} - 1\right) \frac{\sigma_0}{C_0}$</td>
<td>$\approx \left(2^\frac{N}{2}\right) \frac{\sigma_0}{C_0}$</td>
<td>$(2^{N-1} + 3)C_0$</td>
</tr>
</tbody>
</table>

Table 4.2: Comparison between the conventional architectures and the novel architecture

4.4.1 Derivation For Standard deviation of Integral Non-linearity (INL) and Differential Non-linearity (DNL)

For calculating the linearity characteristics of the proposed scheme, each of the capacitor is modeled as the sum of the nominal capacitance plus the error.

\[
C_n = 2^{n-2}C_0 + \delta_n
\]  
(4.7)

\[
C_{n-1} = 2^{n-3}C_0 + \delta_{n-1}
\]  
(4.8)

\[
C_0 = C_0 + \delta_0
\]  
(4.9)
The error term $\delta_n$ has zero mean and a standard deviation of

$$E[\delta_n^2] = 2^{n-2} \sigma_0^2$$

(4.10)

If there are no initial charges, then $V_x$ can be expressed as

$$V_x = \left( \sum_{n=1}^{b-1} \frac{(2^{(n-2)}C_0 + \delta_n)D_n}{2^{(b-1)}C_0} + \frac{(C_0 + \delta_0)D_0}{2^{(b-1)}(C_0 + (C_0 + \delta_0)D_0)} \right) V_{ref}$$

(4.11)

Subtracting the nominal value yields the error term

$$V_{error} = \left( \sum_{n=1}^{b-1} \frac{\delta_n D_n}{2^{(b-1)}C_0} + \frac{(C_0 + \delta_0)D_0}{2^{(b-1)}(C_0 + (C_0 + \delta_0)D_0)} \right) V_{ref}$$

(4.12)

which can be approximated as

$$V_{error} = \left( \sum_{n=1}^{b-1} \frac{\delta_n D_n}{2^{(b-1)}C_0} + \frac{(C_0 + \delta_0)D_0}{2^{(b)}C_0} \right) V_{ref}$$

(4.13)

which can be written as

$$V_{error} = \left( \sum_{n=1}^{b} \frac{(\delta_n)D_n}{2^{(b)}C_0} \right) V_{ref}$$

(4.14)

with variance

$$E[V_{error}^2(y)] = \frac{y}{2^{2b}} \frac{\sigma_0^2}{C_0^2} V_{ref}^2$$

(4.15)

From that the worst case INL can be derived as

$$\sigma_{INL} = 2^{(b/2)-1} \frac{\sigma_0}{C_0} LSB$$

(4.16)

and the worst case DNL be

$$\sigma_{DNL} = 2^{(b/2)} \frac{\sigma_0}{C_0} LSB$$

(4.17)

The novel architecture can also be a part of split capacitor array dac, so that the savings in capacitor improves further compared with the normal split capacitor array dac. For example, an 8 bit digital to analog converter with binary weighted capacitor array would require 256 unit capacitors, whereas a split capacitor array would require 31 unit capacitors. If we employ the proposed novel architecture in the split capacitor array, the resultant architecture requires 22 unit capacitors. Fig 4.10, fig 4.11 and fig 4.12 explain the above mentioned concepts. From fig 4.10 it is evident that it requires 31 unit capacitors to implement an 8-bit Digital to Analog converter. Fig 4.11 shows the same
Figure 4.10: Split-capacitor array DAC and its simulation
Figure 4.11: Split-Capacitor DAC with proposed Scheme on LSB sub-DAC and its simulation
8-bit digital to analog conversion, but uses only 26 unit capacitor. It employs the proposed DAC architecture for its LSB sub-DAC. The simulation results show that both the architectures behave in the same way. Fig 4.12 shows the 8-bit conversion with 21 unit capacitors and it employs the proposed architecture for both the LSB and MSB sub-DACs.

4.5 Design Considerations

In this section we consider the effects of Capacitor parasitics and Capacitor mismatches.

4.5.1 Capacitor Parasitics

Case 1 : A Parasitic Capacitance \( (C_p) \) at \( V_1 \), would result in the following circuit. Using the Star-Delta conversion an equivalent would be generated as shown in fig 4.13.

Where

\[
C_1 = \frac{mC_0 + mlC_0 + lC_0}{l} \\
C_2 = \frac{mC_0 + mlC_0 + lC_0}{m}
\]
Figure 4.13: Generalized equivalent circuit with parasitic capacitance.

Figure 4.14: Equivalent circuit with a Delta-Star conversion

\[ C_3 = mC_0 + mlC_0 + lC_0 \]  
(4.20)

From Fig 4.14, with equations (4.18), (4.19) and (4.20), \( V_1 \) can be written as

\[ V_1 = \frac{V_{ref}C_1}{C_1 + \frac{C_2C_0}{C_2+C_0} + C_p + \frac{C_3C_0}{C_3+C_0}} \]  
(4.21)

while substituting (4.18), (4.19) and (4.20) in equation (4.21)

\[ V_1 = \frac{V_{ref} \left( mC_0+mlC_0+lC_0 \right)}{\left( mC_0+mlC_0+lC_0 \right) + \left( \frac{mC_0+mlC_0+lC_0}{m} \right)C_0 + C_p + \frac{(mC_0+mlC_0+lC_0)C_0}{(mC_0+mlC_0+lC_0)+C_0}} \]  
(4.22)
Node voltage $V_x$ can be written as

$$V_x = \left( \frac{m + ml + l}{m + ml + l + 1} \right) V_1$$  \hspace{1cm} (4.23)

$V_x$ can be written as in (4.24), while substituting (4.22) in (4.21)

$$V_x = \left( \frac{m + ml + l}{m + ml + l + 1} \right) \left( \frac{mC_0 + mlC_0 + lC_0}{l} \right) + \left( \frac{mC_0 + mlC_0 + lC_0}{m} \right) C_0 + C_p + \left( \frac{mC_0 + mlC_0 + lC_0}{m} \right) C_0 \left( \frac{mC_0 + mlC_0 + lC_0}{l} \right)$$

(4.24)

The following example would illustrate the effect of $C_p$ at $V_x$.

Consider a bit pattern of "11101" for a 5-bit digital to analog conversion with $m = 14$, $l=2$. Now $V_x$ can be calculated as

$$V_x = \left( \frac{1276C_0}{1408C_0 + 58C_p} \right) V_{ref}$$  \hspace{1cm} (4.25)

$$V_x = \left( \frac{29C_0}{32C_0 + 1.3C_p} \right) V_{ref}$$  \hspace{1cm} (4.26)

For the next bit pattern "11110"

$$V_x = \frac{15}{16} V_{ref}$$  \hspace{1cm} (4.27)

The difference in these two generated voltages is

$$V_{x1} - V_{x2} = \frac{15}{16} V_{ref} - \left( \frac{29C_0}{32C_0 + 1.3C_p} \right) V_{ref}$$  \hspace{1cm} (4.28)

In the above equation, if $C_p = 0$, then the difference is $(1/32)V_{ref}$ which is $V_{ref}/2^n$. If $C_p/C_0 = 0.5$ then the difference in two consecutive generated voltages is $(1/22)V_{ref}$ which is well within 0.5 LSB. This explanation shows that the Parasitic capacitance at $V_1$ will not affect the static characteristics of the proposed DAC.

Case 2 : If there is an additional parasitic capacitance from $V_{DD}$ to $V_1$: The generalized equivalent diagram would be as shown in fig 4.15. The generalized voltage at $V_x$ is

$$V_x = \left( \frac{m(C_0 + C_p) + ml(C_0 + C_p) + lC_0}{m(C_p + C_0) + ml(C_p + C_0) + lC_0 + C_0} \right) V_{ref} \left( \frac{mC_0 + mlC_0 + lC_0}{lC_0} \right) + \left( \frac{mC_0 + mlC_0 + lC_0}{mC_0 + C_0} \right) C_0 + C_p + \left( \frac{mC_0 + mlC_0 + lC_0}{mC_0 + mlC_0 + lC_0 + C_0} \right) C_0$$

(4.29)
For a five bit digital to analog conversion, with a bit pattern of "11101", \( m = 14 \), \( l=2 \) and for \( (C_p/C_0) = 0.5 \). From these values \( V_x \) can be calculated as

\[
V_{x1} = \frac{29.33}{32} V_{ref}
\]

For "11110", \( V_x \) can be generated as

\[
V_{x2} = \frac{15}{16} V_{ref}
\]

The difference between the two subsequently generated voltage is

\[
V_{x2} - V_{x1} = \frac{0.67}{32} V_{ref}
\]

Which is well within 0.5LSB.

Fig. 4.16 and 4.17 plots the impact of \( C_p \) on DAC linearity for an 8-bit DAC. The peak-to-peak INL of the DAC is plotted against the ratio \( C_p/C_u \) and the corresponding DNL and INL plots for when \( C_p/C_u \) is 0.1 and 0.5 are also plotted. As the plots show, in order to get an INL below +/-0.5 LSB, the unit capacitance, \( C_0 \), should be about 2x larger than the parasitic cap at the output node.

### 4.5.2 Capacitor mismatches

The novel architecture employs 3 additional capacitances, which are the same as the unit capacitance. So the required matching ratio compared with the unit capacitor is 1:1. This makes the
Figure 4.16: DNL for capacitor parasitics

Figure 4.17: INL for capacitor parasitics
design less prone to capacitance mismatches. The impact of these random variations is captured in Fig. 4.18 which plots the INL of an 8-bit DAC for $3\sigma C_0$ variation of 5%. As the plot shows, the DAC shows a fairly muted response even to significantly large random per unit capacitor variations.

![INL for randomly mismatched capacitor](image)

**Figure 4.18:** INL for randomly mismatched capacitor