CHAPTER 7

CONCLUSION AND SCOPE FOR FUTURE WORK

7.1 CONCLUSION

In this thesis, several kinds of high performance VLSI architecture required for digital signal processing are proposed, implemented and compared with the existing methods. The variable precision two-dimensional fine grain pipelining is illustrated by designing a multiplier for FIR filter. Comparison of the results with the existing techniques makes it clear that the proposed method reduces the power consumption by 18% with 3% additional area.

The second method, called data transition power diminution technique has been applied on adders, multipliers and FIR filter to reduce the power consumption. The proposed FIR filter using Booth multiplier with DPDT has been implemented in Xilinx Spartan 3E FPGA. There is a decrease in power consumption, area and delay by 31%, 17.9% and 3% respectively, when compared to the existing FIR filter using Booth multiplier with DRD unit.

The third approach deals with an asynchronous pipelined FIR filter which is built using RSPCHB QDI Template. It has the advantage of high speed and low latency. The asynchronous design provides 12 times higher speed with 8 times reduced latency and 2 times increased area when compared with synchronous design.
The fourth method of analog CMOS FIR Filter implementation reduces the power consumption and area of the FIR filter. The average power consumption of digital implementation amounts to 900mW. The switched capacitor implementation consumes 63mW whereas the proposed system consumes only 23mW. In all these proposed methods, there is a considerable improvement in the performance of VLSI architecture.

After analyzing different techniques, it has been established that the analog CMOS implementation of DSP algorithm is advantageous in terms of power consumption and utilization area for low frequency applications like voice processing. For high frequency signal processing applications, the asynchronous implementation using RSPCHB QDI template is suitable since it gives more or less 12 times higher speed than the synchronous design. For maximum speed with minimum power, the variable precision two-dimensional fine grain pipelining technique can be preferred. Designing low power System-on-Chip (SoC) for multi-media applications where the signal correlations are very less, the DPDT is a better method. As DSP continues to make a major impact in many key areas of technology, the proposed methods have vast opportunities for expansion.

7.2 SCOPE FOR FUTURE WORK

The variable precision two-dimensional pipeline gating technique may be incorporated in asynchronous pipeline; this may further reduce the power consumption of the DSP ICs with higher clock frequency. This technique can be thought of for mobile communication devices. Further, the analog implementation technique may be improved by adding analog memory cells to store the analog values directly. This will completely remove the digital subsystem required for DSP applications and reduce the gate density of the circuit considerably.