CHAPTER 6

CONCLUSIONS

6.1 THE PRESENT STUDY

Power consumption is one major factor which almost every consumer cares about in both wall-powered and battery-powered devices. In today’s competitive market, designing a product which consumes higher power or which costs more competitive products can result in reduced market success.

When optimizing, power consumption is a major criterion. Designers should look at critical parameters like choosing the appropriate components and making sure that they are not overrated for the desired end application, as well as making sure that the system does not operate at higher speeds than that are required. In addition, developers want to seriously consider how long the system spends in active and standby modes and the relative power consumption in each.

With the arrival of deep-submicron technologies, leakage loss is a most important concern for scaling down portable devices that have burst-mode type integrated circuits. Leakage drains the battery, even when a circuit is completely idle. In this dissertation, a sleep controlled and self-controlled leakage reduction techniques have been developed for CMOS VLSI circuits. A three transistor based logic gates have been developed for power hungry
SOC applications. In this chapter, a summary of contributions of this work and suggestions and pointers for future work are presented.

The main contributions of this research are presented:

- **Design of Sleepy-pass gate and DT-LECTOR for logic circuits**: Two new low-leakage techniques “Sleepy-pass gate and “D1-LECTOR” are developed in this research work. These techniques are applied to generic CMOS logic circuits and benchmark circuits and achieved between two to three orders of magnitude leakage power reduction compared to the best prior state saving technique.

- **Design of a new 3T based logic gates**: A new set of low power three transistor (3T) based logic gates such as OR, AND, NAND and NOR to reduce dynamic power with reduced area and high speed is designed. According to HSPICE simulation in 22 nm CMOS process technology at room temperature, and under given conditions, the proposed 3T gates shows an improvement of 88% less power consumption on an average over conventional CMOS logic gates. The devices designed with 3T gates will make longer battery life by ensuring extremely low power consumption.

- **Design of a D-Latch using 3T NAND gate**: D-Latch is a power hungry component in a VLSI chip. Therefore, the 3T NAND gate is applied to design D-Latch. Since the new universal gates comes with less area and delay penalties, many possible D-Latch circuit combinations are explored for comparisons. Also provided new Pareto points that can be used by designers who want extremely low leakage power
consumption (and are not willing to pay a cost of some area and/or delay increase).

6.2 SCOPE FOR FUTURE WORK

The proposed two leakage reduction techniques and three transistor based logic gates are new low power techniques. Although much theoretical and simulation research done on it, much detailed design work has to be done to make it more easily and effectively usable in practical ASIC and SoC designs. The following are possible future work:

- Study the Effects of Gate Leakage: The primary goal of this dissertation work was to invent techniques to minimize subthreshold leakage. However, the gate leakage problem poses a significant design challenge for sub-100 nm CMOS technologies. The effects of the gate leakage component of power dissipation could be studied and augmented to provide a complete leakage minimization package.

- Investigation of Leakage Reduction Techniques at Higher Levels of Abstraction: The investigation of leakage reduction techniques at the behavioral level or even system level of abstraction would be an interesting topic for further in-depth research. The effect of noise on various gates with proposed techniques and its corresponding conventional gates could be studied.

- Investigation on n-input logic gate: Investigate on more than 2 input OR, AND, NAND and NOR logic gates with reduced transistor count could be analyzed and developed along with noise analysis.