APPENDIX 1

FPGA IMPLEMENTATION

The proposed four methods are simulated in Model Sim and implemented in Field Programmable Gate Array. RTL view of the GLFSR (BP), GLFSR (BP & BS), GLFSR (BP & BI) and GLFSR (BP, BS & BI) are represented in Appendix.

The following Figures A1.1, Figure A1.2 indicates the Main and Internal RTL view of GLFSR Bipartite Technique.

Figure A1.1 Main RTL View of the GLFSR Bipartite Technique
Figure A1.2 Internal RTL View of the GLFSR Bipartite Technique

The following Figures A1.3, A1.4 points the Main and Internal RTL view of GLFSR Bipartite Bit Swapping Technique.

Figure A1.3 Main RTL View of the GLFSR Bipartite Bit Swapping Technique
Figure A1.4 Internal RTL view of GLFSR Bipartite Bit Swapping Technique

The following Figures A1.5, A1.6 specifies the Main and Internal RTL view of GLFSR Bipartite Bit Insertion Technique.

Figure A1.5 Main RTL view of GLFSR Bipartite Bit Insertion Technique
Figure A1.6 Internal RTL View of the GLFSR Bipartite Bit Insertion Technique
The Subsequent Figures A1.7, A1.8 designates the Main and Internal RTL view of GLFSR Bipartite Bit Insertion and Swapping Technique.

Figure A1.7 Main RTL view of GLFSR Bipartite Bit Insertion and Swapping Technique
Figure A1.8 Internal RTL view of GLFSR Bipartite Bit Insertion and Swapping Technique