Chapter 7

Conclusion

and

Future Scope
This chapter summarizes the work done in the thesis and makes certain conclusions. It may be mentioned that some of the results agree with the work done earlier by other research groups, as referred in chapters 3, 4, 5 and 6, but other results demand new explanations. In certain cases further search is needed to give a definite conclusion and finally there are a few situations where the investigations can be extended to another level. However, all these do not come under the purview of the present study, but are mentioned in this chapter appropriately.

Electrical characterization of prepared Heterojunction diodes in the present investigation is the main objective of this thesis. In this context various barrier parameters of Heterojunction diode and finally current transport mechanisms were studied. Besides, structural, optical and electrical characterizations were made on Nanocrystalline thin films of p-SnSe to assess the film parameters for their suitability required for device preparation.

7.1 Final Remarks

Considering the importance of group IV-VI in various electronic applications as described in chapter 1, author has chosen to grow Nanocrystalline p-SnSe in thin film form which is a member of this group for its structural, optical and electrical properties and its use in Heterojunction devices.

In this present study structural, optical and electrical properties of prepared Nanocrystalline thin of p-SnSe having different thicknesses and annealing temperature have been studied. These prepared thin films were used to prepare Heterojunction diode with n-MoSe₂ crystal.

As discussed in chapter 2 Nanocrystalline thin films of p-SnSe were prepared by various techniques. Among these techniques spin
coating method was chosen for this films and device preparation. It is concluded from the EDAX results that the spin coating method yields in to relatively good quality thin films with good stoichiometry. The deposited thin films were then characterized for their structural and microscopic properties using XRD, TEM, SEM and AFM.

Structural studies by XRD and ED pattern indicated the polycrystalline nature of the films. The data are in good agreement with JCPDS file with their respective code. The grain sizes of deposited films were found to be 10.80nm to 17.54nm for all thin films. These obtained grain size is small comparison to the Bohr radius of this material so we can say that our deposited thin films are in the Nano forms. It is further found that all the deposited films posses Orthorhomic structure and calculated lattice parameters are in good agreement with the reported values. From XRD spectra of deposited films, the strain and dislocation density of the prepared films were calculated and these values were found to be decreasing with increase in film thickness and annealing temperature. The topography of the surfaces of the prepared thin films was studied using the SEM micrographs for all thin films. The films were found to be continuous on the glass substrates and the films deposited with higher thickness were uniform with minor cracks. AFM photographs also show the structural improvement with film thickness and annealing temperature. Optical absorption study of deposited thin films were made in the wavelength range 200–2500nm. It is revealed that the direct allowed transition of charges due to strong absorption has been found as a dominant carrier transition mechanism. The values of optical band gap for all deposited thin films decrease with increase in thickness and annealing temperature of thin film. Further, the value of refractive index is also calculated for all deposited thin films.

Electrical properties of deposited thin films have been studied using three methods viz. high temperature resistivity, thermoelectric
power measurement with fixed temperature gradient and high temperature dielectric measurements. Room temperature I – V characteristics show the ohmic nature of steel pressure contacts with all deposited thin films. In extrinsic conductivity region activation energy for different temperature interval was evaluated. While in intrinsic conductivity region electrical band gap of deposited thin films was determined and possible reason for the deviation of electrical band gap compared to optical band gap has been discussed in detail in chapter 5. The positive sign of Seebeck coefficient confirms the p type nature of all deposited thin films. The increasing nature of resistance with fall in temperature and increasing nature of Seebeck coefficient with rise in temperature show the typical nature of semiconductor. Using thermoelectric power measurement Fermi energy has been obtained. Finally, it is found that the thickness and annealing temperature dependent structural changes are reflected in electrical properties of deposited films.

Looking toward the electrical properties of thin films, it is then decided to fabricate Heterojunction diodes by depositing p-SnSe thin films on to cleaved n-MoSe₂ crystals. I–V characteristics of these diodes have been observed in the temperature range 290-390K. From the detailed and careful analysis of observed I – V characteristics following conclusions have been drawn. All the Heterojunction exhibit fairly good rectification properties. The values of parameters like barrier height and ideality factor for each diode were determined over a wide range of temperatures. Other important junction parameters e.g. ‘A*’, ‘o0’, ‘o5’, ‘P₂’ and ‘P₃’, percentage of inhomegenitites etc. were also determined for diode. It has been observed that the ideality factor increases with decrease in temperature for all diodes. On the other hand, the zero bias barrier height decreases with decrease in temperature. The ideality factor is simply a manifestation of the barrier uniformity and it increases for an
inhomogeneous barrier. An apparent increase in ideality factor and decrease in BH at low temperature are possibly caused by inhomogeneities of thickness and composition of the layer, non uniformity of the interfacial charges. Since the current transport across the interface is a temperature activated process, at low temperature the current will be dominated by the current through the patches of low barrier height. Therefore at low temperature, electrons are able to overcome the lower barriers, and hence current transport will be dominated by current flowing through the patches of lower BH and result into a larger ideality factor. As the temperature increases, more and more electrons have sufficient energy to overcome the higher barriers. As a result both BH and $\eta$ are strongly dependent on temperature. We can also see that the percentage of inhomogeneity in all diodes is around 29\%. It is due to the non uniform surface of MoSe$_2$ as well as formation of junction of two different types of semiconductros (i.e. bulk n-MoSe$_2$ and Nano p-SnSe thin films). The calculated Richardson constant and modified Richardson constant are found to be in good agreement with reported values. Capacitance-Voltage method is very important method to evaluated Heterojunction parameters such as $V_D$, $\Delta E_c$ and $\Delta E_v$ so in the present investigation we measured C-V characteristics at room temperature and analyzed this data to evaluated such parameters. Using this an energy level location in band diagram of all prepared Hetrojunction were done using C-V analysis.

7.2 Future Direction

The main aim of present thesis is to investigate various properties of Nanocrystalline thin films of p-SnSe and its application as a Heterojunction diode material. The notable investigations on thickness and annealing temperature dependent properties of SnSe thin films grown successfully by spin coating technique and that on Heterojunction devices have been chapterized in the present thesis. However, the
outcome of the present research efforts has opened new directions of further studies in future. Following is a brief note on important outcome which leads to scope for future work.

➢ Since spin coating technique is well known for depositing a good quality and pure thin films, it is difficult to deposit on large area substrate uniformly with controlled rate of deposition.

➢ Also obtaining smooth surface of the deposited film of a compound semiconductor is probably a challenging task in the case of spin coating technique.

➢ To reduce and avoid the above mentioned limitations, one can use other deposition techniques like thermal evaporation, RF sputtering, Magnetron sputtering etc. to deposit smooth coverage of large area substrate surface by thin films.

➢ In present investigation various properties of deposited thin films and devices were examined as an effect of film thickness and annealing temperature successfully. It will be investigated to study them with variation of rpm on it. Prepared Heterojunction diodes have been characterized with I - V – T method to evaluate their barrier parameters using thermionic model with assumption of Gaussian distribution of barrier height at the junction of devices. However 1st order Gaussian distribution has been applied to estimate the barrier parameters of prepared diodes. One can apply at-least 2nd order Gaussian distribution to evaluate the barrier parameter in order to evaluate barrier parameters close to their realistic values.

➢ It is also interesting to develop such structure by using Nanowire and Nanosheet forms.

➢ In this work Nanocrystalline p-SnSe thin film Heterojunction junctions with bulk n-Mose₂ crystals are studied. As this system of Nanocrystalline thin film-bulk crystal is less studied. It will be further interested to study the effect of band gap of bulk
semiconductor crystal by choosing another n-type crystal instead of n-MoSe₂.

- Also Heterojunction using both semiconductor in Nanocrystalline thin film forms open a new interesting field in Nano electronics.
- MESFETs and MOSFETs as well as a solar cell are interested and important devices to be explored by using this structure.
PUBLICATIONS


Appendix - II

RESEARCH PAPERS PRESENTED AT CONFERENCES / WORKSHOP / SYMPOSIUM

1. “Current-Voltage characteristics and barrier parameters of Al/CdS Schottky diodes in a wide temperature range”

2. “Chemical, structural and optical properties of SnSe crystal”


4. “Structural, Optical And Dielectric Properties Of Tin Selenide Nanoparticles Prepared By Aqueous Solution Method”
CONFERENCES/ WORKSHOPS ATTENDED


3. XXIV- Gujarat Science Congress-2010 “Science and Technology for better environment” held at Gujarat University Ahmadabad (Gujarat), on 21th March-2010.


5. “One day seminar on innovation in collegiate Science education and Research” held at V. P. & R. P. T. P. Science College, Sardar Patel University, Vallabh Vidyanagar -388 120 (Gujarat), on 8th January-2011.

6. “One day seminar on Condensed matter physics with Nano flavors” organized by Department of Physics, Sardar Patel University, Vallabh Vidyanagar -388 120 (Gujarat), on 4th February-2011.


8. “Semiconductor devices and nano materials characterization – A technical seminar” in Department of Physics, Sardar Patel University, Vallabh Vidyanagar -388 120 (Gujarat), on 7th July-2011.

9. “One day seminar on Nuclear technology for raising standard of living” oaganized by Department of Physics, Sardar Patel University, Vallabh Vidyanagar - 388 120 (Gujarat), on 11th September- 2011.

10. “National conference on recent trends in material science (RTMS-2011)” organized by Jaypee University of Information Technology,
Waknaghat, Solan (Himachal Pradesh), during (8 – 10) October-2011.

