Chapter 6

Fabrication of p-SnSe/n-MoSe₂
Hetrojunction Diode
and
its I-V-T and C-V Characteristics.
6.1 Literature Survey on Heterojunction

A Heterojunction is formed when two semiconductors, of different band gap energies are brought together. The study of semiconductor Heterojunction is a most desired field of research for advancement of semiconductor devices and technology. In 1951, Shockley first proposed the abrupt Heterojunction to be used as an efficient emitter based junction in bipolar transistor [1]. In the same year, Gubanov published theoretical paper on Heterojunction [2]. Kroemer later analysed a similar, although graded, Heterojunction as a wide gap emitter [3]. Since then, Heterojunctions have been extensively studied, and many important applications such as room temperature injection laser, light emitter diode, photodiode and solar cell etc. have been made. In addition, by forming periodic layered Heterojunctions with layer thickness of the order of 100Å, the so called super lattice structures are obtained [4]. The Heterojunctions have been reviewed by Milnes and Feucht [5] and Sharma and Purohit [6]. Though bulk Heterojunction diode is widely used in most of the electronic circuits for different applications, the research activities and development of various thin film Heterojunctions has been in progress since last forty years. R. S. Muller and R. Zuleeg investigated the thin film Heterojunction diodes of vapor deposited CdS and other semi insulators viz, CdTe, Al₂O₃ and SiOₓ [7]. W. A. Gutierrez reported a CdSe/ZnSe thin film Heterojunction as rectifier [8]. F. A. Shallcross reported a photoconductor diode array made by CdS/CdSe thin films [9]. C. J. Moore and D. E. Brodie fabricated a ZnSe/ZnTe amorphous thin film Heterojunction by thermal evaporation method [10]. F. Pfisterer and others investigated ZnTe/CdS thin film solar cell prepared by vacuum deposition [11]. J. Touskova et. al. investigated the fundamental properties of CdS/CdTe thin film Heterojunction prepared by electrochemically depositing CdTe layer over the CdS film prepared by spray pyrolysis method [12]. Venugopal et al have grown
CdTe/ZnSe\textsubscript{x}CdS\textsubscript{1-x} Heterojunction on glass substrates by vacuum evaporation [13]. N. I. Aly et. al. fabricated a Heterojunction of amorphous GaAs thin film and n-type Si and studied the carrier transport mechanism [14]. M. Rami et. al. investigated the heating effect and CdCl\textsubscript{2} treatment on the electrodeposited CdTe/CdS Heterojunction [15]. Mridha and Basak have investigated the p-CuO/n-ZnO thin film Heterojunction prepared by sol-gel technique for H\textsubscript{2} gas sensor applications [16]. Adieovich et. al. studied the SnO\textsubscript{2}-CdS-CdTe thin film Heterojunction and investigated the structure as photodiode arrays [17].

Hema Chanda et. al. fabricated the p-AgGa\textsubscript{0.25}In\textsubscript{0.75}Se\textsubscript{2}/n-Zn\textsubscript{0.35}Cd\textsubscript{0.65}S polycrystalline thin film Heterojunction and characterized it [18]. G. C. Wary et al studied the optical and electrical properties of n-ZnO/p-CdTe Heterojunction [19]. It is seen that in the study of thin film junctions, besides the electroluminescence cell and photodiode, more emphasis is given on the photovoltaic performance of the junctions. W. D. Gill and R. H. Bube studied the photovoltaic properties of Cu\textsubscript{2}S-CdS Heterojunction [20]. Alan L. Fahrenbruch et al reported some II-VI Heterojunctions for solar energy conversion [21]. Fredrik Buch et al studied the photovoltaic properties of n-CdSe/p-ZnTe Heterojunction by depositing epitaxial film of n-CdSe on p-ZnTe crystal [22]. T. L. Chu et al obtained 13.45% efficient thin film CdS/CdTe solar cells [23]. S. N. Alamri and A. W. Brinkman studied the effect of the transparent conductive oxide on the performance of thin film CdS/CdTe solar cells [24]. H. Bayhan investigated the current transport mechanism of CdS/CdTe thin film Heterojunction solar cell prepared by thermal evaporation technique [25]. M. Purica et al studied the electrical properties of CdS/InP Heterostructure for photovoltaic applications [26].

From the above literature survey it was found that much more research efforts have been made for preparation of Heterojunctions using semiconductor materials in bulk crystalline and thin film forms. It was
also found that very few workers made effort for the preparation of Heterojunction diode by using Nanocrystalline thin films. So in the present investigation we prepared Heterojunction diode by using our Nanocrystalline thin films of p-SnSe with n-MoSe₂ crystal (p-SnSe/n-MoSe₂). Various Heterojunction diode parameters have been evaluated by studying diode’s I-V-T and C-V measurements. Hence this chapter starts with brief introduction of MoSe₂ because it is used as a semiconductor substrate material in these diodes, followed by preparation of p-SnSe/n-MoSe₂ Heterojunction diode and evaluation of various diode parameters by different standard models.

6.2 Structural, Electrical and Optical Properties of MoSe₂

Structural Properties

MoSe₂ form hexagonal layered structures. The repeating 2-D unit is a block formed by a plane of Mo atoms, in between two planes of Se as shown in figure 6.1(a). Interactions between atoms in a block are mainly covalent, while only saturated orbital’s of the Se are exposed to the exterior. Block to block interactions is 1 to 2 orders of magnitude weaker than within a block.

Figure 6.1: (a) Crystal structure of MoSe₂. (b) Lattice section along the (0001) plane, indicating the atomic positions for the abc notation, relative to the a and b crystallographic directions.
These weak interactions are generally referred to as of the van der Waals type, even though a covalent coupling is also possible [27]. Therefore cleavages along the interlayer gap (van der Waals gap) is easy, and in ideal cases, perfect dangling bond free surfaces can be obtained by peeling off few layers using a scotch tape attached to a crystal. The hexagonally close packed surfaces of the cleavage plane are for this reason called van der Waals surfaces. Since the strength of interactions is remarkably larger within the blocks, the chemical and physical properties are anisotropic and usually considered as nearly two dimensional. The Mo atom within the block is always coordinated by six Se atoms. Two geometries are possible: trigonal prismatic and trigonal antiprismatic (commonly referred to as octahedral, although distorted). The preferred coordination is determined by the bond ionicity as given by the electro negativity difference between metal and chalcogen. Octahedral coordination is preferred in more ionic compounds, since it maximizes the distance between negatively charged chalcogens. On the other hand the overlap between Mo and Se wave functions is optimized in a trigonal prismatic coordination [27], which is typically found for more covalent compounds. Due to the weak interlayer interactions, several stacking polytypes are found. The free energy of formation of the different polytypes is similar and the transition requires a low activation energy. For this reason MoSe\textsubscript{2} is also used as solid-state lubricants [28-32].

The unit cell is defined with the c axis perpendicular to the layers, and the a and b axes along the minimal Se-Se distance. In a close-packed stacking the hexagonal lattice planes can occupy one of three equivalent positions. If atoms of a plane occupy the position A (i.e. at the origin of the a-b two-dimensional unit cell, as in figure. 6.1 (b)) atoms of the next planes can occupy either position B or C. In
dependence of the contained species, each atomic plane can be indicated as A, B, C for the Se and a, b, c for the Mo, [a], [b], [c] for possible guest species. According to this notation the trigonal prismatic coordination is indicated with AbA, while the octahedral is AbC. Many possible layer stackings exist if we consider that alternated trigonal prismatic and octahedral structures are also known.

Electrical Properties

All the properties of layer materials are very anisotropic. The electron paramagnetic resonance studies by Title and Shafer (1972, 1973) [33, 34] on Nb and As acceptors in MoSe₂ established, The dz² character of the uppermost filled band extremum, thus confirming the ordering of the bands as proposed by Wilson and Yoffe (1969) [35]. However, there is now considerable evidence that the minimum indirect band gap in these semiconductors is greater than 0.3 eV, (Yoffe 1973, 1974) [36, 37] and the electrical conductivity in these materials is extrinsic at 300 K. The value of the conductivity at 300 K varies widely from sample to sample, probably due to varying impurity concentrations (Kalikhman and Umanskii 1973) [38]. At high temperatures, usually above 400-600K, intrinsic conduction has been observed with an activation energy corresponding to a bandgap of 1.4 eV (Lagrenaudie 1954) [39] to 1.7eV (Evans and Young 1965) [40] in MoSe₂, 1.1 eV (Evans and Hazelwood 1971) [41] in MoSe₂, and 0.9 eV (Revolinsky and Beerntsen 1964) [42] to 1.0 eV (Lepetit 1965) in MoSe₂. Photoemission studies (Williams and Shepherd 1973, Shepherd and Williams 1974, Wertheim et al. 1973, McMenamin and Spicer 1972, Williams 1973, Murray and Williams 1974) [43-45] indicate that the dz² band maximum lies in the order of 1eV below the Fermi level, so that carrier concentrations in the range 10¹⁵ cm⁻³ to 10¹⁹ cm⁻³ as observed in these materials must be attributed to the presence of donor or acceptor levels.
From the literature survey, it is seen that an early studies were made by Regnault in 1952 [46]. He has shown that the carrier concentration of both n and p type MoSe$_2$ specimen were of the order of $10^{19}$ cm$^{-3}$ and $10^{14}$ cm$^{-3}$ respectively. An extensive study has been made on mobility of charge carriers in the layered semiconductors by Fivaz (1967) [47]. He has studied the temperature dependence of electrical resistivity and Hall coefficient of semiconducting compounds e.g. GaSe, MoS$_2$, MoSe$_2$, and WSe$_2$ to detect the possible nontrivial departures of physical properties of layer structures from the isotropic crystals. From the measurements of temperature dependent mobility he has derived various scattering mechanisms involved in these materials. It was shown that in these materials, the free charge carriers tend to become localized within individual layers and thus to behave as if moving through a stack of independent layers. Moreover, it was found that this tendency is accompanied by a strong interaction between the free carriers and the optical phonons polarized normally to the layers.

Optical properties

The transmission spectra and optical absorption of group VI materials have been confined to measurements at liquid nitrogen temperature, 77K and room temperature by Frindt 1965, Evans and Young 1965 and 1968, Wilson and Yoffe 1969, Evans and Hazelwood 1971 [35,40,41,48,49] and the transmission spectra of group VIA have been measured at liquid helium temperature by A. R. Beal. [50]. Ying – Sheng Huang [51] studied the optical properties of 2H – MoSe$_2$ by thermoreflectance (TR) and electrolyte electroreflectance (EER) technique in the range of 1.4 to 6.2 eV at room temperature. The measurements of TR and EER spectrum of these crystals have enabled them to identify the various features in the spectrum and determine their interband transition energies with better accuracy. The absorption edge anisotropy of 2H – MoSe$_2$ was studied by photoconductivity (PC) measurements as a
function of temperature in the range of 12-300K. S.Y.Hu [51] observed the significant shift towards lower energies in the PC spectra on the edge plane with respect to those corresponding to the van der Waal (vdW) plane. Anisotropy of optical absorption in Re doped MoSe$_2$ layered single crystals was described by M.M. Vora et al. [52]. Ennaoui (1986) and J.M Huang (2000) have reported the photovoltaic properties and uses of MoSe$_2$ [53, 54]. M.D Curtist (1986) reported the action of MoSe$_2$ as dehydrosulfurization catalysts (1986). Recent investigations have shown that the layer type semiconducting group VI transition metal dichalcogenides, which absorb visible and near infrared light, are particularly interesting materials for photoelectrochemical solar energy conversion. The most efficient system up to now turned out to be MoSe$_2$. Recent applications include polymer based MoSe$_2$ solar cells.

### 6.3 Crystal Growth of MoSe$_2$

Now a day there are many techniques available for the crystal growth. The majority of compounds of the transition metal dichalcogenides belonging to MX$_2$ group are insoluble in water and decompose before their melting points are reached. Therefore, the growth of such crystals from the melt and aqueous solution is not possible and hence the growth of single crystals of these compounds, using vapour phase technique was found to be most suitable. It has been reported that the better method to obtain pure crystals is the direct vapour transport technique and it is possible to grow fairly large crystals of TMDCs by DVT where the transport of materials takes place directly due to the temperature gradient set up across the charge containing ampoule without any transporting agents. Since the direct vapour transport technique seems to be a better, easier and comparatively an economical method for the growth of pure crystals, this method has been used for the growth of MoSe$_2$ crystals in the present case.
In this technique, the materials in their elemental form from which the crystals are to be grown are transported from the source zone, which is kept at comparatively high temperature than the growth zone, kept at lower temperature of an enclosed system. During the growth process, the compound in the volatile form reacts or decomposes. This can be accomplished only if certain requirements of the growth mechanism, concerning the encasing tube as well as the furnace constructions, are satisfied. The requirements of the growth process by the direct vapour transport method are:

- Since a temperature profile with gradient is necessary for the crystal growth for 200 to 300 hrs, the furnace should essentially have two zones with separate temperature controllers.

- The transportation of the volatile compounds should be done in an impurity free, enclosed system / environment to ensure the purity of the grown crystal.

- The material used to make the encasing assembly should sustain at higher temperature compared to the melting / boiling point of the material to be grown. At the same time, the material of the encasing tube should be non-reactive at these temperatures in order to avoid contamination of the grown crystals.

Taking the above requisites into consideration, a two-zone horizontal furnace was found to be convenient to produce an appropriate temperature gradient over the entire length of quartz ampoule. A two-zone furnace was fabricated in the University Science and Instrumentation Centre, Sardar Patel University, Vallabh Vidyanagar by using a special sillimanite muffle tube of grade KR 80 GA HG. This muffle tube is closed at one end and having 450 mm length, 70 mm outer diameter and 56 mm inner diameter, with a threaded pitch of 3
mm, imported from Koppers Fabriken Feuerfester, Germany. A super Kanthal A-1 wire of 17 SWG was used for winding. This wire can withstand temperatures up to 1673K and was wound directly on to the furnace muffle in two different regions. The muffle was enclosed in glass wool jacket, brick powder and refractory bricks for proper insulation. The complete arrangement was fully encased in the metal sheets and the entire assembly was supported in a steel framework. In order to achieve required temperature profile, temperature controllers (Make: Select, Model: PR502) with profile programming facility based power unit were used for the two zones of the furnace. Thermocouples used were Pt (13 %), Rh - Pt. The complete structure of the furnace with the temperature controlling system is shown in figure 6.2.

![Figure 6.2: The complete furnace structure with temperature controlling system.](image)

As we know that quartz was considered as the best choice for making the encasing tube. High quality fused quartz tubes having a melting point of about 1773K were used for the growth experiments. The ampoules were cleaned prior to filling them with the stoichiometric mixture of required materials. The ampoule containing the source material was evacuated to a pressure of $10^{-5}$ Torr to minimize the
reaction of the elements with atmosphere at elevated temperatures and also to create an inside pressure very low so that the vapour pressure developed at high temperature within the ampoule does not lead to its blasting.

The sealed ampoule containing stoichiometric mixture of Mo and Se was loaded in the two zone horizontal furnace and the temperatures of both the zones were raised slowly for reaction between elements. The temperatures and the period for which the ampoule was kept in the furnace depended upon the material, which was being grown. The growth parameters such as temperature distribution, growths period etc used for the growth of MoSe₂ have been given in table 6.1.

<table>
<thead>
<tr>
<th>Source Zone Temp K</th>
<th>Growth Zone Temp K</th>
<th>Growth period (hrs)</th>
<th>Average dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1368</td>
<td>1343</td>
<td>197</td>
<td>7mm×4mm×5µm</td>
</tr>
</tbody>
</table>

### 6.4 Basic Heterojunction Model

Historically, Heterojunction theory has been divided into two parts as abrupt and graded Heterojunction. Abrupt Heterojunction theory is the older and was initially a straight forward extension of the formalism that was developed for the Heterojunction. Most phenomena however, could not be adequately explained by this simple model and an increasing number of hypotheses have been added to remove the discrepancy between theory and experiment. The progress in abrupt Heterojunction theory has been hampered by experimental difficulties in preparing true abrupt Heterojunction i.e. an electrical contact between two different semiconductors in which the interface width, being the length of the disordered region, is of the order of few atomic distances. The width of the interface region in nearly all experimental
Heterojunction is of the same order as the space charge regions on both sides of the metallurgical interface.

Semiconductor interfaces can be organized into three types of Heterojunction: straddling gap (type I), staggered gap (type II) and broken gap (type III) as seen in the figure 6.3. There are three relevant material parameters for classifying a given junction and understanding the carrier dynamics for a Heterojunction viz. band gap, electron affinity and work function. The energy difference between the valence band (VB) and conduction band (CB), called the band gap, is anywhere from 0eV for a metal (there is no gap) to over 4eV for an insulator. The work function of a material is the energy difference between the Fermi energy (chemical equilibrium energy) and the vacuum level (where electron removal occurs). Finally the electron affinity of each material is needed which is the energy difference between the conduction band and the vacuum level.

![Figure 6.3: Types of Heterojunction based on the band gap.](image)

The energy band model of ideal abrupt Heterojunction without interface traps was proposed by Anderson based on the previous work of Shockley.
Figure 6.4: (a) Energy band diagram for two isolated semiconductors. (b) Band alignment and formation of Heterojunction.

(a)

Figure 6.5: Energy band diagram of an n-p anisotype Heterojunction at thermal equilibrium.

Figure 6.4(a) shows the energy band diagram of two isolated pieces of two semiconductors. The two semiconductors were assumed to have different bandgaps $E_g$, different permittivities $\varepsilon$, different workfunctions $\Phi$ and different electron affinities $\chi$. Workfunction and electron affinity are defined as the energy required for removing an electron from the Fermi level $E_F$ and from the bottom of the conduction band $E_C$ respectively to a position just outside the material (vacuum level). The difference in energy of the conduction band edge in the two semiconductors is represented by $\Delta E_C$ and that in the valence band edges by $\Delta E_V$. 
When a junction is formed between these semiconductors, the energy band profile at equilibrium is as shown in figure 6.4(b) for an n-p anisotype Heterojunction. Since the Fermi level must coincide on both sides in equilibrium (figure 6.5) and the vacuum level is parallel to the band edges and is continuous.

6.5 Current Transport in Heterojunction Diode

Current transport in Hetrojunction is due to the thermionic emission. The thermionic emission theory assumes that the current is controlled only by the transfer of carriers across the top of the barrier, provided they move towards the barrier and the drift and diffusion that occur as a result of collisions within the space charge region are considered unimportant. The actual shape of the barrier is hereby ignored. For Heterojunction under forward bias assuming $q\Phi_b >> kT$, the electrons emitted over the barrier from one semiconductor into the another will be in equilibrium with the electron population in the semiconductors and thus will have a Maxwellian energy distribution. The resultant current $I$ due to thermionic emission for an applied bias $V$ is given by S. M. Sze [55],

$$I = AA^* T^2 \exp\left(-\frac{q\Phi_b}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$  (6.1)

where, $A$ is cross-sectional area of the diode, $A^*$ is Richardson constant, $T$ is temperature, $k$ is Boltzmann constant, $h$ is Plank’s constant, $q$ is electronic charge, $V$ is effective bias across the interface and $\Phi_b$ is the barrier height.

If the barrier height is assumed to vary linearly with bias as,

$$\Phi_b = \Phi_{b0} + \gamma V$$  (6.2)

where $\Phi_{b0}$ is the barrier height at zero bias and $\gamma (=\partial\Phi_b/\partial V)$ is positive.
Substituting equation 6.2 in equation 6.1 we get,

\[ I = I_0 \exp\left(\frac{-\gamma qV}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \]  

\[ \text{6.3} \]

where \( I_0 = A A^* T^2 \exp\left(\frac{-q\Phi_{b0}}{kT}\right) \)  

\[ \text{6.4} \]

\( I_0 \) is called the thermionic emission saturation current and hence one can write equation 6.4 in the form of,

\[ \Phi_{b0} = \frac{kT}{q} \ln \left(\frac{AA^* T^2}{I_0}\right) \]  

\[ \text{6.5} \]

Now, introducing a parameter \( \eta \) such that \( 1/\eta = 1 - \gamma \), equation 6.3 can be written as,

\[ I = I_0 \exp\left(\frac{qV}{\eta kT}\right) \left[1 - \exp\left(\frac{-qV}{kT}\right)\right] \]  

\[ \text{6.6} \]

Above equation 6.6 ensures that the current is zero if no voltage is applied as in thermal equilibrium any motion of carriers is balanced by a motion of carriers in the opposite direction. The \( \eta \) in equation 6.6 known as ideality factor gives a measure of the quality of the junction which is highly process dependent. For an ideal Heterojunction, when \( \eta = 1 \) (or \( \gamma = 0 \)), equation 6.6 reduces to the case of pure thermionic emission-diffusion (equation 6.1). This mode of current transport is commonly referred to as the "thermionic emission" current [56, 57]. In practice, however, larger values for \( \eta \) are obtained due to the presence of non-ideal effects or other contributing components to the total current through the junction.

Normally, the neutral region of the semiconductors, outside the depletion region and ohmic contacts, offers a series resistance (\( R_s \)) and
so a significant voltage drop (=IRs) occurs across it at large forward currents. This amounts to a reduction of the voltage across the barrier region from that actually applied to the terminals of the diode. This is accounted for by replacing V by V – IRs in equation 6.6. The current equation then becomes,

\[ I = I_o \exp \left( \frac{q(V - IR_s)}{\eta k T} \right) \left[ 1 - \exp \left( - \frac{q(V - IR_s)}{k T} \right) \right] \]

### 6.6 Barrier Height Inhomogeneity

It has been reported that the increase in ideality factors (η > 1) may be due to the spatial / lateral inhomogeneity at the junction. This inhomogeneity can be explained by using an analytical potential fluctuation model based on spatially inhomogeneous barrier height at the interface [58-60].

Suppose that the distribution of the barrier height is Gaussian in character \( P(\Phi_b) \) with a standard deviation \( \sigma_s \). So the barrier \( \Phi_b \) depend on the location within the interface plane with this barrier distribution \( P(\Phi_b) \) around the mean barrier \( \overline{\Phi}_b \). The Gaussian barrier distribution can be expressed as [58-60],

\[ P(\Phi_b) = \frac{1}{\sigma_s \sqrt{2\pi}} \exp \left( \frac{\Phi_b - \overline{\Phi}_b}{2\sigma_s^2} \right) \]

Now, the current across a homogeneous barrier at a forward bias V, when \( V > 3kT/q \), based on the thermionic emission theory is given by equation 6.7. According to Werner and Guttler [58-60] the net current I through an inhomogeneous junction is controlled by the effective /apparent barrier height \( \Phi_{ap} \) and the corresponding ideality factor is \( \eta_{ap} \). For most non homogeneous Heterojunction diodes, the current – voltage characteristics can still be well described with the help of the thermionic
emission theory, except that $\Phi_{b0}$ and $\eta$ should be replaced by $\Phi_{ap}$ and $\eta_{ap}$ in equation 6.7.

Considering equations 6.7 and 6.8 to describe the inhomogeneities of junctions, the total current $I$ can be expressed as,

$$I(V) = \int_{-\infty}^{+\infty} J(\Phi_b, V) P(\Phi_b) d\Phi$$

6.9

Performing this integration from $-\infty$ to $+\infty$, the apparent barrier height $\Phi_{ap}$ and ideality factor $\eta_{ap}$ at zero bias are given by [61,62],

$$\Phi_{ap} = \Phi_{b0} (T = 0) - \frac{q \sigma_0^2}{2kT}$$

6.10

$$\left(\frac{1}{\eta_{ap}} - 1\right) = \rho_2 - \frac{q \rho_3}{2kT}$$

6.11

The temperature dependence of $\sigma_s$ is usually small and thus can be neglected. However, $\sigma_s$ and $\Phi_{b0}$ are assumed to be linearly bias dependent on Gaussian parameters such that,

$$\Phi_b = \Phi_{b0} + \rho_2 V$$

6.12

$$\sigma_s = \sigma_0 + \rho_3 V$$

6.13

Where, $\rho_2$ and $\rho_3$ are the voltage coefficients that may depend on temperature and they quantify the voltage deformation on the barrier height distribution [60,62]. Thus, the standard deviation $\sigma_s$ and hence the parameter $\sigma_0$ can be considered as a measure of the barrier inhomogeneity.
6.7 Fabrication of p-SnSe/n-MoSe₂ Heterojunction diodes.

❖ Substrate cleaning

Initially crystals of MoSe₂ having flat shining surfaces grown by DVT method as discussed in section 6.3 were chosen. These crystals were cleaved with the help of low adhesion tap and then washed in acetone to remove contaminations and to make the surface clean. Later they were dried in the oven at 323K.

❖ Formation of Heterojunction

In this study Nanocrystalline thin film of p-SnSe were deposited using spin coating technique as discussed in chapter 2. In order to get deposited Nanocrystalline p-SnSe film on a confined area of the crystal surface, crystals were masked with araldite having circular holes of area 1mm². The second advantage of araldite is that it prevents the short circuit between back contact of MoSe₂ and deposited thin film.

❖ Electrical contacts

Back diode contact of n-MoSe₂ was taken by low strain thin Ag alloy wires (Lakeshore wire part No.671-260) and Ag conductive paste (Eltec-1228C), since silver gives good ohmic contact to n-MoSe₂. The second ohmic contact was taken on to the deposited Nanocrystalline thin film of p-SnSe with same wire and same paste. In the present study we prepared p-SnSe/n-MoSe₂ Heterojunction from deposited thin films with different thickness and annealing temperature as discussed in chapter 2. Prepared diodes structure and photograph is shown in figure 6.6.
6.8 I-V-T and C-V measurements

There are various methods that can be used for the determination of Heterojunction diode parameters, e.g. Current – voltage (I-V) analysis, Capacitor – voltage (C-V) analysis, Photoelectron spectroscopy etc. Amongst these methods I-V and C-V are the basic and simplest of all methods since they involve direct measurement of current, voltage and capacitance and provide first-hand information about the nature of the developed junction across the interface. In the present investigation the I-V-T and C-V data were acquired using Keithley Semiconductor Characterization System SCS-4200 along with HP-4284A LCR meter. The Model 4200-SCS provides a total system solution for DC characterization of semiconductor devices, test structures and materials. This advanced parameter analyzer provides intuitive and sophisticated capabilities for semiconductor device characterization. The Model 4200-SCS combines unprecedented measurement speed and accuracy with an embedded Windows NT-based PC and Keithley Interactive Test Environment (KITE) to provide a powerful single-box solution. KITE allows users to gain familiarity quickly with tasks such as managing tests and results and generating reports. Sophisticated and simple test sequencing and external instrument drives simplify performing automated device and wafer testing. The Keithley Model 4200 Semiconductor Characterization System (SCS) [63] can be programmed to characterize I-V and C-V of semiconductor devices and test structures, using up to eight Source-Measure Units (SMUs). A variety of supported external components
enhance the capabilities. The exceptional low current performance of the Model 4200-SCS makes it the perfect solution for research studies of single electron transistors (SETs), molecular electronic devices and other Nano electronic devices that requires I-V characterization.

**Figure 6.7: The complete furnace structure with temperature controlling system.**

Figure 6.7 shows the complete block diagram of Keithley Model 4200 Semiconductor Characterization System (SCS). The variation of current and voltage with temperature were accomplished by single zone small furnace along with temperature controller (Omron E5CZ). Keithley 4200 – Semiconductor Characterization System (SCS) is a versatile instrument, in which the start, stop and step for current or voltage values of the SMU’s are assigned initially. The switching of the terminals is to be connected to the device can be done using switch matrix unit coupled to the respective SMU’s. When these variables were set ready, temperature was also set constant at the desired level using temperature controller and the data obtained were stored as spreadsheet in the computer memory. The experiment was repeated at different temperatures from 293K to 393K in steps of 10K. The results can be
observed either in the table form or in the graphical form and may be edited as needed. It also allows saving comma-separated values in text files that can be easily imported into most analysis and spreadsheet programs such as excel or origin. Provisions are also there to save the test configuration being done. In the present investigation, adopting I-V-T and C-V as the measurement technique, various Heterojunction parameters were calculated by standard methods as discussed in next section.

6.9 Results and discussions

6.9.1 Stability of prepared diodes

For any prepared device stability is the most important parameter for the point of its commercial application. Hence first we check stability of our prepared Heterojunction diode.

Figure 6.8 shows I-V characteristics of prepared diodes with different film thickness and annealing temperature of p-SnSe thin films. They were measured on an alternate days of a week. This results show that prepared diodes are stable against open environments because there is no significant change in the rectification ratio of each diode with time. Thus we considered that these diodes as a stable electronic device for further investigation. It is observed that the similar diodes prepared by deposition of bulk p-SnSe thin films using thermal evaporation are not found as stable as by using Nanocrystalline p-SnSe prepared by spin coating method.
Figure 6.8: (a to f) I-V characteristics for prepared n-MoSe$_2$/p-SnSe diode with time.
6.9.2 I-V-T analysis

After the confirmation of stability for diodes I-V-T characteristics were measured for prepared diodes as shown in figure 6.9. From these graphs we can say that all diodes possess good rectification ratio. It is also observed from above graph, as the film thickness is increased rectification ratio is also increased because of as the film thickness is increased its crystallinity is increased (from XRD & TEM results). Also as the annealing temperature is increased rectification ratio is increased due to the fact that as annealing temperature is increased film becomes more crystalline (from XRD & TEM results).

In the present investigation, measured I-V-T characteristics were analyzed by using standard method [64-67] for evolution of various Hetrojunction diode parameters such as zero bias barrier height ($\Phi_{b0}$), ideality factor ($\eta$) and series resistance ($R_S$) as given below.

1. LnI→ V method
2. Norde method
3. Cheung method
Figure 6.9: (a to f) I-V characteristics for prepared n-MoSe₂/p-SnSe diode.
**LnI → V method**

The plot of LnI → V yield a straight line for V > (3kT/q) and this may cover two to three decades of change in current at low forward bias voltages. The intercept on y-axis of this straight line gives the value of saturation current (I₀). By using this value of I₀, a plot of Ln (I₀/AT²) → 1/T (Richardson plot) as shown in figure 6.10, gives straight line and intercept of this straight line on y axis gives value of Richardson constant (A') according to equation 6.4. The value of A' is near to reported values for bulk SnSe. Some deviation may be due to the Nanostructure of prepared p-SnSe thin films as well as inhomogenities present at the interface of the diode. By using both values of I₀ and A', Φₜ₀ can be calculated using equation 6.5 as mentioned above. Also from the slope of this straight line LnI → V plot at low forward bias, the ideality factor η can be calculated as,

\[
\eta = \frac{q}{kT} \frac{dV}{d\ln I}
\]

Where dV/dLnI is the inverse of the slope of LnI→ V plot.

![Figure 6.10: Plot of Ln(I₀/T²) → 1/T (Richardson plot) for prepared diodes.](image-url)
Figure 6.11: (a to f) plot of $\text{Ln} I \rightarrow V$ for prepared diodes.
Figure 6.11 shows Ln I → V graphs of prepared diodes. From figure 6.10 it is observed that reverse current is not saturated that shows bias dependent barrier height. From the slope and intercept of straight line corresponding to low forward bias voltage $\Phi_{b0}$ and $\eta$ were calculated as discussed above. The values of these parameters as obtain for prepared diodes are shown in table 6.2 for all temperatures.

**Norde Method**

The series resistance is a very important parameter of Heterojunction diode. Because of high series resistance, it is difficult to evaluate the accurate barrier height from the standard LnI → V method. Hence Norde [66] proposed an alternative method to determine values of $\Phi_{b0}$ and $R_s$ of diode even for high series resistance. In this method Norde function $F(V)$ is defined as,

$$
F(V) = \frac{V - kT}{q} \ln\left(\frac{I}{A A' T^2}\right)
$$

Where all symbols have usual meaning as describe above. $F(V)$ is used to plot against voltage. For a particular value of voltage we get minimum value of function $F(V)$ called $F(V)_{\text{min}}$ which is the point of interest in Norde method. The zero bias barrier height $\Phi_{b0}$ and series resistance $R_s$ is given by,

$$
\Phi_{b0} = F(V)_{\text{min}} + \frac{V_{\text{min}}}{2} - \frac{kT}{q}
$$

$$
R_s = \frac{kT}{q I_{\text{min}}}
$$

Figure 6.12 shows the plot of F(V)→V for prepared diodes. From these graph it is observed that in every diode we observed minimum value of F(V) at a particular value of applied voltage. By using these value of $F(V)_{\text{min}}$, $V_{\text{min}}$ and $I_{\text{min}}$ which is corresponding to $F(V)_{\text{min}}$ we calculate $\Phi_{b0}$ and $R_s$ using equation 6.16 and 6.17. Obtain results are shown in table 6.2.
Figure 6.12: (a to f) $F(V) \rightarrow V$ plot of prepared diodes.
Cheung Method

The Hetrojunction diode parameters such as $\Phi_{b0}$, $\eta$ and $R_s$ were also evaluated using a method developed by Cheung and Cheung [67]. Cheung’s functions can be written as follows,

$$H(I) = V - \eta \frac{kT}{q} \ln \left( \frac{I}{AA'T^2} \right)$$  \hspace{1cm} (6.18)

For the construction of $H(I)$ there is a requirement of $\eta$ and it is obtain by below equation

$$\frac{dV}{d(Ln I)} = I R_s + \eta \frac{kT}{q}$$ \hspace{1cm} (6.19)

From above equation 6.19 it is seen that if we plot graph of $dV/d(LnI) \rightarrow I$ it gives a straight line as shown in figure 6.13. From the value of intercept of this straight line we calculate $\eta$ and calculate $H(I)$ given by equation 6.18.

Cheung function (equation 6.18) is also writing as

$$H(I) = I R_s + \eta \Phi_{b0}$$ \hspace{1cm} (6.20)

From equation 6.20 it is seen that If we plot of $H(I) \rightarrow I$, its gives a straight line as shown in figure 6.14. From the slope of this straight we determine $R_s$ and from the intercept we calculate $\Phi_{b0}$. Obtain results are shown in table 6.2.
Figure 6.13: (a to f) plot of $dV/d(LnI)$ vs $I$ for prepared diodes.
Figure 6.14: (a to f) plot of H(I) → V for prepared diodes.
Table 6.2(a): Evaluated diode parameters for p-SnSe (1µm)/n-MoSe₂ diode

<table>
<thead>
<tr>
<th>T K</th>
<th>In I → V Method</th>
<th>Norde Method</th>
<th>Chung Method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I₀ (µA)</td>
<td>η</td>
<td>Φ₀₀ (eV)</td>
</tr>
<tr>
<td>293</td>
<td>0.19</td>
<td>7.50</td>
<td>0.67</td>
</tr>
<tr>
<td>303</td>
<td>0.21</td>
<td>7.23</td>
<td>0.69</td>
</tr>
<tr>
<td>313</td>
<td>0.24</td>
<td>7.00</td>
<td>0.71</td>
</tr>
<tr>
<td>323</td>
<td>0.28</td>
<td>6.79</td>
<td>0.73</td>
</tr>
<tr>
<td>333</td>
<td>0.32</td>
<td>6.58</td>
<td>0.75</td>
</tr>
<tr>
<td>343</td>
<td>0.39</td>
<td>6.25</td>
<td>0.77</td>
</tr>
<tr>
<td>353</td>
<td>0.46</td>
<td>6.07</td>
<td>0.79</td>
</tr>
<tr>
<td>363</td>
<td>0.53</td>
<td>5.90</td>
<td>0.81</td>
</tr>
<tr>
<td>373</td>
<td>0.62</td>
<td>5.74</td>
<td>0.83</td>
</tr>
<tr>
<td>383</td>
<td>0.73</td>
<td>5.59</td>
<td>0.84</td>
</tr>
<tr>
<td>393</td>
<td>0.85</td>
<td>5.45</td>
<td>0.86</td>
</tr>
</tbody>
</table>

Table 6.2(b): Evaluated diode parameters for p-SnSe (2µm)/n-MoSe₂ diode

<table>
<thead>
<tr>
<th>T K</th>
<th>In I → V Method</th>
<th>Norde Method</th>
<th>Chung Method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I₀ (µA)</td>
<td>η</td>
<td>Φ₀₀ (eV)</td>
</tr>
<tr>
<td>293</td>
<td>1.30</td>
<td>10.50</td>
<td>0.62</td>
</tr>
<tr>
<td>303</td>
<td>1.33</td>
<td>10.13</td>
<td>0.64</td>
</tr>
<tr>
<td>313</td>
<td>1.44</td>
<td>9.80</td>
<td>0.66</td>
</tr>
<tr>
<td>323</td>
<td>1.57</td>
<td>9.49</td>
<td>0.68</td>
</tr>
<tr>
<td>333</td>
<td>1.70</td>
<td>9.21</td>
<td>0.70</td>
</tr>
<tr>
<td>343</td>
<td>1.85</td>
<td>8.93</td>
<td>0.72</td>
</tr>
<tr>
<td>353</td>
<td>2.02</td>
<td>8.67</td>
<td>0.74</td>
</tr>
<tr>
<td>363</td>
<td>2.21</td>
<td>8.43</td>
<td>0.76</td>
</tr>
<tr>
<td>373</td>
<td>2.28</td>
<td>8.20</td>
<td>0.79</td>
</tr>
<tr>
<td>383</td>
<td>2.52</td>
<td>7.98</td>
<td>0.80</td>
</tr>
<tr>
<td>393</td>
<td>2.93</td>
<td>7.75</td>
<td>0.82</td>
</tr>
</tbody>
</table>

Table 6.2(c): Evaluated diode parameters for p-SnSe (3µm)/n-MoSe₂ diode

<table>
<thead>
<tr>
<th>T K</th>
<th>In I → V Method</th>
<th>Norde Method</th>
<th>Chung Method</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I₀ (µA)</td>
<td>η</td>
<td>Φ₀₀ (eV)</td>
</tr>
<tr>
<td>293</td>
<td>0.62</td>
<td>8.95</td>
<td>0.63</td>
</tr>
<tr>
<td>303</td>
<td>0.76</td>
<td>9.37</td>
<td>0.65</td>
</tr>
<tr>
<td>313</td>
<td>0.91</td>
<td>9.69</td>
<td>0.67</td>
</tr>
<tr>
<td>323</td>
<td>1.10</td>
<td>10.30</td>
<td>0.69</td>
</tr>
<tr>
<td>333</td>
<td>1.24</td>
<td>9.99</td>
<td>0.71</td>
</tr>
<tr>
<td>343</td>
<td>1.38</td>
<td>9.70</td>
<td>0.73</td>
</tr>
<tr>
<td>353</td>
<td>1.56</td>
<td>9.43</td>
<td>0.75</td>
</tr>
<tr>
<td>363</td>
<td>1.76</td>
<td>9.17</td>
<td>0.77</td>
</tr>
<tr>
<td>373</td>
<td>2.08</td>
<td>8.92</td>
<td>0.79</td>
</tr>
<tr>
<td>383</td>
<td>2.23</td>
<td>8.08</td>
<td>0.81</td>
</tr>
<tr>
<td>393</td>
<td>2.67</td>
<td>7.87</td>
<td>0.82</td>
</tr>
</tbody>
</table>
### Table 6.2(d): Evaluated diode parameters for p-SnSe (4µm)/n-MoSe$_2$ diode

<table>
<thead>
<tr>
<th>$T$ (K)</th>
<th>$I_0$ (µA)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>293</td>
<td>0.47</td>
<td>8.84</td>
<td>0.64</td>
<td>26.84</td>
<td>8.30</td>
<td>0.63</td>
<td>25.52</td>
<td></td>
</tr>
<tr>
<td>303</td>
<td>0.52</td>
<td>8.03</td>
<td>0.66</td>
<td>23.84</td>
<td>7.92</td>
<td>0.65</td>
<td>22.90</td>
<td></td>
</tr>
<tr>
<td>313</td>
<td>0.59</td>
<td>7.77</td>
<td>0.68</td>
<td>21.15</td>
<td>7.66</td>
<td>0.67</td>
<td>20.35</td>
<td></td>
</tr>
<tr>
<td>323</td>
<td>0.69</td>
<td>7.53</td>
<td>0.70</td>
<td>18.11</td>
<td>7.43</td>
<td>0.69</td>
<td>17.39</td>
<td></td>
</tr>
<tr>
<td>333</td>
<td>0.81</td>
<td>7.30</td>
<td>0.72</td>
<td>15.46</td>
<td>7.20</td>
<td>0.71</td>
<td>14.85</td>
<td></td>
</tr>
<tr>
<td>343</td>
<td>0.98</td>
<td>7.09</td>
<td>0.74</td>
<td>12.70</td>
<td>6.99</td>
<td>0.73</td>
<td>12.20</td>
<td></td>
</tr>
<tr>
<td>353</td>
<td>1.12</td>
<td>6.87</td>
<td>0.76</td>
<td>11.08</td>
<td>6.83</td>
<td>0.75</td>
<td>10.60</td>
<td></td>
</tr>
<tr>
<td>363</td>
<td>1.29</td>
<td>6.68</td>
<td>0.78</td>
<td>9.63</td>
<td>6.64</td>
<td>0.76</td>
<td>9.24</td>
<td></td>
</tr>
<tr>
<td>373</td>
<td>1.51</td>
<td>6.50</td>
<td>0.80</td>
<td>8.39</td>
<td>6.46</td>
<td>0.78</td>
<td>8.05</td>
<td></td>
</tr>
<tr>
<td>383</td>
<td>1.70</td>
<td>6.33</td>
<td>0.82</td>
<td>7.30</td>
<td>6.29</td>
<td>0.80</td>
<td>6.70</td>
<td></td>
</tr>
<tr>
<td>393</td>
<td>1.96</td>
<td>6.17</td>
<td>0.83</td>
<td>6.36</td>
<td>6.13</td>
<td>0.82</td>
<td>5.92</td>
<td></td>
</tr>
</tbody>
</table>

### Table 6.2(e): Evaluated diode parameters for p-SnSe (1µm AA 373K)/n-MoSe$_2$ diode

<table>
<thead>
<tr>
<th>$T$ (K)</th>
<th>$I_0$ (µA)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>293</td>
<td>0.07</td>
<td>4.63</td>
<td>0.69</td>
<td>60.70</td>
<td>4.51</td>
<td>0.67</td>
<td>63.74</td>
<td></td>
</tr>
<tr>
<td>303</td>
<td>0.08</td>
<td>4.47</td>
<td>0.71</td>
<td>53.61</td>
<td>4.36</td>
<td>0.69</td>
<td>56.29</td>
<td></td>
</tr>
<tr>
<td>313</td>
<td>0.10</td>
<td>4.33</td>
<td>0.73</td>
<td>47.32</td>
<td>4.22</td>
<td>0.71</td>
<td>49.69</td>
<td></td>
</tr>
<tr>
<td>323</td>
<td>0.11</td>
<td>4.20</td>
<td>0.76</td>
<td>43.40</td>
<td>4.09</td>
<td>0.73</td>
<td>45.57</td>
<td></td>
</tr>
<tr>
<td>333</td>
<td>0.13</td>
<td>4.07</td>
<td>0.78</td>
<td>39.76</td>
<td>3.96</td>
<td>0.75</td>
<td>41.75</td>
<td></td>
</tr>
<tr>
<td>343</td>
<td>0.14</td>
<td>3.95</td>
<td>0.80</td>
<td>36.40</td>
<td>3.85</td>
<td>0.77</td>
<td>38.22</td>
<td></td>
</tr>
<tr>
<td>353</td>
<td>0.16</td>
<td>3.84</td>
<td>0.82</td>
<td>33.29</td>
<td>3.74</td>
<td>0.79</td>
<td>34.96</td>
<td></td>
</tr>
<tr>
<td>363</td>
<td>0.18</td>
<td>3.73</td>
<td>0.84</td>
<td>30.42</td>
<td>3.64</td>
<td>0.81</td>
<td>31.95</td>
<td></td>
</tr>
<tr>
<td>373</td>
<td>0.20</td>
<td>3.63</td>
<td>0.86</td>
<td>27.78</td>
<td>3.54</td>
<td>0.83</td>
<td>29.17</td>
<td></td>
</tr>
<tr>
<td>383</td>
<td>0.23</td>
<td>3.54</td>
<td>0.88</td>
<td>25.35</td>
<td>3.45</td>
<td>0.86</td>
<td>26.62</td>
<td></td>
</tr>
<tr>
<td>393</td>
<td>0.26</td>
<td>3.45</td>
<td>0.91</td>
<td>23.12</td>
<td>3.36</td>
<td>0.88</td>
<td>24.28</td>
<td></td>
</tr>
</tbody>
</table>

### Table 6.2(f): Evaluated diode parameters for p-SnSe (1µm AA 423K)/n-MoSe$_2$ diode

<table>
<thead>
<tr>
<th>$T$ (K)</th>
<th>$I_0$ (µA)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
<th>$\eta$</th>
<th>$\Phi_{b0}$ (eV)</th>
<th>$R_S$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>293</td>
<td>0.03</td>
<td>3.28</td>
<td>0.71</td>
<td>16.76</td>
<td>3.28</td>
<td>0.68</td>
<td>16.39</td>
<td></td>
</tr>
<tr>
<td>303</td>
<td>0.03</td>
<td>3.17</td>
<td>0.73</td>
<td>15.25</td>
<td>3.17</td>
<td>0.71</td>
<td>14.06</td>
<td></td>
</tr>
<tr>
<td>313</td>
<td>0.04</td>
<td>3.07</td>
<td>0.76</td>
<td>13.87</td>
<td>3.074</td>
<td>0.73</td>
<td>12.37</td>
<td></td>
</tr>
<tr>
<td>323</td>
<td>0.05</td>
<td>2.98</td>
<td>0.78</td>
<td>12.59</td>
<td>2.97</td>
<td>0.75</td>
<td>10.89</td>
<td></td>
</tr>
<tr>
<td>333</td>
<td>0.05</td>
<td>2.89</td>
<td>0.80</td>
<td>11.42</td>
<td>2.88</td>
<td>0.77</td>
<td>9.58</td>
<td></td>
</tr>
<tr>
<td>343</td>
<td>0.06</td>
<td>2.80</td>
<td>0.82</td>
<td>10.36</td>
<td>2.80</td>
<td>0.79</td>
<td>9.08</td>
<td></td>
</tr>
<tr>
<td>353</td>
<td>0.07</td>
<td>2.72</td>
<td>0.85</td>
<td>9.38</td>
<td>2.72</td>
<td>0.81</td>
<td>7.99</td>
<td></td>
</tr>
<tr>
<td>363</td>
<td>0.08</td>
<td>2.65</td>
<td>0.87</td>
<td>8.49</td>
<td>2.65</td>
<td>0.83</td>
<td>7.03</td>
<td></td>
</tr>
<tr>
<td>373</td>
<td>0.09</td>
<td>2.58</td>
<td>0.89</td>
<td>7.67</td>
<td>2.54</td>
<td>0.86</td>
<td>6.23</td>
<td></td>
</tr>
<tr>
<td>383</td>
<td>0.10</td>
<td>2.51</td>
<td>0.91</td>
<td>6.93</td>
<td>2.48</td>
<td>0.88</td>
<td>5.48</td>
<td></td>
</tr>
<tr>
<td>393</td>
<td>0.12</td>
<td>2.45</td>
<td>0.93</td>
<td>6.26</td>
<td>2.41</td>
<td>0.90</td>
<td>4.82</td>
<td></td>
</tr>
</tbody>
</table>
From the above table 6.2 it is seen that as the temperature is increased zero bias barrier height $\Phi_{b0}$ is increased while ideality factor $\eta$ is decreased in all prepared diodes. This temperature dependency of both parameters shows presence of inhomogeneities at the interface region of prepared diodes. It is also concluded from table 6.2 that series resistance is decreased with increase in temperature due to semiconducting nature of both materials used in Hetrojunction diodes. It is also observed from above table 6.2 that as the thickness of SnSe thin film is increased we obtain minor change in ideality factor. While due to annealing temperature ideality factor reduce more compare to the other diodes because the effect of annealing is higher on to the film crystallanity in comparison to thickness as observed in XRD and TEM.

For ideal Hetrojunction diode, in particular, desirable for device application, an ideality factor approaching unity is desired. The ideality factors of real Hetrojunction diodes may be described by the Sah–Noyce–Shockley theory, yielding values of $n=1$ at a low voltage and $n=2$ at higher voltages [68]. If there were no defects present, the total diode current would be based exclusively on diffusion and $n$ would be 1. Therefore, no recombination processes are expected inside the space-charge region. The resulting minimization of leakage current loss at reverse bias and increased rectification characteristic are favorable properties of such devices. As recombination processes are driven by defects, more defects lead to more space-charge recombination increasing $n$ up to 2 the “nonideal” case. For Hetrojunction diodes, an ideality factor $n>2$ obtain in our investigation is not covered by the Sah–Noyce–Shockley theory and suggests the presence of surface or interface states, indicating that the junction is far from being ideal [69]. Breitenstein et al [70] introduced a model to describe ideality factors $n>2$ occurring in silicon based Hetrojunction on donor acceptor pair recombination, giving rise to an increased recombination current. It is
stated that for a high density of defect states, hopping conduction in the defect volume may govern the reverse conductivity of the devices. The model is able to explain ideality factors in the range n>2 as obtain in our Hetrojunction diodes.

6.9.3 Barrier Height Inhomogeneities

The interfaces of the semiconductor Heterojunction are important part of semiconductor devices. One of the most interesting properties of a semiconductor Heterojunction interface is its barrier height ($\Phi_b$), which is a measure of the mismatch of the energy levels for the majority carriers across the interface. Temperature dependent ideality factor ($\eta$) and barrier height ($\Phi_b$) and deviation of the Richardson constant ($A^*$) suggest an inhomogeneous barrier. Inhomogeneities are imperfections at the interface between two materials. These are borne from the surface not being atomically flat due to grain boundaries, multiple phases, facets, defects, etc. Other sources of inhomogeneity include nonuniformity within the doping profile and residual materials left over from processing creating interfacial states between the surfaces. The Gaussian statistics technique used to extract the barrier height inhomogeneities parameters and modify the Richardson plot to evaluate exact Richardson constant($A^*$) is discussed in section 6.6.

Below figure 6.15(a) shows the variation of $\Phi_{b0}$ with $\eta$ for all diodes. It can be said that the significant decrease of the zero bias barrier height with increase of the ideality factor especially are due to the barrier height inhomogeneities.
To find out the barrier height inhomogeneities parameters such as \( \sigma_0 \), \( \rho_2 \), and \( \rho_3 \) and barrier height at \( T=0 \) by using equation 6.10 and 6.11 as discussed in section 6.6. We plot graph of \( \Phi_{\text{ap.}} \rightarrow q/2kT \) and \( (\eta_{\text{ap.}}^{-1} - 1) \rightarrow q/2kT \) as shown in figure 6.16(b) and 6.15(b) respectively. From the graph of \( \Phi_{\text{ap.}} \rightarrow q/2kT \) we determine \( \sigma_0 \) and barrier height at \( T=0 \) from the slope and intercept of this graph respectively. As well as from \( (\eta^{-1} - 1) \rightarrow q/2kT \) plot we determine \( \rho_2 \) and \( \rho_3 \) from intercept and slope of this graph respectively. Obtain results are shown in table 6.3.
By using the obtain value of $\sigma_0$, the Richardson plot is modified by below equations 6.21 as [71],

$$
Ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2 \sigma_0^2}{2k^2 T^2}\right) = Ln\left(A_{\text{A}}\right) - \frac{qD_{\text{b}0}}{kT}
$$ 6.21

Plot of $(\ln (I_0/T^2) - (q^2\sigma_0^2/2k^2T^2)) \rightarrow 1/T$ is known as modified Richardson plot as shown in figure 6.16(a). From the intercept of this graph we calculate the accurate value of Richardson constant ($A^*$) is shown in table 6.3.

<table>
<thead>
<tr>
<th>Diodes</th>
<th>$\sigma_0$</th>
<th>% of Inhomogeneties</th>
<th>$\rho_2$</th>
<th>$\rho_3$</th>
<th>$A^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-SnSe (1µm)/n-MoSe₂</td>
<td>0.19</td>
<td>28.35</td>
<td>0.66</td>
<td>0.0101</td>
<td>22.99</td>
</tr>
<tr>
<td>p-SnSe (2µm)/n-MoSe₂</td>
<td>0.20</td>
<td>32.25806</td>
<td>0.77</td>
<td>0.0063</td>
<td>23.90</td>
</tr>
<tr>
<td>p-SnSe (3µm)/n-MoSe₂</td>
<td>0.19</td>
<td>30.15873</td>
<td>0.74</td>
<td>0.0092</td>
<td>22.23</td>
</tr>
<tr>
<td>p-SnSe (4µm)/n-MoSe₂</td>
<td>0.19</td>
<td>29.6875</td>
<td>0.70</td>
<td>0.0089</td>
<td>22.29</td>
</tr>
<tr>
<td>p-SnSe (1µm AA 373K)/n-MoSe₂</td>
<td>0.20</td>
<td>28.98551</td>
<td>0.49</td>
<td>0.0141</td>
<td>24.97</td>
</tr>
<tr>
<td>p-SnSe (1µm AA 423K)/n-MoSe₂</td>
<td>0.20</td>
<td>28.16901</td>
<td>0.29</td>
<td>0.0202</td>
<td>25.62</td>
</tr>
</tbody>
</table>

6.10 Band diagram construction using C-V Measurement

It is seen that the extraordinary success of low-dimensional semiconductor Heterojunction has attracted vast efforts in both fundamental and applied physics [72]. The electrical characteristics of such structures and devices are critically dependent on the Heterojunction band structure, which plays an important role in transport phenomena. The transition between the two materials at the Heterojunction interface causes energy discontinuities in the conduction and valence bands, $\Delta E_c$ and $\Delta E_v$, in the vicinity of the metallurgical junction [73,74]. In addition, a dipole layer may appear at the junction,[75] and various kinds of imperfections at the interface may
result in interface charge [76]. Due to the band discontinuities, the interface charge, dipole, and a possible change in the net doping concentrations at the junction, an electric field appears at the junction. Thus, it is essential to evaluate band discontinuities in order construct a band diagram of a Heterojunction diode. Various approaches have been developed for this [73, 74]. In our study we determine band offset by C-V measurements.

In the present study of p-SnSe/n-MoSe₂ Heterojunction diode, the reverse bias voltage depend junction capacitance (C) can be shown to follow the relation [77,78],

$$\frac{1}{C^2} = 2 \left( \frac{\varepsilon_{MoSe_2} N_{CMoSe_2} + \varepsilon_{SnSe} N_{CSnSe}}{qN_{CMoSe_2} \varepsilon_{MoSe_2} N_{CSnSe} \varepsilon_{SnSe}} \right) \times \left( \frac{V_D - V - 2kT}{A^2} \right)$$

6.22

Where $\varepsilon$ is dielectric constant, $N_c$ is carrier concentration of SnSe and MoSe₂ and $V_D$ is built-in-potential.

The extrapolation of the straight line of $1/C^2$→V plot to the point $1/C^2 =0$ gives $V_{int}$. Relation between $V_{int}$ and $V_D$ is given by

$$V_{int} = V_D - \frac{2kT}{q}$$

6.23

Using above equation we determine value of $V_D$ and this is used to deduce the conduction band offset $\Delta E_c$ using the relationship [77,78],

$$\Delta E_c = qV_D \left( E_{gSnSe} - \Delta E_{F_{MoSe_2}} - \Delta E_{F_{SnSe}} \right)$$

6.24

$E_g$ is the band gap of SnSe. $\Delta E_F$ is the separation of Fermi level from valance band or conduction band.
With this value of $\Delta E_c$, the valance band offset $\Delta E_V$ can also be determined using,

$$\Delta E_V = \Delta E_g - \Delta E_C$$  \hspace{1cm} 6.25

Where $\Delta E_g$ is the difference of the band gap of MoSe$_2$ and SnSe.

Also the built in potential $V_D$ divided into SnSe side ($V_{D_{\text{SnSe}}}$) and into MoSe$_2$ side ($V_{D_{\text{MoSe}_2}}$) determine as [77,78],

$$V_D = V_{D_{\text{SnSe}}} + V_{D_{\text{MoSe}_2}}$$  \hspace{1cm} 6.26

And

$$\frac{V_{D_{\text{SnSe}}}}{V_{D_{\text{MoSe}_2}}} = \frac{\varepsilon_{\text{MoSe}_2} N_{C_{\text{MoSe}_2}}}{\varepsilon_{\text{SnSe}} N_{C_{\text{SnSe}}}}$$  \hspace{1cm} 6.27

It is also observed from above equation 6.22 that slope of straight line portion of $1/C^2 \rightarrow V$ plot gives $\frac{2}{A^2} \left( \frac{\varepsilon_{\text{MoSe}_2} N_{C_{\text{MoSe}_2}} + \varepsilon_{\text{SnSe}} N_{C_{\text{SnSe}}}}{qN_{C_{\text{MoSe}_2}} \varepsilon_{\text{MoSe}_2} N_{C_{\text{SnSe}}} \varepsilon_{\text{SnSe}}} \right)$. From this value we determine carrier concentration of Nanocrystalline thin film of p-SnSe used in Heterojunction diode as shown in table 6.3.

In the determination of band offset values and carrier concentration as discussed above using C-V measurement we take values of required parameters of MoSe$_2$ crystals from early work on similar crystals [79, 80]

Figure 6.17 shows graph of $1/C^2 \rightarrow V$. The values of band offsets, $V_{D_{\text{SnSe}}}$ and $V_{D_{\text{MoSe}_2}}$ for prepared diodes are calculated as discussed above which are shown in table 6.4. From this values of band offset band diagram are constructed for prepared Hetrojunction diodes as shown in figure 6.18.
Figure 6.17: (a to f) plot of $1/C^2 \rightarrow V$ for prepared diodes taken at 10kHz frequency.
Table 6.4: The values of $V_{\text{int}}$, $V_D$, $V_{\text{D}_{\text{SnSe}}}$, $V_{\text{D}_{\text{MoSe}_2}}$, band offsets and carrier concentration for prepared diodes.

<table>
<thead>
<tr>
<th>Diodes</th>
<th>$V_{\text{int}}$</th>
<th>$V_D$</th>
<th>$V_{\text{D}_{\text{SnSe}}}$</th>
<th>$V_{\text{D}_{\text{MoSe}_2}}$</th>
<th>$\Delta E_C$</th>
<th>$\Delta E_V$</th>
<th>$N_{\text{CSnSe}} \times 10^{20}$ m$^{-3}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-SnSe (1µm)/n-MoSe$_2$</td>
<td>0.190</td>
<td>0.2417</td>
<td>0.0176</td>
<td>0.2241</td>
<td>0.1938</td>
<td>0.3262</td>
<td>6.028</td>
</tr>
<tr>
<td>p-SnSe (2µm)/n-MoSe$_2$</td>
<td>0.180</td>
<td>0.2317</td>
<td>0.0183</td>
<td>0.2134</td>
<td>0.1872</td>
<td>0.1128</td>
<td>6.344</td>
</tr>
<tr>
<td>p-SnSe (3µm)/n-MoSe$_2$</td>
<td>0.170</td>
<td>0.2217</td>
<td>0.0194</td>
<td>0.2022</td>
<td>0.1819</td>
<td>0.0181</td>
<td>6.663</td>
</tr>
<tr>
<td>p-SnSe (4µm)/n-MoSe$_2$</td>
<td>0.165</td>
<td>0.2167</td>
<td>0.0216</td>
<td>0.1951</td>
<td>0.1815</td>
<td>0.0815</td>
<td>7.052</td>
</tr>
<tr>
<td>p-SnSe (1µm 373K)/n-MoSe$_2$</td>
<td>0.175</td>
<td>0.2267</td>
<td>0.0219</td>
<td>0.2048</td>
<td>0.1977</td>
<td>0.0123</td>
<td>6.978</td>
</tr>
<tr>
<td>p-SnSe (1µm 423K)/n-MoSe$_2$</td>
<td>0.155</td>
<td>0.2067</td>
<td>0.0343</td>
<td>0.1723</td>
<td>0.1798</td>
<td>0.1598</td>
<td>7.365</td>
</tr>
</tbody>
</table>

(a) p-SnSe(1µm)/n-MoSe$_2$  
(b) p-SnSe(2µm)/n-MoSe$_2$  
(c) p-SnSe(3µm)/n-MoSe$_2$  
(d) p-SnSe(4µm)/n-MoSe$_2$
Figure 6.18 (a to f): Band diagram of prepared hetero junction diode.

6.11 Conclusions

- Heterojunction diode of p-SnSe/n-MoSe$_2$ have been successfully fabricated by depositing Nanocrystalline thin films of P-SnSe on cleaved n-MoSe$_2$ crystal by spin coating technique and they were studied for their stability and I-V characteristics in the temperature range 293K – 393K.

- The current voltage characteristics of the fabricated diodes show good rectification ratio.

- The dominant current conduction mechanism in this diode has been found to be thermionic emission (TE). On the basis of this diode parameters were deduced.

- The value of zero bias barrier height has been calculated using three different methods i.e. $\ln I$ vs. $V$ method, $F(V)$ vs. $V$ method and $H(I)$ vs. $I$ method for the temperature range 293K - 310K and it was revealed that the barrier height decreases with decrease of temperature for diodes which is shown in table 6.2.

- The decrease of barrier height with decreasing of temperature may be attributed to the interface states, inhomogeneous nature of the fabricated diode, multiple transport mechanisms involved in the conduction of carriers etc.
The diode ideality factor has also calculated by above mentioned method for the same temperature range which shows that as temperature decreases the ideality factor increases (Table 6.2).

The inhomogeneous thickness and composition of the layer, non-uniformity of the interfacial charges, etc. may be ascribed for the change of barrier height and ideality factor at low temperature.

Three different methods have been applied to extract the barrier parameters to subtract the effect of diode series resistance from barrier parameters as mentioned above. But, in present investigation there are no any large variation has been found in the values of barrier parameters extracted using three different methods (Table 6.2) which shows that series resistance does not affect the barrier parameters by large amount.

The Richardson plot drawn for the given diode yields a straight line giving the Richardson constant.

The percentage value of inhomogeneity for prepared diodes is around 29% (table 6.3).

The reason for the higher inhomogeneity in this case may be due to presence of more structural defects in morphology of prepared thin films.

From the C –V analysis conduction band off set $\Delta E_c$, valance band off set $\Delta E_v$, built in potential $V_D$ divided into SnSe side ($V_{D\text{SnSe}}$) and into MoSe$_2$ side ($V_{D\text{MoSe}_2}$) were determine(table 6.4).
References:

1. W. Shockley, 

2. A. I. Gubanov, 
   Zh. Tekh. Fiz, 21, (1951), 304.

3. H. Kroemer, 

4. Harald Böttner, Gang Chen, and Rama Venkatasubramanian, 

5. A. G. Milnes and D. L. Feucht, 
   Heterojunctions and Metal-Semiconductor Junctions, Academic, 

6. B. L. Sharma and R. K. Purohit, 

7. R. S. Muller and R. Zuleeg, 

8. W. A. Gutierrez and H. L. Wilson, 

9. F. V. Shallcross, 

10. C. J. Moore and D. E. Brodie, 

11. F. Pfisterer and H. W. Schock, 

12. J. Touskova, D. Kindl and J. Kovanda, 

13. R. Venugopal, B. K. Reddy and D. R. Reddy, 

14. N.I.Aly, A.A.Akl, A.A.Ibrahim, and A.S.Riad, 


37. A. D Yoffe, 12\textsuperscript{th} Int. Conf. on Physics of semiconductors, (1974).


58. H. H. Guttler and J. H. Werner,


63. Keithley 4200 SCS user manual.


