CHAPTER 8

FATIGUE LIFE ESTIMATION OF ELECTRONIC PACKAGES SUBJECTED TO DYNAMIC LOADS

8.1 INTRODUCTION

Vibration environments can often involve millions of stress cycles because natural frequencies in electronics can range from 50 Hz to well over 1000 Hz. Stress raisers and stress concentrations can be very severe when millions of cycles are accumulated. Electrical lead wires loaded in tension or bending will fail very often in vibration events because a large number of stress cycles can be accumulated in a short period of time. Stress concentrations in the solder joints do not appear to have much effect on the fatigue life. The relatively soft solder joints relieve the high local stresses associated with stress concentrations by plastically deforming in these areas.

Testing has shown that thermal cycling events typically produce many more solder joint failures than lead wire failures for surface-mounted and through-hole-mounted PCB components. Vibration events tend to produce many more electrical lead wire failures than solder joint failures in surface-mounted and through-hole-mounted PCBs (Steinberg 2001). When a solder joint failure shows up during vibration, most of the time crack initiation was due to thermal cycling. Since thermal cycling is slow, the crack propagation is also very slow. However, vibration can often develop several hundred stress cycles in a second, so the crack propagation is very rapid in vibration. The solder joint failure then appears to be due to vibration.
Stress reversals can occur in electronic equipment during exposure to vibration conditions. The combination of high stresses and a large number of stress reversals can destroy almost any type of structure. Every stress cycle uses up part of the fatigue life of the structure. It does not matter if the stress cycle is generated by thermal, vibration or shock. The life used up by a component due to different environments can be estimated by using Miner’s cumulative damage criteria. It uses a ratio of the actual number of stress cycles divided by the number of cycles requires to produce a failure. When the sum of all the ratios equals 1.0, the part is expected to fail.

Accurate determination of stresses and strains induced in the lead wires or solder joints due to dynamic loads is not possible by experimental procedures. Therefore, in past many researchers (Ron Li 2001, Andy Perkins 2008, YoungBae Kim 2006, Shaw Fong Wong 2007, Dehbi 2005, Sony Mathew 2006, Chen 2008) have used finite element simulation to determine the stresses and strains in the critical elements of the electronic package. In this thesis also, stresses induced in the lead wires were determined from the finite element simulation.

In this chapter, efforts are made to show that the lead wires of DIP and PSOP components attached to PCBs mounted on rubber spacers will experience less fatigue damage ratio in sinusoidal and random vibration environments.

### 8.2 FATIGUE LIFE ESTIMATION IN A SINUSOIDAL VIBRATION ENVIRONMENT

#### 8.2.1 Damage Developed during a Sine Sweep through a Resonance

Many a times the natural frequencies of the PWB assemblies are excited and experience high acceleration levels due to harmonic excitation.
The lead wires of the electronic packages will undergo several stress reversals
in sinusoidal vibration environment. Most of the damage produced in a vibration environment will occur, when the natural frequency of the structure is excited and a high transmissibility can often be expected at the natural frequency. Most of the damage accumulated during a sinusoidal sweep test will occur as the frequency sweeps through the peak response area. This reference area is the half power points, used extensively by electrical engineers to characterize resonant peaks in electrical circuits. These are the points where the power that can be absorbed by damping is proportional to the square of the amplitude at a given frequency. The half power points are then used to define the bandwidth of the system as shown in Figure 8.1.

![Figure 8.1 Half power points for transmissibility curve](image)

The time it takes to sweep through the half power points using a logarithmic sinusoidal input can be obtained from Equation (8.1).

\[
t = \frac{\log e \left( 1 + \frac{1}{2Q} \right)}{R \log e \left( \frac{1}{2Q} \right)}
\]

(8.1)
where \( t \) = time in minutes to sweep through the half power points
\[ R = \text{sweep rate in octave per minute} \]
\[ Q = \text{transmissibility at resonance (dimensionless)} \]

Also, the time taken to complete one logarithmic sinusoidal sweep between two different frequencies \( f_2 \) and \( f_1 \) can be obtained from Equation (8.2).

\[
 t = \frac{\log e \left( \frac{f_2}{f_1} \right)}{R \log e 2}
\]  

\( f_2 \) = upper frequency, Hz.
\( f_1 \) = lower frequency, Hz
\( R \) = sweep rate in octave per minute

### 8.2.2 Resonance Dwell Test

Resonance dwell test is conducted to check the ruggedness of electronic packages by using sine-sweep in the frequency range \( \pm 5\% \) (Yang et al 2000) around the first natural frequency (46 Hz in case of DIP-PCB assembly). The PCB assembly is subjected to maximum displacement and stresses as it passes through the resonant frequency of 46 Hz. PCB assembly was subjected to 2500 sweeps at an input acceleration load of 1G. During resonance dwell tests, the failure of component lead wires were monitored using a failure detecting circuit as shown in Figure 4.3 (Chapter 4). In case, any of the lead wire or solder joint fails, the LED provided on the circuit will go off or blink due to opening of lead wire or solder joint. After 2500 sweeps, the PCB assembly was removed from the fixture for inspection. The inspection process revealed no failures in the components of the PCB assembly.
8.2.3 Fatigue Life Calculations for a Through-Hole Mounted Electronic Component (DIP)

The lead wires and solder joints of electronic components are usually the most critical elements of an electronic package. Due to small size of the package lead wires, it is not possible to estimate the stress levels by experimental methods. Hence, finite element analysis is used to estimate the stresses induced in the lead wires of the electronic package due to vibration environment. The finite element simulation procedure is explained in section 4.4 of chapter 4. The sinusoidal test at 1G input load was simulated in ANSYS using similar conditions such as boundary conditions used during sine sweep test and damping ratio (obtained from tests). The stress plot obtained from the simulation is shown in Figure 8.2 and from the figure it is observed that the outer pins are subjected to more stresses compared to the inner pins. The maximum stress induced in the outer pins is 44.3 MPa and hence these are the most critical component of package. The fatigue life calculations will be based on this data.

![Stress plot at 1G with PCB mounted on plastic spacers](image)
The fatigue life of the DIP lead wires is calculated using the procedure as described by Steinberg (2001). The number of cycles required for the failure of lead wire is calculated using the Basquin power law given by Equation (8.3).

$$N_1 = N_2 \left( \frac{s_2}{s_1} \right)^b$$  \hspace{1cm} (8.3)

where,

$N_1 = \text{expected number of cycles for lead wire to fail at stress level } S_1$

$S_1 = 44.3 \text{ MPa (stress magnitude in the outer lead wire, obtained from Figure. 8.2)}$

$N_2 = 1000 \text{ cycles (number of cycles to fail at reference stress } S_2, \text{ Figure 8.3)}$

$S_2 = 310.26 \text{ MPa (stress magnitude at } N_2 \text{ cycles, obtained from Figure 8.3)}$

$b = 6.4 \text{ (slope of } S-N \text{ curve, Figure 8.3)}$

![Figure 8.3 S-N curve of the lead wire material](image-url)
Thus, the numbers of cycles \( N_1 \) required for the failure of outer lead wires (at 1G input) are obtained using Equation (8.3).

\[
N_1 = 1000 \left( \frac{310.26}{44.3} \right)^{6.4} = 257 \times 10^6 \text{ cycles}
\]

Similarly, the number of cycles \( n_1 \) accumulated during 2500 sweeps of resonance test is determined using Equation (8.4).

\[
n_1 = f_n \times (3600 \text{ sec}) \times \text{(test duration in hours)} \quad (8.4)
\]

Time \((t)\) taken for one sweep (logarithmic) calculated using Equation (8.1) at fundamental frequency of 46 Hz, transmissibility ratio \((Q)\) of 25 (at 1G input), and a sweep rate \((R)\) of one octave per minute is found to be 0.058 minute. Therefore, the time taken for 2500 sweeps is 145 minutes (2.42 hours).

The number of cycles \((n_1)\) accumulated during 2500 sweeps i.e. 2.42-hour test are:

\[
n_1 = 46 \times (3600 \text{ sec}) \times (2.42) = 400200 \text{ cycles}
\]

The fatigue damage ratio due to 2.42 hour resonance test can be estimated using Equation (8.5).

\[
R_n = \frac{n_1}{N_1} \quad (8.5)
\]

\[
R_n = \frac{400200}{257 \times 10^6} = 0.0016
\]
The life used up by the lead wires of the DIP package during 2.42 hours of resonance dwell test is 0.16%.

The PCB assembly mounted on rubber spacers was also simulated in ANSYS, and the stresses induced in lead wires of the DIP are shown in Figure 8.4. The maximum stress of 32.7 MPa is noticed in the outer lead wires. This magnitude of stress induced in lead wires is 26% less compared to the stress magnitude in lead wires when the PCB assembly was mounted on plastic spacers.

![Stress plot at 1G with PCB mounted on rubber spacers](image)

**Figure 8.4 Stress plot at 1G with PCB mounted on rubber spacers**

The fatigue damage ratio for the outer pins (at 1G input) when PCB is mounted on rubber spacers is estimated and tabulated in Table 8.1.
### Table 8.1 Fatigue damage ratio in DIP lead wires due to 1G input

<table>
<thead>
<tr>
<th>PCB assembly mounted on:</th>
<th>$N$ (cycles)</th>
<th>$n$ (cycles)</th>
<th>Fatigue damage ratio $R_n = n/N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic spacers</td>
<td>$257 \times 10^6$</td>
<td>400200</td>
<td>0.0016</td>
</tr>
<tr>
<td>Rubber spacers</td>
<td>$1796 \times 10^6$</td>
<td>552772</td>
<td>0.00031</td>
</tr>
</tbody>
</table>

The fatigue damage ratio due to 1G input acceleration for the DIP-PCB assembly mounted on plastic spacers is 0.0016 and similarly for the PCB mounted on rubber spacers it is 0.00031 which is about 81% less than the former case. From Table 8.1, it is very clear that, by using the rubber spacers the fatigue damage ratio can be reduced and the life of electronic equipment may be improved.

#### 8.2.4 Fatigue Life Calculations for a Surface-Mounted Electronic Component (PSOP)

The fatigue damage ratio of the lead wires of the PSOP subjected to 0.5G input acceleration load was estimated when the PCB was mounted on plastic spacers and rubber spacers. The procedure as explained in section 8.2.3 was used to estimate the fatigue damage ratio. The stresses induced in the lead wires are obtained from the finite element analysis result, which is explained in section 7.5.1. The maximum stress induced in the lead wires when the PCB assembly is mounted on plastic spacers is shown in Figure 8.5 and from the figure it is observed that, the maximum stress of 29 MPa is induced in the outer pins of the centrally located package. Hence, the outer pins of PSOP will be treated as critical elements in the assembly and fatigue damage ratio will be estimated for these elements.
Figure 8.5 Stress plot for PSOP at PCB centre (plastic spacer)

Figure 8.6 shows the stresses induced in lead wires of PSOP located at the corner of the PCB. The stresses induced in lead wires of corner mounted PSOP is about 10MPa which is much less compared to the stresses in the centrally located PSOP lead wires.

Figure 8.6 Stress plot for PSOP at PCB corner (PCB on plastic spacers)
Similarly, the magnitude of stresses induced in the lead wires of centrally located PSOP when PCB assembly was mounted on rubber spacers is shown in Figure 8.7 and the magnitude of stress levels experienced by the outer pins is found to be 25 MPa. By mounting the PSOP-PCB assembly on rubber spacers the stress magnitude is reduced by 14%. Due to reduction in the stress magnitude the lead wires will experience less fatigue damage ratio.

![Figure 8.7 Stress plot for PSOP at PCB centre (PCB on rubber spacers)](image)

Similarly, the maximum stress induced in the lead wires of the PSOP mounted at the PCB corner is found to be 6 MPa. The fatigue damage ratio for the two cases of PCB-PSOP assembly mounting are estimated and tabulated in Table 8.2.

### Table 8.2 Fatigue damage ratio in PSOP lead wires due to 0.5G input

<table>
<thead>
<tr>
<th>PCB assembly mounted on:</th>
<th>$N$ (cycles)</th>
<th>$n$ (cycles)</th>
<th>Fatigue damage ratio $R_n = n/N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic spacers</td>
<td>$3869 \times 10^6$</td>
<td>$0.73 \times 10^6$</td>
<td>0.00019</td>
</tr>
<tr>
<td>Rubber spacers</td>
<td>$17060 \times 10^6$</td>
<td>$1.23 \times 10^6$</td>
<td>0.000072</td>
</tr>
</tbody>
</table>
From Table 8.2 it is evident that the fatigue damage ratio experienced by the PSOP lead wires when the PCB assembly is mounted on rubber spacers is found to be 0.00019 which is 61.8% less than the fatigue damage ratio of the PSOP lead wires when the PCB assembly is mounted on plastic spacers. Thus, from the data tabulated in Table 8.2, it is evident that the fatigue damage ratio of the PSOP lead wires when the PCB assembly is mounted on rubber spacers is less than the fatigue damage ratio of lead wires of the PSOP when the PCB assembly is mounted on plastic spacers.

8.3 FATIGUE LIFE ESTIMATION IN A RANDOM VIBRATION ENVIRONMENT

8.3.1 Three band technique and Miner’s rule

Random vibration is non-periodic, so probability functions based on past history are used to predict various acceleration and displacement amplitudes, but it is not sufficient to predict precise magnitude at a specific instant. The distribution most often used is the Gaussian distribution (normal). The total area under the curve is unity. The area under the curve between any two points represents the probability that the accelerations will be between these two points. The maximum acceleration level considered for random vibrations is $3\sigma$ level. The three band method of analysis is based on Gaussian distribution. The instantaneous accelerations between $+1\sigma$ and $-1\sigma$ levels are assumed to act at the $1\sigma$ level 68.3% of the time. Instantaneous acceleration levels between $+2\sigma$ and $-2\sigma$ are assumed to act 27.1% (95.4 - 68.3) of the time. Instantaneous acceleration levels between $+3\sigma$ and $-3\sigma$ are assumed to act 4.33% (99.7 - 95.4) of the time. These three bands and normal distribution curve are as shown in Figure 8.8.
The total fatigue damage ratio due to different stress levels in a random vibration environment may be estimated using the principle of linear damage superposition or the Miner’s rule which is given by Equation (8.6).

\[
\text{Damage Ratio, } R_n = \frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3} + \ldots = \sum_{i=1}^{m} \frac{n_i}{N_i} \tag{8.6}
\]

where \( N_i \) = number of cycles to failure when subjected only to load amplitude level \( i \)

\( n_i \) = number of cycles accumulated at the amplitude level \( i \).

8.3.2 Fatigue Life Calculations for a Through-Hole Mounted Electronic Component (DIP)

To calculate the fatigue damage ratio at any given stress level, the magnitude of \( 1\sigma \) RMS stresses induced in the lead wires of the package are essential. The magnitude of stresses induced in the lead wires are obtained
from the finite element analysis (spectrum analysis). The procedure of doing spectrum analysis in ANSYS is explained in section 5.3.2 of chapter 5. The $1\sigma$ RMS stress plot obtained from spectrum analysis corresponding to the conditions when PCB is mounted on plastic spacers is shown in Figure 8.9. From this figure it is observed that, the maximum stresses (45.2 MPa) are again induced in the outer lead wires of the package.

![RMS stress plot](image)

**Figure 8.9 $1\sigma$ RMS stress plot (PCB on plastic spacers)**

The fatigue damage ratio of the lead wires due to random vibration environment was estimated using the procedure as explained below.

The number of cycles ($N_i$) required for the failure of lead wire at different stress levels is calculated using the Equation (8.3).

\[
N_i = \text{expected number of cycles for lead wire to fail} \\
S_i = 45.2 \text{ MPa ($1\sigma$ stress magnitude in the lead wire, obtained from Figure 8.9)}
\]
\( N_2 = 1000 \text{ cycles (number of cycles to fail at reference stress } S_2, \text{ Figure 8.3)} \)
\( S_2 = 310.26 \text{ MPa (stress magnitude at } N_2 \text{ cycles, obtained from Figure 8.3)} \)
\( b = 6.4 \text{ (slope of S-N curve, Figure 8.3)} \)

Number of cycles for failure at \( 1\sigma \) level is:

\[
1\sigma N_1 = 1000 \left( \frac{310.26}{45.2} \right)^{6.4} = 226026344.56 \text{ cycles}
\]

Similarly, the number of expected cycles for failure of lead wires at \( 2\sigma \) and \( 3\sigma \) levels are calculated and tabulated in Table 8.3.

The actual number of cycles (\( n_i \)) applied during the operation, may be estimated by multiplying the time duration, the first mode frequency and the percentage of times corresponding to each sigma band as given below.

\[
I\sigma n = f_n \times (3600 \text{ sec}) \times (\text{test duration in hours}) \times (0.683)
\]

The number of stress cycles (\( n_i \)) accumulated during 30 minutes (0.5 hour) of random vibration test is calculated at \( 1\sigma \) level using three band method as follows.

\[
I\sigma n_1 = f_n \times (3600 \text{ sec}) \times (0.5 \text{ Hr}) \times (0.683) = 50 \times 3600 \times 0.5 \times 0.683
\]
\[= 61470 \text{ cycles}\]
\((f_n = 50 \text{ Hz, the fundamental frequency of PCB assembly})\)

Similarly, the number of stress cycles at \( 2\sigma \) and \( 3\sigma \) levels are estimated and tabulated in Table 8.3.
Now the cumulative damage ratio $R_n$ is calculated using following relation.

$$R_n = \frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3} + \frac{n_4}{N_4} + \ldots$$

$$R_n = \frac{61470}{226026344.56} + \frac{24300}{2676499.02} + \frac{3897}{199794.27} = 0.029$$

The number ‘0.029’ represents the life used up by the PCB assembly during 30 minutes of random vibration test.

Similarly, the magnitude of $1\sigma$ RMS stresses induced in the lead wires when the DIP-PCB assembly was mounted on rubber spacers is obtained from finite element simulation and the plot is shown in Figure 8.10. From this figure it is observed that, the maximum stress of 16.8 MPa is induced in the outer pins. Thus, by mounting the DIP-PCB assembly on rubber spacers, the stress magnitude is reduced by 63%. The fatigue damage ratio estimated for the outer pins of the DIP is tabulated in Table 8.3.

![Figure 8.10 $1\sigma$ RMS stress plot (PCB on rubber spacers)
Table 8.3 Fatigue damage estimation in DIP lead wires due to random vibrations

<table>
<thead>
<tr>
<th>PCB assembly mounted on:</th>
<th>Sigma level</th>
<th>( n_i ) (cycles)</th>
<th>( N_i ) (cycles)</th>
<th>( n_i/N_i )</th>
<th>Cumulative fatigue damage ratio ( \Sigma n_i/N_i )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic Spacers</td>
<td>( 1\sigma )</td>
<td>61470</td>
<td>2.26x10^8</td>
<td>2.72x10^{-4}</td>
<td>0.029</td>
</tr>
<tr>
<td></td>
<td>( 2\sigma )</td>
<td>24390</td>
<td>2.68x10^6</td>
<td>9.11x10^{-3}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( 3\sigma )</td>
<td>3897</td>
<td>2.00x10^5</td>
<td>1.95x10^{-2}</td>
<td></td>
</tr>
<tr>
<td>Rubber Spacers</td>
<td>( 1\sigma )</td>
<td>56552</td>
<td>1.27x10^{11}</td>
<td>4.44x10^{-7}</td>
<td>4.72x10^{-5}</td>
</tr>
<tr>
<td></td>
<td>( 2\sigma )</td>
<td>22439</td>
<td>1.51x10^{9}</td>
<td>1.49x10^{-5}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( 3\sigma )</td>
<td>3585</td>
<td>1.13x10^{8}</td>
<td>3.18x10^{-5}</td>
<td></td>
</tr>
</tbody>
</table>

\( i=1\sigma, 2\sigma, 3\sigma \)

From Table 8.3 it is seen that the cumulative fatigue damage ratio of the DIP lead wires when the PCB assembly is mounted on plastic spacers is more (0.029) than the cumulative fatigue damage ratio of the DIP lead wires when the PCB assembly is mounted on rubber spacers. Thus, from this data it is again evident that, the rubber spacers are effective in enhancing the life of electronic packages in random vibration environment also.

8.3.3 Fatigue Life Calculations for a Surface-Mounted Electronic Component (PSOP)

Spectrum analysis on PSOP-PCB assembly was performed in ANSYS simulating the conditions when the assembly is mounted on plastic and rubber spacers. The simulation result for the PCB mounted on plastic spacers is shown in Figure 8.11.
The $l\sigma$ RMS stress level of 6.3 MPa is observed in the outer lead wires of centrally located package (Figure 8.11). Similarly, the $l\sigma$ RMS stress level of about 2.8 MPa is noticed in outer lead wires of the package mounted at the corner of the PCB. Therefore, the lead wires of the centrally located package are subjected to maximum stresses and the fatigue damage will be estimated for these lead wires.

Figure 8.12 shows the $l\sigma$ RMS stress level induced in lead wires of the centrally located package when the PSOP-PCB assembly is mounted on rubber spacers. The stress magnitude in the outer lead wires is found to be 4.5 MPa.

The fatigue damage ratios for the lead wires when PCB assemblies are mounted on plastic spacers and rubber spacers are estimated and tabulated in Table 8.4. From the Table 8.4 it is again observed that, the fatigue damage ratio experienced by the lead wires of package with PCB mounted on rubber
spacers is about 89% less than the fatigue damage ratio experienced by the package lead wires when the PCB assembly is mounted on plastic spacers. Thus, from the results it is evident that, by mounting PCBs on rubber spacers the fatigue damage ratio is reduced and the life of the package is improved.

Figure 8.12 $\sigma$ RMS stress plot in PSOP at PCB centre

Table 8.4 Fatigue damage estimation in PSOP lead wires due to random vibrations

<table>
<thead>
<tr>
<th>PCB assembly mounted on:</th>
<th>Sigma level</th>
<th>$n_i$ (cycles)</th>
<th>$N_i$ (cycles)</th>
<th>$n_i/N_i$</th>
<th>Cumulative damage $\Sigma n_i/N_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic Spacers</td>
<td>$1\sigma$</td>
<td>454878</td>
<td>$6.71 \times 10^{13}$</td>
<td>$6.78 \times 10^{-9}$</td>
<td>$7.20 \times 10^{-7}$</td>
</tr>
<tr>
<td></td>
<td>$2\sigma$</td>
<td>180486</td>
<td>$7.95 \times 10^{11}$</td>
<td>$2.27 \times 10^{-7}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$3\sigma$</td>
<td>28838</td>
<td>$5.93 \times 10^{10}$</td>
<td>$4.86 \times 10^{-7}$</td>
<td></td>
</tr>
<tr>
<td>Rubber Spacers</td>
<td>$1\sigma$</td>
<td>417996</td>
<td>$5.76 \times 10^{14}$</td>
<td>$7.26 \times 10^{-10}$</td>
<td>$7.71 \times 10^{-8}$</td>
</tr>
<tr>
<td></td>
<td>$2\sigma$</td>
<td>165882</td>
<td>$6.82 \times 10^{12}$</td>
<td>$2.43 \times 10^{-8}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$3\sigma$</td>
<td>26500</td>
<td>$5.09 \times 10^{11}$</td>
<td>$5.21 \times 10^{-8}$</td>
<td></td>
</tr>
</tbody>
</table>

$i=1\sigma, 2\sigma, 3\sigma$
8.4 RESULTS AND DISCUSSIONS

Lead wires of the DIP and PSOP packages are considered to be the critical elements in electronic package which succumb to failures due to vibration fatigue. In a vibration environment the lead wires are subjected to high cycle fatigue, and during every stress cycle a portion of the life is used up. From statistics it is proved that lead wires will fail because of high cycle vibration fatigue and solder joints will fail due to low cycle thermal fatigue (Steinberg 2001). Therefore, in this thesis the fatigue life of the lead wires due to vibrations alone was estimated.

The fatigue damage ratios for the DIP and PSOP lead wires due to sinusoidal vibrations are estimated. From the results it was found that the fatigue damage ratio of the lead wires of both DIP and PSOP, when PCB was mounted on rubber spacers is reduced by about 80% and 61.8% respectively compared to the fatigue damage ratio of the lead wires when the PCB was mounted on plastic spacers. The reason for the lower percent (61.8) of reduction in case of PSOP package is because of the high fundamental frequency of the PCB (340 Hz), due to which large number of cycles are accumulated within a short period of time.

Similarly, a reduction of about 99% in fatigue damage ratio is achieved in random vibration environment when DIP-PCB assembly was mounted on rubber spacers and about 89% reduction for the PSOP-PCB assembly. Thus, from these results, it is obvious that the rubber spacers may be effectively used to reduce the fatigue damage ratio of the critical components of the electronic package and improve their life.