CHAPTER 3

DESIGN AND IMPLEMENTATION OF ANALOG PFC
FOR SRM DRIVE

3.1 INTRODUCTION

The Switched Reluctance motor drive uses a diode bridge rectifier and a large filter capacitor on the front end. The switching of the voltage into phase windings of SRM and the discontinuous current in the input side results in low power factor and high input current harmonics. With the increasing demand for the better power factor, a power factor correction circuit with an SRM drive is necessary. To improve the power factor of the drive, PFC approaches have been presented.

In recent years, many research scholars showed interest in Power factor control of SRM drives. The power factor of the circuit is improved by using the boost converter circuit by the authors Corda, Krishnan, Geun-Hie Rim, Caruso, Frede Blaabjerg, Goyal and Helle. They have employed PI control, PID control or Hysteresis control methods for the Boost converter operation.

Anderson, Feel soon Kang, Helle have integrated the power factor circuit and machine converter circuit into single stage. The improvement in power factor, by changing the Switching angles is discussed by the authors Xue X D and Beno. Jun Oyama improves the power factor by changing the construction of SRM with a pair of permanent magnets attached on the rotor between poles. Jianing Liang reduces the torque ripple of single phase SRM
with PFC by adding one switching device and diode. Youn Hyun Kim improves the performance of single phase SRM with change in the LC parameters. Corda, Virendra Kumar Sharma, Consoli, Xue X D and Goyal done the analysis and simulation for power factor.

In the above said methods, the authors have discussed the analysis, simulation as well as experimental results for the PFC. From the reference papers mostly the authors have employed analog circuits for the improvement of PFC. The authors have employed different types of SR machine converter circuits like C-dump converters (Krishnan, Lee, Consoli, Cacciato) and Asymmetric converter (Corda, Frede Blaabjerg, Feel Soon Kang). They have also used different types of SR motor like Single phase SRM, 4/2 SRM, 6/4 SRM, 8/6 SRM.

From the above technical publications, it is found that a lot of research work is going in the improvement of power factor in SRM drive. In this thesis, an attempt is made to improve the power factor by employing a boost converter in both analog as well as digital methods. The boost converter is used to improve the input current waveform. The output of the boost converter is reduced to low machine operating voltage by using buck converter. This buck stage, consists of inverter, transformer and rectifier.

This chapter describes the hardware design and implementation of a power factor controller with closed loop speed control for prototype 6/4 pole SRM drive. In this research, the procedure to design the hardware is developed and implemented for the power factor controller.
3.2 POWER FACTOR CONTROLLER CIRCUIT

The SRM motor with power factor controller circuit consists of rectifier, boost and buck converter and SRM power converter as shown in Figure 3.1.

![Diagram of PFC circuit](image)

**Figure 3.1 Overall block diagram of PFC**

3.2.1 Design of Boost converter

The power factor controller is implemented in the input side of the SRM motor to improve the power factor. This power factor controller circuit uses a boost converter as shown in Figure 3.2. It uses current averaging method to maintain lower line current distortion both in continuous and discontinuous operation. It uses a multiplier that has a square gain function from the voltage amplifier to reduce AC gain at light output load and maintains low line current distortion. This power factor controller is designed to operate with single phase input supply and to produce an output voltage of 400V DC. The input voltage is normally 230 V with a peak voltage of 364 Volts. The output of the boost converter is normally selected as 400V (Rossetto L 1994).
The main components of boost converter of the PFC are boost inductor, power switch, blocking diode and output capacitor. The design is based on the parameters of the 6/4 pole SRM given in the appendix 1. The 6/4 pole SRM has an output Power ($P_0$) of 1.2 kW and voltage and current ratings of 160 V and 16 A.

The value of the Inductor is selected from the duty cycle, input voltage, switching frequency and change in current. The peak line current of this circuit is calculated by the equation given below,

$$I_{line}(pk) = \frac{\sqrt{2} P_0}{V_{in\ (min)} \eta}$$  \hspace{1cm} (3.1)$$

where,

- $I_{line}(pk)$ – Peak line current (Amps)
- $V_{in\ (min)}$ – Minimum RMS voltage (Volts)
- $\eta$ – Efficiency of the converter
Assume an efficiency of 90%

Substituting the values in equation (3.1).

\[ I_{\text{line (pk)}} = \frac{\sqrt{2} \times 1200}{150 \times 0.9} = 12.57\, \text{A} \]

The Duty cycle (D) is calculated from the input voltage and output DC voltage and is given by Keith (1989), Peter Wood (1932)),

\[ D = \frac{V_o - V_{in}}{V_o} \tag{3.2} \]

where,

\[ V_o \quad \text{output voltage (volts)} \]
\[ V_{in} \quad \text{Minimum peak input voltage (volts)} \]
\[ D = \frac{400 - 150 \sqrt{2}}{400} = 0.469 \]

The inductance is given by,

\[ L = \frac{V_{in} \sqrt{2} D}{f_s \Delta I} \tag{3.3} \]

where,

\[ f_s \quad \text{switching frequency} \]
\[ \Delta I \quad \text{Change in current} \]

The inductor is designed to limit the peak ripple current (\( \Delta I \)) within 20% of the peak input current.
The ripple current $\Delta I = 0.2 \ I_{\text{line(pk)}}$ (3.4)

$= 0.2 \ (12.57) = 2.514 \ \text{A}.$

The switching frequency is selected as 50 KHz. At this frequency the size of the inductor and capacitor are having less size and the losses in the devices are less.

$L = (150 \sqrt{2} \ (0.4698)) \ / \ ((50 \ (10^3) \ (2.514)) = 0.791 \ \text{mH}$

The nearest available value of inductor is 1 mH and it is chosen for the boost converter.

The output capacitor is selected depending on the factors such as switching frequency, ripple current, second harmonic ripple current, DC output voltage, output ripple voltage and hold up time (Ralph E. Tarter). The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current.

$C_o = \frac{2P_{out} \Delta t}{V_o^2 - V_{o(min)}^2}$ (3.5)

where

$C_o$ - output capacitor ( $\mu$F)

$P_{out}$ - load power ( watts)

$\Delta t$ - Hold up time (sec)

$V_o$ - output voltage (volts)

$V_{o(min)}$ - minimum output voltage (volts)

$C_o = (2 \ (1200)10 \ (10^3)) \ / \ (400^2 - 350^2) = 640 \ \mu$F.
The nearest available value of capacitor is 1000 \( \mu \text{F} \) and it is chosen for the boost converter.

**Calculation of current sensing resistor \( \text{R1} \):**

The maximum peak current flowing through the current sensing resistor is calculated from the formula (Philip C. Todd),

\[
I_{\text{pk}} \text{ (max)} = I_{\text{pk}} + \Delta I / 2 \\
= 12.57 + 2.514 / 2 \\
= 13.827 \text{ Amps.}
\]

The current sensing resistor value is given by,

\[
R_s = \frac{V_{rs}}{I_{pk} \text{ (max)}}
\]

where \( V_{rs} \) is the peak voltage across the resistor and it is taken as 2.0 volts.

Therefore, \( R_s = 2.0 / 13.827 \)

\( R_s = 0.15 \Omega \)

Nearest available standard value is 0.25\( \Omega \) and it is used as current sensing resistor.

**Calculation of voltage divider resistors (\( \text{R2 and R3} \)):**

The maximum value of the voltage across the output terminals of the boost converter output is 400V. The voltage across the resistance \( \text{R3} \) is chosen to be less than the voltage across the resistance \( \text{R2} \). The voltage across the \( \text{R3} \) is chosen to be 7.5 V.
\[
\left(\frac{400}{R_2 + R_3}\right) \times R_3 = 7.5
\]  \hspace{1cm} (3.8)

Solving the equation, we get the relationship between \( R_2 \) and \( R_3 \) as,

\[
R_3 = \frac{7.5 \times R_2}{392.5}
\]  \hspace{1cm} (3.9)

The value of \( R_2 \) is normally chosen as higher value compared to \( R_3 \). The value of \( R_2 \) is chosen as 1000 KΩ.

Nearest available standard value of resistance is 510 KΩ. Two resistors are connected in series and the total value will be 1020 KΩ. Substituting the value of \( R_2 \) of resistance as 1020 KΩ in equation (3.9)

\[
R_3 = 19.49 \text{ KΩ}.
\]

The voltage divider values are calculated as, \( R_2 \) is equal to 1022 KΩ and \( R_3 \) is equal to 20 KΩ.

3.2.2 Design of DC-DC Converter

The SRM motor is operated from low voltage to the maximum voltage of 160 V. A buck converter is used to reduce the boost converter output of 400 V to the SRM operating voltage as shown in Figure 3.3. It also provides isolation between input side and output side. It operates in variable frequency resonant mode zero voltage switching. A half bridge converter circuit is used in ZVS configuration.
In the half bridge, the switch peak voltages are clamped to the DC input link voltage. It will reduce the switch voltage stress compared to single ended converters operating in resonant mode zero voltage switching conditions.

When building a zero voltage switch circuit, the objective is to shape the power transistors voltage waveform so that the voltage across the transistor is zero when the device is turned on, still maintaining regulation. This is accomplished by maintaining a fixed dead time and by varying the frequency. Thus the effective duty cycle is changed.

The resonant frequency of the converter circuit is given by (Otmer Klingenstein),

$$f_r = \frac{1}{2\pi \sqrt{L_R 2C_R}}$$  \hspace{1cm} (3.10)

$$f_r = \frac{1}{2\pi \sqrt{(40 \times 10^{-6})2(4.7 \times 10^{-9})}}$$

$$= 367 \text{ kHz.}$$
The selection of Transformer depends upon the turns ratio, primary and secondary turns and the primary current.

The turns ratio of the transformer is given by,

\[
\text{Turns Ratio (n)} = \frac{V_{0(\text{max})} + V_F + V_{LS}}{\delta_{T(\text{max})} \cdot V_{in(\text{min})}}
\]

(3.11)

\[
= \frac{160 + 1.2 + 1.5}{0.4 \times 200} = \frac{162.7}{80} = 2.03
\]

where,

- \(V_{0(\text{max})}\) – Maximum output voltage (volts)
- \(V_F\) – Forward voltage drop (volts)
- \(V_{LS}\) – Choke voltage drop (volts)
- \(\delta_{T(\text{max})}\) – Maximum Duty cycle
- \(V_{in(\text{min})}\) – Minimum input voltage (volts)

The DC output voltage of the Boost converter is 400V. In Half bridge inverter the available voltage is 200V. Therefore, \(V_{in(\text{min})}\) is selected as 200 Volts.

The number of secondary turns is given by,

\[
N_S \geq \frac{\delta_{T(\text{max})} V_{p(\text{max})} n 10^4}{f A_{\text{min}} 2 \hat{B}}
\]

(3.12)

\[
\geq \frac{0.4 \times 200 \times 2.03 \times 10^4}{20 \times 10^3 \times 5.32 \times 0.3}
\]

\[
\geq 50.8
\]

\(\approx 51\) turns
The values of the frequency, Minimum cross section area and the flux density are taken from the references.

The total number of secondary turns is equal to 51 turns

where,

\[ \delta_T^{(\text{max})} \] - Maximum Duty cycle

\[ V_p^{(\text{max})} \] - Maximum peak voltage (volts)

\[ n \] - turns ratio

\[ f \] - frequency (Hz)

\[ A_{\min} \] - Minimum cross sectional Area (mm\(^2\))

\[ \hat{B} \] - flux density (Wb / mm\(^2\))

The number of primary turns is given by ,

\[ N_p = \frac{N_s}{n} \quad (3.13) \]

\[ N_p = \frac{51}{2.04} = 25 \text{ turns} \]

The primary current of the transformer is calculated from the load current, ripple current, magnetizing current and turns ratio and it is given by the equation ,

\[ I_{py} = (I_o + I_r) n + I_m \quad (3.14) \]

where ,

\[ I_{py} \] – Primary current (Amps)

\[ I_o \] – Load current (Amps)

\[ I_r \] – Ripple current (Amps)

\[ n \] – Turns ratio

\[ I_m \] – Magnetizing current (Amps)

\[ I_{py} = (10 + 1.1) (2.04) + 0.5 = 23.14 \text{ A.} \]
The MOSFET selected is IRFP 450. The Devices $C_1$ and $C_2$ are used for switching capacitors of the MOSFET. $R_2$ and $C_5$ are used as snubber circuit across the secondary of transformer. Diodes $D_3$ and $D_4$ are used for the unidirectional current flow and $C_3$ and $C_4$ are used as snubber capacitance. $C_7$ is used as filter capacitor. $L_2$ is used as filter choke. The Devices $R_1,C_6$ and $D_5$ are used in the snubber circuit.

### 3.2.3 Selection of Filter Components

The values of electrolytic capacitors used in the circuit are calculated from the Equivalent Series Resistance (ESR) and an Equivalent Series Inductance (ESL). The ESR is the resistance offered by the capacitor to alternating current flow. It generates heat within the capacitor, when an alternating current passes through it. It is normally specified for 100Hz at $20^\circ$C. Equivalent series inductance is usually in the order of few nano-henries and is denoted in $X_L$. The impedance of the capacitor $Z$ is given by

$$Z = \sqrt{ESR^2 - (X_L - X_C)^2}$$  \hspace{1cm} (3.15)

At the series resonant frequency the inductive reactance is equal to capacitive reactance and so the impedance is given as,

$$Z = \text{ESR}$$  \hspace{1cm} (3.16)

When the frequency is more than the series resonant frequency, the inductive reactance overtakes the capacitive reactance and the capacitor behaves like an inductor. The Dissipation factor ($\tan \delta$) for capacitor is defined as the ratio of the ESR to the capacitive reactance. It is also called as loss angle tangent.

$$\tan \delta = \frac{\text{ESR}}{X_C}$$

$$X_C = \frac{1}{2\pi fC}$$
Therefore,

$$\tan \delta = \text{ESR}(2\pi fC) \quad (3.17)$$

The dissipation factor increases with frequency. Ripple current rating of the capacitor is normally defined at 100 Hz at 85°C and the ripple current rating increases with increasing frequency. The ripple current is limited by the internal temperature rise within the capacitor as follows.

Power dissipated $P = I_{rip}^2 \cdot \text{ESR} \quad (3.18)$

and

$$P = \Delta T S \mu \quad (3.19)$$

where $\Delta T$ is the difference between ambient temperature and capacitor surface temperature, $S$ is the capacitor surface area ($\text{cm}^2$) and $\mu$ is the dissipation factor or thermal gradient ($\text{watt/cm}^2/\text{deg.C}$).

Therefore,

$$I_{rip} = \frac{\sqrt{\Delta T S \mu}}{\text{ESR}} \quad (3.20)$$

Electrolytic capacitors should be selected based on the above formula. At high frequencies the ESR & ESL offers higher impedance resulting in poor filtering. Hence multiple capacitors are recommended instead of a single capacitor.

The ferrite core inductances used are having inter winding capacitance, which allows a free path for switching frequency ripple and noise. It is complimented with a high frequency filter comprising an air core inductor and film foil capacitor along with electrolytic capacitor. This filter reduces switching frequency ripple and differential mode noise. To suppress the common mode noise generated during switching, a common mode filter comprising of common mode inductor and capacitors are used.
3.3 CALCULATION OF TEMPERATURE AND LOSSES

3.3.1 Calculation of Temperature and Losses in MOSFET (Boost Converter)

The selection of power switch depends upon the current rating and voltage rating. This power switch is selected based on the current rating at least equal to the maximum peak current of the inductor and a voltage rating equal to the output voltage. In this boost converter stage four MOSFET’s (IRFP450) are used in parallel. A soft recovery diode is used as blocking diode.

The input and output side filter components are smaller at higher operating frequencies. This reduction in size reduces the cost and increases the packaging density. The operating frequencies of the boost converter depend on the switching losses of MOSFET, output capacitance and reverse recovery current of the boost diode. The losses are more for frequencies higher than 100 kHz.

At higher power levels, use of normal fast recovery diode produces more switching losses. This will affect the controller performance by inducing radiated interference in the circuit, which may lead to failure of the circuit. To reduce this problem, soft recovery diode or slowing down the turn on process is employed. The temperature and losses in the MOSFET used in the boost converter is calculated by using the following formula.

The current through the MOSFET ($I_{\text{mosfet}}$) is given by,

$$I_{\text{mosfet}} = \sqrt{D} \frac{I_{\text{line}}p_k}{\sqrt{2}} \quad (3.21)$$

$$= \sqrt{0.469} \frac{12.57}{\sqrt{2}}$$

$$I_{\text{mosfet}} = 6.09 \text{A}$$
The conduction and switching losses of the MOSFET are calculated as below,

Conduction loss of the MOSFET \( (P_{\text{cond}}) = -I_m^2 \left( \frac{R}{n} \right) \) \hspace{1cm} (3.22)

\[ P_{\text{cond}} = (6.09)^2 \times (0.4)(1.75) / 4 = 6.5 \text{ W} \]

where,

\[ R = 0.4 \text{ @ } T_j = 25^\circ \text{c and } R = 0.4 \times 1.75 \text{ @ } T_j = 100^\circ \text{c} \]

\( n \)- Number of MOSFET's connected in parallel

Switching loss \( (P_{\text{switch}}) = V_o I_{\text{mosfet}} f \left( \frac{t_r + t_f}{2} \right) \) \hspace{1cm} (3.23)

\[ = 400 \times 6.09 \times 50 \times 10^3 \times (100 \times 10^{-9}) / 2 \]

\[ = 6.09 \text{ W} \]

where

\( V_o \) - Output voltage of the boost converter (volts)

\( I_{\text{mosfet}} \) - Current through the mosfet (Amps)

\( f \) - frequency (Hz)

\( t_r \) - rise time (sec)

\( t_f \) - fall time (sec)

The value of rise time and fall time are taken from the IRFP 450 datasheets.

The total loss of MOSFET is calculated from the summation of conduction loss and switching losses.

\[ \text{Total loss} \ (P_{\text{loss}}) = \text{Conduction loss} + \text{Switching loss} \] \hspace{1cm} (3.24)
= 6.5 + 6.09 = 12.59 Watts

The temperature of the junction of the device and the heat sink are calculated from the equations,

\[ T_j = (R_{(JC)} + R_{(CS)} + R_{(SA)}) \times P_{\text{loss}} + T_{\text{amb}} \]  \hspace{1cm} (3.25)

where,

\begin{align*}
R_{(JC)} & \quad \text{- Junction to case Resistance (°Celsius / Watts)} \\
R_{(CS)} & \quad \text{- Case to Heat sink Resistance (°Celsius / Watts)} \\
R_{(SA)} & \quad \text{- Heat sink to Ambient Resistance (°Celsius / Watts)} \\
T_j & \quad \text{- Junction temperature (°Celsius)} \\
T_{\text{amb}} & \quad \text{- Ambient temperature (@ 50° c) (°Celsius)} \\
P_{\text{loss}} & \quad \text{- Total loss in the MOSFET (Watts)}
\end{align*}

The values of \( R_{(JC)} , R_{(CS)} , R_{(SA)} \) are taken from the datasheets.

\[ T_j = \left( 0.65 + 0.24 + 3.5 \cdot \frac{63}{150} \right) \times 12.59 + 50 \]

\[ T_j = 79.7°C \]

The temperature of the Heat sink is calculated by,

\[ T_{hs} = R_{(SA)} \times P_{\text{loss}} + T_{\text{amb}} \]  \hspace{1cm} (3.26)

\[ T_{hs} = \left( 3.5 \cdot \frac{63}{150} \right) \times 12.59 + 50° = 68.51°C \]

3.3.2 Calculation of Temperature and Losses in Diode (Boost Converter)

The conduction and switching losses of the Diode are calculated by,

\[ \text{Conduction loss of the diode} \ (P_{\text{cond}}) = (1-D)I_{\text{ave}} V_f \]  \hspace{1cm} (3.27)
\[ P_{\text{cond}} = (1-0.469) \left( \frac{2}{\pi} \right) (12.59) (0.6) \]

\[ P_{\text{cond}} = 2.55 \text{ Watts} \]

Switching loss \( (P_{\text{switch}}) = \frac{Q_{rr} V_f f}{3.28} \)

\[ P_{\text{switch}} = 400 \times 10^{-9} \times 400 \times 50 \times 10^3 = 8 \text{ Watts} \]

where,

\[ V_f – \text{Diode drop (volts)} \]

\[ Q_{rr} – \text{Reverse recovery charge (coulomb)} \]

The total loss of Diode is calculated from the summation of conduction loss and switching losses.

\[ \text{Total loss } (P_{\text{loss}}) = \text{Conduction loss} + \text{Switching loss} \]

\[ = 2.55 + 8 = 10.55 \text{ Watts} \]

The junction temperature of the device and the heat sink are calculated from the following equations,

\[ T_j = (R_{\text{j}(JC)} + R_{\text{j}(CS)} + R_{\text{j}(SA)}) \times P_{\text{loss}} + T_{\text{amb}} \] \hspace{1cm} (3.29)

\[ T_j = \left( 0.65 + 0.24 + 3.5 \frac{63}{150} \right) \times 10.55 + 50 \]

\[ T_j = 108.7^\circ \text{C} \]

The temperature of the Heat sink is calculated by,

\[ T_{hs} = R_{\text{j}(SA)} \times P_{\text{loss}} + T_{\text{amb}} \] \hspace{1cm} (3.30)

\[ T_{hs} = \left( 3.5 \frac{63}{150} \right) \times 10.55 + 50^\circ = 96.5^\circ \text{C} \]
3.3.3 Calculation of Losses in MOSFET (DC-DC Converter)

The losses occurred in the MOSFET used in DC-DC converter is calculated from the following equations,

Conduction loss of the MOSFET ($P_{\text{cond}}$) = $I_m^2\left(\frac{R}{n}\right)$  

(3.31)

$P_{\text{cond}} = (2.94)^2(0.4)(1.75)/4 = 43.2$ W

The Switching loss ($P_{\text{switch}}$) in the MOSFET is zero, due to zero voltage switching of the device. The total loss of MOSFET is calculated from the summation of conduction loss and switching losses.

Total loss ($P_{\text{loss}}$) = Conduction loss + Switching loss

= 43.2 Watts

3.3.4 Calculation of Losses in Diode (DC-DC Converter)

The losses occurred in the Diode which is used in ZVS DC-DC converter is calculated from the following equations,

The conduction and switching losses of the Diode are calculated by,

Conduction loss of the diode ($P_{\text{cond}}$) = $I_0 V_f D$

(3.32)

$P_{\text{cond}} = 10 \times 0.6 \times 0.4$

$P_{\text{cond}} = 2.4$ Watts

Switching loss ($P_{\text{switch}}$) = $Q_{rr}V_f f$

(3.33)

$P_{\text{switch}} = 0.1 \times 10^{-6} \times 180 \times 20 \times 10^3 = 0.36$ Watts

Total loss ($P_{\text{loss}}$) = Conduction loss + Switching loss

= 2.4 + 0.36 = 2.76 Watts
3.4 EXPERIMENTAL RESULTS

The Switched reluctance motor is coupled with a DC shunt generator as shown in Figure 3.4. The closed loop speed control of SRM is done with the use of Digital signal processor as shown in Figure 3.5. The program written in DSP is given in the appendix 2. The variation in load or change in the input side voltage variation does not affect the set speed of the motor. The set speed and measured speed are captured by using the Digital storage oscilloscope. Figure 3.6 shows the flow chart of the closed loop speed control. The speed of the motor is found from the rotor position signals. The signals from the rotor position sensors are taken and it is given to the frequency to voltage converter. Each division in the Y axis in the figures from 3.7 to 3.10 is equal to 500 RPM.

![Figure 3.4 SRM with loading arrangement](image1.png)

![Figure 3.5 SRM Closed loop speed control](image2.png)
The closed loop speed control was performed with different control methods like PI, PD and PID. The PID controller is found to give the minimum error. The load condition at which minimum error occurs is implemented.
Figure 3.7 Variation of speed in two steps: From 500 RPM to 800 RPM.

Figure 3.8 Increment of speed from 500 RPM - 900 RPM - 1400 RPM.
Figure 3.9  Constant set speed and measured speed during a variation in the load current from zero current to 1.6 Amps

Figure 3.10  Constant set speed and measured speed during a variation in the load current in three steps – zero – 2 Amps -3.2 Amps

Figure 3.7 shows the speed variation of set speed and measured speed in one step. The speed is varied from 500 RPM to 800 RPM. Figure 3.8
shows the speed variation in three steps from 500 RPM to 900 RPM and then to 1400 RPM. Figure 3.9 shows that the variation in the load from zero amps to 1.6 amps, there is no change in measured speed. Figure 3.10 shows that change in current in two steps from zero current to 2 amps and then to 3.2 amps. The speed of the SRM is maintained constant during the loaded conditions.

Figures 3.11 - 3.14 show the details of the experimental results obtained without and with power factor controller. It shows the voltage and current waveforms, current harmonic spectrum, details of power, voltage and current values for an input DC voltage of 60 V, 80V, 100V and 120V for a load current of 5.6 A.

The experimental results are taken for various DC input voltages and different load currents with closed loop speed control. Tables 3.1 - 3.4 shows the readings taken for different DC input voltage to the SRM for 60V, 80V, 100V and 120V. Figures 3.15, 3.17, 3.19 and 3.21 shows the relationship between the load current and power factor for with and without power factor controller for different DC input voltages to SRM for 60V, 80V, 100V and 120V. Figures 3.16, 3.18, 3.20 and 3.22 shows the relationship between the load current and percentage total harmonic distortion for with and without power factor controller for different DC input voltages to SRM for 60V, 80V, 100V and 120V.

From the results shown in Tables 3.1 and 3.4, it is observed that the power factor of the circuit is improved with the designed power factor controller. The total harmonic distortion of the circuit is also reduced with power factor controller. Table 3.5-3.6 shows the individual harmonics of the motor with and without power factor controller. From these results it is observed that, the individual harmonics of the system is reduced with the power factor controller.
Figure 3.11  Experimental results at DC input voltage of 60 V and Load current of 5.56 A (Without and With PFC)
Figure 3.12 Experimental results at DC input voltage of 80 V and Load current of 5.56 A (Without and With PFC)
Figure 3.13  Experimental results at DC input voltage of 100 V and Load current of 5.56 A (Without and With PFC)
Figure 3.14 Experimental results at DC input voltage of 120 V and Load current of 5.56 A (Without and With PFC)
Table 3.1  Power factor and % THD at various loads without PFC and PFC for a Input DC Voltage of 60 V

<table>
<thead>
<tr>
<th>Load current (Amps)</th>
<th>Power factor</th>
<th>% THD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>1.3</td>
<td>0.55</td>
<td>0.85</td>
</tr>
<tr>
<td>2.9</td>
<td>0.59</td>
<td>0.92</td>
</tr>
<tr>
<td>3.8</td>
<td>0.60</td>
<td>0.94</td>
</tr>
<tr>
<td>4.7</td>
<td>0.64</td>
<td>0.96</td>
</tr>
<tr>
<td>5.56</td>
<td>0.62</td>
<td>0.96</td>
</tr>
<tr>
<td>6.5</td>
<td>0.63</td>
<td>0.95</td>
</tr>
<tr>
<td>7.5</td>
<td>0.64</td>
<td>0.94</td>
</tr>
</tbody>
</table>

Figure 3.15 Comparison of load current vs %THD for 60 V

Figure 3.16 Comparison of load current vs Power factor for 60 V
Table 3.2 Power factor and % THD at various loads without PFC and PFC for a Input DC Voltage of 80 V

<table>
<thead>
<tr>
<th>Load current (Amps)</th>
<th>Power factor</th>
<th>% THD</th>
<th>Power factor</th>
<th>% THD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>1.3</td>
<td>0.57</td>
<td>0.87</td>
<td>108.1</td>
<td>14.8</td>
</tr>
<tr>
<td>2.86</td>
<td>0.59</td>
<td>0.9</td>
<td>109.8</td>
<td>14.3</td>
</tr>
<tr>
<td>3.81</td>
<td>0.60</td>
<td>0.91</td>
<td>113.5</td>
<td>13.7</td>
</tr>
<tr>
<td>4.7</td>
<td>0.61</td>
<td>0.85</td>
<td>113.8</td>
<td>14.8</td>
</tr>
<tr>
<td>5.56</td>
<td>0.63</td>
<td>0.95</td>
<td>113.7</td>
<td>11.9</td>
</tr>
<tr>
<td>6.5</td>
<td>0.63</td>
<td>0.96</td>
<td>112.8</td>
<td>11.0</td>
</tr>
<tr>
<td>7.5</td>
<td>0.64</td>
<td>0.97</td>
<td>109.4</td>
<td>10.5</td>
</tr>
</tbody>
</table>

Figure 3.17 Comparison of load current vs power factor for 80 V

Figure 3.18 Comparison of load current vs %THD for 80 V
Table 3.3 Power factor and % THD at various loads without PFC and PFC for a Input DC Voltage of 100 V

<table>
<thead>
<tr>
<th>Load current (Amps)</th>
<th>Power Factor</th>
<th>% THD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>3.8</td>
<td>0.61</td>
<td>0.92</td>
</tr>
<tr>
<td>4.7</td>
<td>0.62</td>
<td>0.94</td>
</tr>
<tr>
<td>5.6</td>
<td>0.61</td>
<td>0.94</td>
</tr>
<tr>
<td>6.5</td>
<td>0.62</td>
<td>0.95</td>
</tr>
<tr>
<td>7.5</td>
<td>0.64</td>
<td>0.97</td>
</tr>
<tr>
<td>8.5</td>
<td>0.66</td>
<td>0.98</td>
</tr>
</tbody>
</table>

Figure 3.19 Comparison of load current vs power factor for 100 V

Figure 3.20 Comparison of load current vs %THD for 100 V
Table 3.4  Power factor and % THD at various loads without PFC and PFC for a Input DC Voltage of  120 V

<table>
<thead>
<tr>
<th>Load current (Amps)</th>
<th>Power Factor</th>
<th>% THD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>4.7</td>
<td>0.62</td>
<td>0.96</td>
</tr>
<tr>
<td>5.6</td>
<td>0.62</td>
<td>0.96</td>
</tr>
<tr>
<td>6.5</td>
<td>0.63</td>
<td>0.96</td>
</tr>
<tr>
<td>7.5</td>
<td>0.65</td>
<td>0.97</td>
</tr>
<tr>
<td>8.5</td>
<td>0.66</td>
<td>0.98</td>
</tr>
</tbody>
</table>

Figure 3.21  Comparison of load current vs power factor for 120 V

Figure 3.22 Comparison of load current vs %THD for 120 V
### Table 3.5 Input current harmonics for input DC Voltage of 60 V

<table>
<thead>
<tr>
<th>Current Harmonic number</th>
<th>Load current (Amps)</th>
<th>4.7 A</th>
<th>5.6 A</th>
<th>6.5 A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>05</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>80</td>
<td>10</td>
<td>85</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>13</td>
<td>01</td>
<td>15</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>65</td>
<td>03</td>
<td>65</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>10</td>
<td>01</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>35</td>
<td>03</td>
<td>35</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>05</td>
<td>01</td>
<td>05</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>20</td>
<td>0</td>
<td>20</td>
<td>0</td>
</tr>
</tbody>
</table>

### Table 3.6 Input current harmonics for input DC Voltage of 80 V

<table>
<thead>
<tr>
<th>Current Harmonic number</th>
<th>Load current (Amps)</th>
<th>4.7 A</th>
<th>5.6 A</th>
<th>6.5 A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without PFC</td>
<td>With PFC</td>
<td>Without PFC</td>
<td>With PFC</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td>5</td>
<td>20</td>
<td>05</td>
</tr>
<tr>
<td>3</td>
<td>75</td>
<td>10</td>
<td>80</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>15</td>
<td>2</td>
<td>15</td>
<td>01</td>
</tr>
<tr>
<td>5</td>
<td>60</td>
<td>5</td>
<td>60</td>
<td>03</td>
</tr>
<tr>
<td>6</td>
<td>10</td>
<td>0</td>
<td>10</td>
<td>01</td>
</tr>
<tr>
<td>7</td>
<td>40</td>
<td>5</td>
<td>35</td>
<td>02</td>
</tr>
<tr>
<td>8</td>
<td>05</td>
<td>0</td>
<td>05</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>25</td>
<td>2</td>
<td>20</td>
<td>0</td>
</tr>
</tbody>
</table>
Figure 3.23 shows the attachment of slotted rotor disc in which the photo diode and photo transistors are connected. Figure 3.24 shows the Connection of the photo transistor output to the combinational logic circuit. Figure 3.25 shows the power circuit of the SRM. Figure 3.26 shows the overall model of the Power circuit and SRM.

Figure 3.23  Rotor position arrangements

Figure 3.24  Rotor position signals from motor to logic circuit
Figure 3.25  Power circuit model

Figure 3.26  Overall arrangement of SRM
3.5 SUMMARY

In this chapter, a SRM drive system with power factor controller circuit in closed loop speed control is designed and implemented. The design procedure is given for the various components of the power factor correction circuit. The experimental results are taken for various DC input voltages to the SRM and for various load currents with closed loop speed control. From the results, it is clearly seen that the total current harmonic distortion and individual current harmonics are very much less with power factor controller. The power factor of the circuit is also improved with the power factor controller, thereby confirming the results obtained from simulation.