CHAPTER 2

SIMULATION METHODOLOGY AND PARAMETER EXTRACTION PROCEDURE

Initially the simulator details are discussed in this chapter. Then the procedure to create device structure, to do device simulation, and to extract DC parameters such as threshold voltage, ON current, OFF current and sub-threshold swing, and AC parameters, unity gain cutoff frequency of the device are discussed.

2.1 INTRODUCTION

Technology computer aided design (TCAD) affords a major benefit to IC technologists and circuit designers in that the details of circuit dependencies on technological and layout aspects can be investigated (Dutton 1993). TCAD is an electronic design automation tool that models the semiconductor device operation and fabrication based on basic physics through the numerical simulations for design and optimization of semiconductor processing technologies and devices. TCAD is used to analyze how structural factors such as geometry and process conditions influence the electrical behaviour of devices. TCAD tools played a main role in the development of new technology creations (Dutton & Strojwas 2000).

For the deep sub micrometer devices, TCAD represents a better approach than any measurement techniques, and they have become indispensible in new device creation. Basic physical partial differential
equations, such as diffusion and transport equations for discretized geometries are solved by TCAD, representing the silicon wafer or the layer system in a semiconductor device. This deep physical approach provides TCAD simulation predictive accuracy. It is therefore, possible to substitute TCAD simulations for expensive and extensive test wafer runs when developing and characterizing a new semiconductor device or technology. Hence TCAD simulations are commonly used all over the semiconductor industries. The semiconductor industry relies increasingly more on TCAD to cut costs and speeds up the research and development process.

2.2 SENTAURUS TCAD

Sentaurus TCAD simulator from Synopsys is used for the simulations (Synopsys, 2012-06). The important modules of this simulator are:

- **Sentaurus Structure Editor (SDE)**
  - Sentaurus Structure Editor is a structure editor, which can be used to build 2D and 3D device structures. The contact sets are defined and the contact placement is done in SDE. It has built-in, analytical profiles allowing user to define doping and algorithms for meshing the device.

- **Sentaurus Device (SDEVICE)**
  - Sentaurus Device simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit.

- **Inspect**
  - Inspect is a plotting and analysis tool for xy data, such as doping profiles and electrical characteristics of semiconductor devices. Inspect is a tool that is used to display and analyze curves.
Sentaurus Visual (SVISUAL)

- Sentaurus Visual is a part of Sentaurus Workbench Visualization. It is plotting software with extensive 2D and 3D capabilities for visualizing data from simulations and experiments.

Figure 2.1 shows the flow diagram of input and output files in SDE and SDEVICE.

**2.2.1 Calibrating TCAD simulation against fabricated device**

The TCAD simulator has been calibrated against the fabricated device. Figure 2.2 shows the calibrated results on n-type trigate Junctionless FETs $I_D-V_{GS}$ data from (Lee, CW et al. 2010). Transport properties are modeled using Drift-Diffusion, Philips Unified Mobility, and Lombardi Mobility Degradation models at interface. Values of the physical parameters used for the mobility are tuned to calibrate the TCAD simulation against fabricated device. Values of the physical parameters used for the mobility are given below.

**Doping–dependent Mobility:**

$$\mu_{dop} = \mu_{min1} \exp\left(\frac{P_e}{(N_{A0} + N_{D0})}\right) + \frac{\mu_{constr} - \mu_{min2}}{1 + \left(\frac{(N_{A0} + N_{D0})}{C_p}\right)^{\alpha}} \left(1 + \left(\frac{C_{s}}{(N_{A0} + N_{D0})}\right)^{\beta}\right)$$
where, \( \mu_{\text{min1}} = 56 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right] \), \( \mu_{\text{min2}} = 56 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right] \), \( \mu_1 = 43.4 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right] \), \( P_c = 0 \text{cm}^{-3} \).

\[ C_r = 9.68 \times 10^4 \text{cm}^{-3}, C_s = 3.43 \times 10^6 \text{cm}^{-3}, \alpha = 0.68 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right], \beta = 2 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right] . \]

Enhanced Lombardi Model:

\[
\frac{1}{\mu} = \frac{D}{\mu_{\text{ac}}} + \frac{D}{\mu_{\text{rr}}},
\]

\[
\mu_{\text{ac}} = \frac{B}{F_\perp} + e^{\left( \frac{N_0 + N_D + N_s}{N_s} \right)^{\frac{1}{2}}}, \quad \mu_{\text{rr}} = \left( \frac{F_{\text{ref}}}{\delta} + e^{\frac{\delta}{\eta}} \right)^{-1},
\]

where, \( B = 3.6 \times 10^5 \left[ \frac{\text{cm}^2}{\text{s}} \right], A = 2.58, C = 1.700 \times 10^4 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right], D = \exp \left( \frac{V}{l_{\text{crit}}} \right), \text{ where } x \text{ is the distance from the interface } \text{ and } l_{\text{crit}} = 1 \times 10^6 \left[ \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \right]. \]

\( F_\perp = \text{transverse electric field normal to semiconductor-insulator interface}. \)

![Figure 2.2](image-url)  

**Figure 2.2**  

\( I_D - V_G \) characteristics of trigate Junctionless FET

### 2.3 EXTRACTION OF PARAMETERS

#### 2.3.1 Extraction of DC Parameters

The saturation \( I_D - V_G \) characteristics are plotted and to extract ON current (\( I_{\text{ON}} \)), OFF current (\( I_{\text{OFF}} \)), Trans-conductance (\( g_m \)), Threshold voltage (\( V_{\text{TH}} \)) and Sub-threshold swing (SS).
When drain voltage is at maximum ($V_{DD}$) and the gate voltage is zero, $I_{OFF}$ is extracted as given in Figure 2.3.

![Figure 2.3 Extraction of OFF current]

As shown in Figure 2.4, $I_{ON}$ is extracted when both the gate and drain voltages are kept maximum. $V_{TH}$ has been extracted by the constant current method, taken as the point in which the gate voltage is at which the drain current density goes above a given current level, 100nA/µm in this case. 100nA/µm current level is chosen since it is used commonly to extract the threshold voltage as per the industry standard. By taking the derivative of the
I_D-V_G curve from the saturation I_D-V_G characteristics, g_m is extracted. From the I_D-V_D characteristics, R_O is extracted at the bias point of V_DD/2.

2.3.2 Extraction of AC Parameter (f_T)

Sentaurus Device computes the Y-matrix in a small-signal analysis simulation. The Y-matrix explains how the currents in a circuit react as the applied voltages at different contact nodes of the circuit are modified. The current and voltage can be represented for any two-port network in matrix form as follows,

\[
\begin{bmatrix}
  i_1 \\
  i_2
\end{bmatrix} = \begin{bmatrix}
  Y_{11} & Y_{12} \\
  Y_{21} & Y_{22}
\end{bmatrix} \times \begin{bmatrix}
  V_1 \\
  V_2
\end{bmatrix}
\]

(2.1)

The AC simulation output of the SDEVICE has the following form

\[
\begin{bmatrix}
  (a_{11}, c_{11}) & (a_{12}, c_{12}) \\
  (a_{21}, c_{21}) & (a_{22}, c_{22})
\end{bmatrix}
\]

(2.2)

This is interpreted in the following way

\[
\begin{bmatrix}
  i_1 \\
  i_2
\end{bmatrix} = \begin{bmatrix}
  (a_{11} + jωc_{11}) & (a_{12} + jωc_{12}) \\
  (a_{21} + jωc_{21}) & (a_{22} + jωc_{22})
\end{bmatrix} \times \begin{bmatrix}
  V_1 \\
  V_2
\end{bmatrix}
\]

(2.3)

The complex Y-matrix can be divided into two parts: the in-phase response of the current with the voltage is measured by the real part ‘a’ (conductance matrix), the imaginary part ‘c’ (capacitance matrix) measures the out-phase response.
The symbol $j = \sqrt{-1}$ denotes the imaginary part of a complex variable and $\omega$ signifies the frequency of the small-signal change. Standard AC simulations are done in SDEVICE and AC simulations yield $Y$ parameter matrix. $f_T$ is the frequency at which $\left| \frac{Y_{21}}{Y_{11}} \right|$ equals one, which is strongly depends on the gate voltage. $f_T$ is calculated at various gate biases, and the maximum of them is taken as $f_T$. Figure 2.5 depicts the graph of the variation of $f_t$ with respect to gate bias.

![Graph of $f_T$ versus gate bias](image)

**Figure 2.5 Typical graph of $f_T$ versus gate bias**

### 2.4 SUMMARY

Since this thesis work is based on TCAD simulation usage of various modules, their capabilities have been discussed in this chapter with block diagram. Simulation methodology and extraction of AC, DC parameters have been discussed with flow charts.