CHAPTER 6

SENSITIVITY OF SILICON NANOTUBE FIELD EFFECT TRANSISTORS TO STRUCTURAL PROCESS PARAMETERS

In this chapter, we have studied the impact of various geometrical parameters on the performance of junction and junctionless based Silicon Nanotube Field Effect Transistor. When we go for mass production, process variations are inevitable, and the SiNT-FETs are of no exception. Process variation studies are meant to identify the most significant parameters in deciding the performance. The performance parameters, ON current, OFF current, Sub-threshold swing, Threshold voltage and unity gain cutoff frequency ($f_T$) are extracted for six different structural factors, gate length, gate oxide thickness (inner and outer), tube wall thickness (using inner diameter and using outer diameter), and tube ovality. Sensitivity of these parameters over a range is also computed by performing ±10% variations in these parameters, at various points in the range. Following this, a two level full factorial design of experiment method is used to find out the ranking of these parameters for various performance parameters. The parameter placed against the 1st rank affects the device performance most significantly, and therefore needs tight process control.

6.1 INTRODUCTION

Process induced variations are inevitable in the device manufacturing. Even a small decrement in gate oxide thickness can lead to
such a gate leakage that is unacceptable for device operation (Khan et al. 2008). So it is very important to analyze the impact of process variations on device performance. Many researchers have analyzed the impact of process variations on devices (Choi et al. 2007; Choi et al. 2002; Khan et al. 2008; Thakker et al. 2010). Xiong & Bokor (2003) have discussed in detail the impact of process variations and the sensitivity of a 20 nm double gate (DG) FET and FinFET by using Monte Carlo simulation. Statistical modeling techniques have been proposed to relate the circuit and device variability to the underlying semiconductor processes (Srinivasaiah & Bhat 2003; Harish et al. 2007). The effect of process variations on the timing response of nanometer digital circuits was discussed by Freijedo et al. (2011). Sensitivity of GAA MOSFETs to process variations is explored in (Yu-Sheng Wu et al. 2008a; Nathan Conrad et al. 2013). Scalability and process induced variation analysis on nanowire are given in (Chitrakant Sahu et al. 2016; Bipul, C et al. 2007). The impact of process variations on the vertical silicon nanowire tunneling FET is studied in (Chen,ZX et al. 2013). Small signal parameter extraction of junctionless Silicon nanowire MOSFETs was done in (Seongjae Cho et al. 2011).

As the SiNT-FET has better scalability over silicon nanowire, it is important to study the process variations of SiNT-FET device. The gate length dependency and tube wall thickness dependency on the output parameters of SiNT-FET and is presented in reference (Daniel Tekleab 2014). Apart from gate length and tube wall thickness, the parameters, gate oxide thickness and tube ovality also affect the device characteristics. Moreover, the study in (Daniel Tekleab 2014) is at the qualitative level. A systematic study of process variations including the important structural parameters such as gate oxide thickness for inner and outer gates, tube ovality of SiNT-FET and JLSiNT-FET is yet to be reported and we have attempted to address this. The block diagram in Figure 6.1 shows that the variation in process parameters
results in the variation of geometrical parameters of the device such as gate length, gate oxide thickness, tube wall thickness and ovality of the device. This in turn leads to variation in the electrical parameters of the device, eventually resulting in output parameter fluctuations as depicted in Figure 6.1.

![Diagram showing process variations leading to device parameters](image)

**Figure 6.1** Impact of geometrical process variations on device output parameters

### 6.2 MOTIVATION, CONTRIBUTION AND ORGANIZATION

As the SiNT-FET has better scalability over SiNW-FET, it is important to study the process variations of SiNT-FET device. A systematic study of process variations including the important structural parameters such as gate oxide thickness for inner and outer gates, tube ovality of SiNT-FET and JLSiNT-FET are yet to be reported and we have attempted to address this.

This chapter has two parts,
To study the impact of various geometrical parameters on the performance of junction and junctionless based SiNT-FETs and to analyze the sensitivity of these parameters over a range.

To find out the ranking of the structural parameters for various performance parameters using two level full factorial design of experiment method.

The contribution block diagram of this chapter is given in the following Figure 6.2.

![Block diagram of the chapter 6](image)

**Figure 6.2 Block diagram of the chapter 6**

Rest of the chapter is organized as follows. Section 6.3 deals with the device description and calibration. In section 6.4, the sensitivity analysis, over a range for different structural factors are discussed. Ranking of structural factors based on DOE method is discussed in Section 6.5. Finally, conclusions are provided in Section 6.6.

### 6.3 DEVICE STRUCTURE AND $I_D-V_G$ CALIBRATION

The devices discussed (SiNT-FET and JLSiNT-FET) in chapter 3 are taken for this study. Figure 6.3 (a) shows the TCAD generated SiNT-FET
device. Figure 6.3 (b) shows the SiNT-FET with gate oxide and spacer removed i.e. silicon portion alone is depicted. Figure 6.3(c) shows the schematic vertical cross section of SiNT-FET device. Figure 6.3 (d) shows the schematic circular cross section of the SiNT-FET device. (Figure 6.3 (a-d) are already given in chapter 4 and are repeated here for better readability). The $I_D$-$V_G$ characteristics of SiNT-FET (Daniel Tekleab 2014) is given in Figure 6.4.

Figure 6.3 (Continued)
Figure 6.3 (Continued)

(a) SiNT-FET structure showing all the regions, (b) Silicon portion alone of SiNT-FET structure, (c) Schematic vertical cross section of SiNT-FET, (d) Schematic circular cross section of SiNT-FET device
Figure 6.4  \( I_D-V_G \) characteristics of SiNT-FET [Daniel Tekleab 2014]

JLSiNT-FET (discussed in chapter 3) is taken in this study (Figure 6.5 is repeated from chapter 3 for better readability). The JLSiNT-FET's \( I_D-V_G \) characteristics plot is given in Figure 6.6.

Figure 6.5(a) JLSiNT-FET device structure showing all the regions, (b) Silicon portion alone of JLSiNT-FET device
6.4 SENSITIVITY ANALYSIS OF SINT-FET'S STRUCTURAL FACTORS

The structural dimensions of SiNT-FET, gate length ($L_G$), inner gate oxide thickness ($T_{OX\_IN}$), outer gate oxide thickness ($T_{OX\_OUT}$), tube wall thickness ($T_{SI}$), and tube ovality ($\varnothing$), are varied over a range, and their impact on $I_{ON}$, $I_{OFF}$ and $f_T$ are studied using sensitivity analysis. It should be noted that the $T_{SI}$ is changed either by changing the outer diameter (OD) (for constant inner diameter), or by changing the inner diameter (ID) (for constant outer diameter) of the tube.

Sensitivity analysis is carried out by varying one parameter at a time (for $\pm 10\%$ variations) by keeping the other parameters constant. The following expression is used to compute the sensitivity:

$$S_y(x) = \left| \frac{\Delta y \cdot y}{\Delta x \cdot x} \right|,$$

(6.1)
where $\Delta y$ is the change in the output parameters ($I_{ON}$, $I_{OFF}$ and $f_T$) and $\Delta x$ is the change in the input parameters ($L_G$, $T_{OX,IN}$, $T_{OX,OUT}$, $T_{SL,IN}$, $T_{SL,OUT}$ and $\varnothing$).

6.4.1 Sensitivity Analysis of Junction Based SINT-FET

6.4.1.1 Impact on $I_{ON}$ AND $I_{OFF}$

Impact of junction based SiNT-FETs structural parameters on $I_{ON}$ and $I_{OFF}$ is discussed in this subsection. Variation of $I_{ON}$ is plotted against $L_G$, $T_{OX,IN}$, $T_{OX,OUT}$, $T_{SL,IN}$, $T_{SL,OUT}$ and $\varnothing$ and are given in Figures 6.7-6.10. The range of the parameters is given in Table 6.1. In this range, their sensitivities are calculated at various points while perturbing the respective inputs by $\pm10\%$. Sensitivity as a function of $L_G$, $T_{OX,IN}$, $T_{OX,OUT}$, $T_{SL,IN}$, $T_{SL,OUT}$ and $\varnothing$ are also plotted in the following graphs (Figures 6.7-6.14).

![Image of $I_{ON}$ and its sensitivity as a function of $L_G$](image)

**Figure 6.7 $I_{ON}$ and its sensitivity as a function of $L_G$**
When \( L_G \) decreases \( I_{ON} \) is expected to increase and can be observed from Figure 6.7. Figure 6.8 shows the \( I_{ON} \) and its sensitivity as a function of \( T_{OX} \). Since there are two gate oxides, inner and outer, we have the following
two cases; (i) varying $T_{\text{OX,OUT}}$ (for constant $T_{\text{OX,IN}}$) (ii) varying $T_{\text{OX,IN}}$ (for constant $T_{\text{OX,OUT}}$). It can be observed from Figure 6.8 that $I_{\text{ON}}$ decreases rapidly when $T_{\text{OX,OUT}}$ increases compared to $T_{\text{OX,IN}}$. The sensitivity is also higher for $T_{\text{OX,OUT}}$. The $T_{\text{OX,OUT}}$ and $T_{\text{OX,IN}}$ can be converted into effective gate oxide thicknesses using, $a_1 \ln(b_1/a_1)$ and $a_2 \ln(b_2/a_2)$ respectively, where $a_1$, $b_1$, $a_2$, and $b_2$ are as shown in Figure 6.3(d). From the above discussions, it follows that the rate of decrease in effective gate oxide thickness is more when $T_{\text{OX,OUT}}$ is increased compared to $T_{\text{OX,IN}}$ i.e. $T_{\text{OX,OUT}}$ is more sensitive to $I_{\text{ON}}$ compared to $T_{\text{OX,IN}}$, as can be seen from Figure 6.8. For thick gate oxides, both $T_{\text{OX,OUT}}$ and $T_{\text{OX,IN}}$ exhibit same sensitivities.

![Figure 6.9 $I_{\text{ON}}$ and its sensitivity as a function of $T_{\text{SI}}$](image)

Figure 6.9 $I_{\text{ON}}$ and its sensitivity as a function of $T_{\text{SI}}$
Figure 6.10 $I_{\text{ON}}$ and its sensitivity as a function of $\varnothing$

Figure 6.11 $I_{\text{OFF}}$ and its sensitivity as a function of $L_G$
Figure 6.12 $I_{OFF}$ and its sensitivity as a function of $T_{OX}$

Figure 6.13 $I_{OFF}$ and its sensitivity as a function of $T_{SI}$
Figure 6.9 shows $I_{ON}$ and its sensitivity as a function of $T_{SI}$ for SiNT-FET device. As stated earlier, the tube wall thickness may be changed either by changing OD keeping ID constant or by changing the ID keeping OD constant. Intuitively we expect the device current to go up when ID is constant (in this case OD increases to increase $T_{SI}$ resulting in more channel width) and similarly, we expect the current to go down when OD is kept constant (because ID should decrease to increase $T_{SI}$ resulting in less channel width). This argument is true when we deal with the absolute current values and it is not true for normalized current values. The normalization current depends upon both the absolute current and the normalization factor (which pre-multiplies the absolute value). Both for ID constant and OD constant cases it is found out that the normalization currents go up when $T_{SI}$ increases. It can also be noted from Figure 6.9 that more sensitivity is observed for constant ID compared to constant OD.

Figure 6.10 depicts the $I_{ON}$ and its sensitivity as a function of $\varnothing$ (ratio between major axis to minor axis). Tube is planned to be a perfect circular shape but it will end up with oval shape by the fabrication processes. Hence we are varying $\varnothing$ of the tube to capture that effect in device characteristics. The perfect circular tube shape occurs when $\varnothing$ is 1 otherwise the oval shape occurs. It can be observed from Figure 6.10 that $I_{ON}$ increases when $\varnothing$ increases due to the increase in channel width. The device is more sensitive at $\varnothing = 1$. 
Figure 6.14 $I_{OFF}$ and its sensitivity as a function of $\phi$

Figures 6.11-6.14 depict $I_{OFF}$ versus various parameters along with their sensitivity. Figure 6.11 exhibits usual $I_{OFF}$ versus $L_G$ characteristics. Similarly Figure 6.12 shows usual $I_{OFF}$ versus $T_{OX}$ plots i.e. when $T_{OX}$ increases, the gate control on the channel reduces, and hence, $I_{OFF}$ increases. When $T_{Si}$ increases leakage cross section increases to increase $I_{OFF}$ (Figure 6.13). $I_{OFF}$ versus $\phi$ is given in Figure 6.14. It can be seen from Figure 6.14 that $I_{OFF}$ increases when $\phi$ increases since the gate control on the channel reduces.
6.4.1.2 Impact on unity gain cut-off frequency ($f_T$)

Unity gain cut-off frequency ($f_T$) is an important metric for RF applications and in terms of device parameters as discussed in chapter 2 already. $f_T$ is given by,

$$f_T = \frac{g_m}{2\pi C_{gg}}, \quad (6.2)$$

where, $g_m$ is the trans-conductance, $C_{gg}$ is the combination of gate to source capacitance ($C_{gs}$), gate to drain capacitance ($C_{gd}$), and overlap capacitance ($C_{ov}$). $f_T$ is extracted from the standard AC simulations, when $\left|\frac{Y_{21}}{Y_{11}}\right|$ equals one. At various gate biases, $f_T$ is calculated and the maximum of them is taken as $f_T$. 

Figure 6.15 $f_T$ and its sensitivity as a function of $L_G$
Figure 6.15 depicts $f_T$ versus $L_G$ plot. As expected $f_T$ increases as $L_G$ decreases, and the simulation results match with the $1/L_G$ trend with a regression coefficient of 0.911. $f_T$ sensitivity also increases as $L_G$ increases. $f_T$ as a function of $T_{OX,\text{OUT}}$ and $T_{OX,\text{IN}}$ are shown in Figure 6.16. By looking at SiNT-FET structure (Figure 6.3), we see that the parasitics related to inner gate reduce leading to increase in $f_T$ as can be seen from Figure 6.16. $f_T$ is more sensitive to $T_{OX,\text{IN}}$ compared to $T_{OX,\text{OUT}}$ as shown in Figure 6.16.

![Figure 6.16 $f_T$ and its sensitivity as a function of $T_{OX}$](image)

Figure 6.16 $f_T$ and its sensitivity as a function of $T_{OX}$

Figure 6.17 shows $f_T$ versus $T_{SI}$ for both constant ID and constant OD cases. In the case of constant OD case, to increase $T_{SI}$ we have to decrease ID which results in reduction in inner gate area and one can expect the $I_{ON}$ to go down. But this area reduction decreases the parasitics associated with the inner gate thereby increases $f_T$. In case of constant ID, we increase the OD to increase $T_{SI}$ which increases outer gate area. Even though this increases $g_m$ and $C_{gg}$, $g_m$ dominates leading to an increase in $f_T$. $f_T$ and its sensitivity as a
function of Ø are shown in Figure 6.18. A small reduction in the effective oxide thickness and an increase in channel width with Ø increase $f_T$. Larger Ø shows more sensitivity.

Figure 6.17 $f_T$ and its sensitivity as a function of $T_{Si}$
6.4.2 Sensitivity Analysis of Junctionless Based SINT-FET

6.4.2.1 Impact on $I_{\text{ON}}$, $I_{\text{OFF}}$ and $f_T$

The impact of the JLSiNT-FET structural parameters on performance parameters $I_{\text{ON}}$ and $I_{\text{OFF}}$ are given in this section. $I_{\text{ON}}$ is plotted against $L_G$, $T_{\text{OX,IN}}$, $T_{\text{OX,OUT}}$, $T_{\text{SL,IN}}$, $T_{\text{SL,OUT}}$ and $\phi$, are given in Figures 6.19-6.22. Their sensitivities are calculated at various points by perturbing the respective inputs by $\pm 10\%$ in the range given in Table 6.1. Sensitivity as a function of structural parameters, $L_G$, $T_{\text{OX,IN}}$, $T_{\text{OX,OUT}}$, $T_{\text{SL,IN}}$, $T_{\text{SL,OUT}}$ and $\phi$ of JLSiNT-FET device are also given in the following graphs (Figures 6.19-6.26). $f_T$ as a function of structural parameters, $L_G$, $T_{\text{OX,IN}}$, $T_{\text{OX,OUT}}$, $T_{\text{SL,IN}}$, $T_{\text{SL,OUT}}$ and $\phi$ of JLSiNT-FET device are given in Figures 6.19-6.26. These results can be interpreted in the same way as has been discussed in section

Figure 6.18 $f_T$ and its sensitivity as a function of $\phi$
6.4.1. E.g. $I_{ON}$ increases when $L_G$ decreases as expected. $I_{ON}$ decreases rapidly when $T_{OX\_OUT}$ increases compared to $T_{OX\_IN}$ as explained in 6.4.1.

Figure 6.19 $I_{ON}$ and its sensitivity as a function of $L_G$
Figure 6.20 $I_{\text{ON}}$ and its sensitivity as a function of $T_{\text{OX}}$

Figure 6.21 $I_{\text{ON}}$ and its sensitivity as a function of $T_{\text{SI}}$
Figure 6.22 $I_{ON}$ and its sensitivity as a function of $\Omega$

Figure 6.23 $I_{OFF}$ and its sensitivity as a function of $L_{G}$
Figure 6.24 $I_{OFF}$ and its sensitivity as a function of $T_{OX}$

Figure 6.25 $I_{OFF}$ and its sensitivity as a function of $T_{SI}$
Figure 6.26 $I_{OFF}$ and its sensitivity as a function of $\varnothing$

Figure 6.27 $f_T$ and its sensitivity as a function of $L_G$
Figure 6.28 $f_T$ and its sensitivity as a function of $T_{OX}$

Figure 6.29 $f_T$ and its sensitivity as a function of $T_{SI}$
6.5 DOE BASED RANKING OF STRUCTURAL FACTORS IN SINT-FETs

The SiNT-FET’s parameters are ranked using a two level full factorial DOE with ±10% deviation from the nominal values (Table 6.1). The response variables, $I_{ON}$, $I_{OFF}$, $V_{TH}$, SS and $f_T$, are written as a function of input variables, $L_G$, $T_{OX,IN}$, $T_{OX,OUT}$, $\varnothing$, and $T_{SI}$ as a first order polynomial expression. For example, $I_{ON}$ can be written as,

$$I_{ON}(L_G, T_{OX,IN}, T_{OX,OUT}, OD, ID, \varnothing)$$

$$= \beta_0 + \beta_{L_G} \cdot L_G + \beta_{T_{OX,IN}} \cdot T_{OX,IN} + \beta_{T_{OX,OUT}} \cdot T_{OX,OUT} + \beta_{OD} \cdot OD$$

$$+ \beta_{ID} \cdot ID + \beta_{\varnothing} \cdot \varnothing$$

(6.3)
The ranking is based on the coefficient values ($\beta$ terms). In the similar way, expressions for other responses can also be written. The individual ranks computed in the above manner.

6.5.1 DOE Based Ranking of Structural Factors in Junction and Junctionless SINT-FET Devices

The individual ranks of structural factors of junction and junctionless based SiNT-FETs are tabulated in Table 6.2. The parameter, OD is the most sensitive parameter except for $V_{TH}$, and ID is the least sensitive parameter except for $V_{TH}$. $T_{OX,OUT}$ is more sensitive compared to $T_{OX,IN}$ in the case of $I_{ON}$ whereas $T_{OX,IN}$ is more sensitive compared to $T_{OX,OUT}$ in the case of $f_T$. By adding all the output coefficient values and arranging them in the decreasing order, the overall ranking for the parameters is evaluated and is given in Table 6.3. It can be observed from Table 6.3 that the OD and $\emptyset$ occupy the top most ranks, whereas $L_G$ and ID occupy the last two ranks. The parameter placed against the 1st rank affects the device performance most significantly, and therefore needs tight process control.

Table 6.2 Individual ranking for the structural parameters of SiNT-FET

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<th>Factor</th>
<th>Rank</th>
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<td></td>
<td>$I_{ON}$</td>
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<tr>
<td></td>
<td>SiNT FET</td>
</tr>
<tr>
<td>OD</td>
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</tr>
<tr>
<td>ID</td>
<td>6</td>
</tr>
<tr>
<td>$T_{OX,OUT}$</td>
<td>3</td>
</tr>
<tr>
<td>$T_{OX,IN}$</td>
<td>4</td>
</tr>
<tr>
<td>$\emptyset$</td>
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</tr>
<tr>
<td>$L_G$</td>
<td>5</td>
</tr>
</tbody>
</table>
Table 6.3 Overall ranking for the structural parameters of SiNT-FET

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<th>Factors</th>
<th>Overall Rank</th>
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</tr>
<tr>
<td>OD</td>
<td>1</td>
</tr>
<tr>
<td>Ø</td>
<td>2</td>
</tr>
<tr>
<td>TOX,IN</td>
<td>3</td>
</tr>
<tr>
<td>TOX,OUT</td>
<td>4</td>
</tr>
<tr>
<td>LG</td>
<td>5</td>
</tr>
<tr>
<td>ID</td>
<td>6</td>
</tr>
</tbody>
</table>

6.6 SUMMARY

We have investigated the effect of six structural process parameters, gate length, inner gate oxide thickness, outer gate oxide thickness, tube wall thickness (constant ID and Constant OD), and tube ovality, on the performance of SiNT-FET and JLSiNT-FET devices using 3D TCAD simulations. The response parameters of interest are ON current, OFF current, Sub-threshold swing, Threshold voltage and unity gain frequency. The above study is done at three levels (i) Varying the six process parameters over a range and studying their impact on each of the response parameter (ii) Extracting the sensitivity of each process parameter over a range by performing ±10% variations at various points of the range (iii) Ranking of six process parameters with respect to each response using a two level Full factorial design of experiment method. The overall ranking suggests that OD is the most sensitive parameter whereas ID is the least sensitive parameter for SiNT-FET and JLSiNT-FET devices. Next to OD, the ovality is a significant parameter. Usually LG is expected to be sensitive parameter but in SiNT-FET and JLSiNT-FET devices LG is not sensitive, ranked 5 among 6.