ABSTRACT

The discrete wavelet transform (DWT) has established itself as an efficient method for processing a signal. Due to many useful characteristics like adaptive time-frequency window, efficient computational complexity, and low aliasing distortion, DWT is widely utilized in the applications such as real-time signal and image processing. DWT generally demands a lot of computation, and many of its applications are productive when operating in real-time. Hence, the DWT architectures are implemented in VLSI such that the requirement of the different DWT applications operating in real time can be met.

The JPEG-2000 standard has adopted the DWT for transform because of its advantage of multi-resolution analysis of the signal with time-frequency localization. The two methods developed to produce the wavelet transform are the convolution scheme and lifting scheme. The traditional convolution method uses FIR filter bank structure to implement the DWT. The computational complexity of such implementation is high, as a result, the convolution method is not desirable for low-power high-speed application. Whereas, the lifting scheme reduces the hardware requirement and storage to build the DWT systematically. It is a simple and efficient algorithm which do not require any complex mathematical operations like in the conventional method to implement the wavelet transform.

Many algorithms and architectures have been proposed in the past to methodically implement the 2-D DWT using the lifting scheme. The structures in the literature are flipping based, folded type or recursive structures. Most of the existing designs are focused on the computational complexity, arithmetic resources, memory usage or throughput. However, there is a need to explore an efficient 2-D DWT with minimal hardware and memory usage, and a competent throughput. The main objective of this research is the development of efficient 2-D DWT processors with a throughput rate of two and four. The predominant feature of these structures is its minimal delay of one multiplier ($1/T_m$) in its critical path to attain high-speed computation. The flipping scheme is adopted to implement the 1-D and
2-D DWT architectures to reduce the hardware and memory requirement with a minimum area on the silicon surface. Three different 2-D DWT architectures based on the modified lifting algorithm are developed with a variable throughput for image compression.

The hardware complexity of the DWT architecture is dominated by the arithmetic and memory unit. The main focus of this work is developing the arithmetic part which comprises of the adders and multipliers. A novel design of the processing element for the 2-D DWT is developed using parallel prefix adder and shift-add multiplier. A systematic design approach of the 8-bit, 16-bit, and 32-bit parallel prefix adders based on Ling equation and modified shift-add multipliers are presented to enhance the performance of the DWT processor. The multiplier employs the parallel prefix adder for the accumulation of the partial product to improve the speed of multiplication operation. The design of the multiplier is focused on the reduction of power by reducing the switching activities while still maintaining the other parameters like area and delay. The performance of the multiplier is examined by calculating the energy per multiplication. The results reveal that the multiplier designed using the parallel prefix adder gives a better performance when compared with the other multipliers.

An efficient design of 1-D and 2-D DWT architectures for Cohen-Daubechies-Feauveau 9/7 and 5/3 filters based on the modified lifting scheme with the bit size of 16 operating at 100 MHz is proposed. The DWT architecture is power efficient with reduced transistor count in the processing element. The structures are analyzed in terms of the hardware complexity, memory, timing complexity, and throughput. This thesis presents a high-performance cost-effective design of a custom application specific integrated circuit DWT processor core for signal and image processing application. The design is synthesized using Cadence RTL Compiler and implemented with Cadence Encounter tool using GPDK 180-nm CMOS technology. Three design parameters namely area, power, and delay are observed to analyze the efficiency of the design. The implemented results show that the architecture achieves high speed with reduced hardware and memory suitable for real-time multimedia applications. The proposed architecture can be used for image/video compression suited for digital cameras and mobile phones.