CHAPTER-4

DESIGN AND IMPLEMENTATION OF ISOGI-PLL BASED
CONTROL ALGORITHM FOR DSTATCOM
4.1 DESIGN OF DISTRIBUTION STATIC COMPENSATOR (DSTATCOM)

DSTATCOM is a shunt connected voltage source converter with an interfacing inductor feeding with a storage capacitor at DC bus connected at point of common coupling, in addition to control algorithm. The converter is operated with a control algorithm and a PWM controller to generate suitable gating pulses for regulating the DC bus voltage. DSTATCOM should effectively compensate power quality problems such as harmonics, poor power factor and load balancing in the case of three-phase distribution system. The performance of DSTATCOM mainly depends on the extraction of reference currents or compensator currents. A suitable control algorithm should be employed for the extraction of reference signals to inject currents into the supply system at PCC to compensate the load disturbances. The DSTATCOM compensates harmonic currents injected by the load by injecting the same magnitude of harmonic currents in phase opposition (180° phase shift). In general, control algorithms employed for DSTATCOM comprises of two sub units viz., one for harmonic extraction and the other is to estimate the reference signals. Therefore, there is a lot of research carried out by many researchers on various harmonic extraction methods and reference signal generation methods. But, all these methods are designed for a normal source voltage with low source impedance. Normal / Stiff voltage source can be defined as the voltage source which is not affected by any currents injected by DSTATCOM and always the voltage is tightly regulated at the
PCC. This is however not a valid approach because, the signal estimation or extraction changes with high impedance AC power supplies. High impedance may lead to severe power quality problems such as, harmonics, sags with or without a phase jump, transient impulses, flickering and transients in the supply voltages. For satisfactory operation of DSTATCOM, the active power drawn by the loads from the source end should be equal to the estimated peak value of the reference current. Then, the differences in active powers of supply and load side are compensated by the DC bus capacitor. If the DC bus voltage is regulated to the reference DC bus voltage then, the power drawn by the load is equal to the power supplied by the source. A single-line diagram of DSTATCOM is shown in Fig. 4. 1.

![Fig. 4. 1 Single-Line Diagram of DSTATCOM](image)
There are four steps involved in order to design and develop a suitable DSTATCOM for improving power quality at the distribution mains.

➢ Selection of DSTATCOM rating
➢ Selection of Filtering / Interfacing Inductor
➢ Selection of reference DC-Link Voltage at DC bus and capacitor.
➢ Selection of control algorithm based on objectives.

4.1.1 Selection of DSTATCOM rating

In general, the voltage and current ratings of DSTATCOM depends mainly on:

➢ Maximum current to be delivered by DSTATCOM

The maximum current is calculated by closing the two switches in the same leg (short-circuited) which equals the maximum line current or per-phase current in a three-phase circuit.

➢ Maximum voltage stress sustaining limit

It is explained as the voltage appearing across the switch when one of the switches is open in a leg which is equal to the DC-link voltage. Hence, the maximum rating of DSTATCOM is chosen more than the DC-link voltage for safer and reliable operation.
Switching frequency

High switching frequency which is approximately ten times more than the harmonic frequency is to be utilized for reactive power and harmonic compensation.

4.1.2 Selection of Filtering / Interfacing Inductor

Inductor used at the output of DSTATCOM should filter out ripple content produced in the compensated current and voltages. The design depends on the ability to compensate both harmonics and reactive power. The peak ripple current is considered at no-load for designing the inductor and the source voltage should be equal to the inverter voltage. It is mathematically expressed as:

\[ L_f = \frac{V_s}{2\sqrt{6}f\Delta I} \]  

(4.1)

Where, \( L_f \) = Interfacing Inductor (Henry)

\( f \) = Supply Frequency (Hz)

\( \Delta I_{(P-P)} \) = Change in ripple should be 15% of the peak injected current (A)

There are also some other alternate methods are available to calculate the value of interfacing inductor in the literature.

4.1.3 Selection of reference DC-Link voltage at DC bus and Capacitor

The compensation ability of the DSTATCOM mainly depends on the DC link voltage \( (V_{dcref}) \) and DC storage capacitor \( (C_{dc}) \). In order to force the
controller currents, the value of the $V_{\text{dcref}}$ should be 1.6 times the peak value of the system voltage.

The DC-link voltage is calculated by considering the maximum modulation index ($m = 1$) and it can be expressed as:

$$m = \frac{V_m}{V_{dc}} = \frac{2V_m}{V_{dc}} = \frac{2\sqrt{2}V_s}{V_{dc}}$$

(4.2)

If $m = 1$, $V_{dc} = 2\sqrt{2}V_s$

(4.3)

If the compensation is achieved effectively then, the source current and source voltage should be in-phase and injected current and source voltage are orthogonal to each other.

The minimum voltage required for DC-link voltage can be expressed as:

$$V_{dc} = \frac{2\sqrt{2}V_s}{1.15}$$

(4.4)

Similarly, the DC-link capacitor has two primary functions:

- To maintain a ripple free and constant voltage during steady state operation.
- To supply real power during transient operation when there is a difference between load and source powers.

Once the value of $V_{\text{dcref}}$ is selected, the value of $C_{dc}$ can be estimated from the transient period of the system. Assume that the DSTATCOM is
connected to x-KVA system and allowing a maximum of 12.5% variation in $V_{dc}$ during transients, the differential energy ($\Delta E_c$) across $C_{dc}$ is given as:

$$\Delta E_c = \frac{C_{dc}[(1.6V_m)^2 - (1.4V_m)^2]}{2} \quad (4.5)$$

If the load is changed from $x$ - KVA to $1.5x$ - KVA then the change in system energy is given as:

$$\Delta E_s = (1.5x - x)1000 * pT \quad (4.6)$$

Where, $p$ is the transient period and $T$ is the time period. Therefore, $C_{dc}$ can be determined as:

$$C_{dc} = \frac{2(1.5x - x)1000 * pT}{[(1.6V_m)^2 - (1.4V_m)^2]} \quad (4.7)$$

Similarly, $C_{dc}$ can be calculated for decrease in load and the maximum value obtained can be chosen as the DC link capacitor $C_{dc}$. This value of capacitor releases the energy required by the load instantaneously.

### 4.2 CONTROL ALGORITHM FOR DSTATCOM

Control algorithm has a main role for improving the overall performance of DSTATCOM. There are three main building blocks for the design of control algorithm. Firstly, voltages and currents are measured and supplied to a phase-locked loop for estimating magnitude and phase of the voltage or current signal based on the requirements. Then, a proper control strategy is applied for estimating reference signals and supplied to a PWM generator for generating suitable gating pulses for DSTATCOM.
In general, conventional unit template methodology is adopted in the case of balanced and sinusoidal conditions. But, this method is not so effective in generating reference signals when the voltage signal is prone to distortions and unbalances. Therefore, an alternate method of estimating phase and magnitude from a source voltage signal is done by the use of Phase-Locked Loop (PLL). An ISOGI-PLL based control algorithm was employed for fast and accurate estimation of phase and magnitude of voltage and current signals under both steady and dynamic conditions, balanced and unbalanced conditions, normal grid and distorted grid conditions. A QSG based SOGI is used for magnitude estimation and the PWM controller generates accurate gating pulses to DSTATCOM for proper and effective harmonic and reactive power compensation. In addition to all these features, ISOGI-PLL is an adaptive filter which filters the input signal and therefore, the estimation signal has low ripple content and thus improved accuracy is achieved.

In this chapter, ISOGI-PLL based control algorithm is designed and compared with SRF theory for compensating current harmonics, load balancing, improving power factor by compensating reactive power, regulating DC bus voltage. The performance of the DSTATCOM is validated using MATLAB/Simulink in both stiff and distorted grid conditions such as voltage sags, harmonics and phase and frequency changes and DC offset for a three-phase distribution system.
4.3 SRF THEORY BASED CONTROL ALGORITHM FOR DSTATCOM

There are many control algorithms that are proposed in the literature and Synchronous Reference Frame (SRF) theory based control algorithm is the popular method and is widely used. The control algorithm used in SRF theory is shown in Fig. 4.2. The DSTATCOM is connected in parallel with the load and source at a point called as point of common coupling (PCC) to cancel out the harmonics or reactive component by injecting currents in phase opposition with the load currents. SRF theory uses transformation technique to transform the variables from stationary frame to synchronously rotating reference frame. Initially, a three-phase SRF-PLL is used to generate reference phase angle from input grid voltage signal. This phase angle is considered as reference phase angle and is used for transformations. The transformation can be done in either ways using Clarke’s transformation or Park’s transformation.

Clarke’s Transformation:

\[ I_a = \frac{2}{3} (I_a) - \frac{1}{3} (I_b - I_c) \]

\[ I_\beta = \frac{2}{\sqrt{3}} (I_b - I_c) \]  \hspace{1cm} (4.8)

Inverse Clarke’s Transformation:

\[ I_a = I_a \]
\[ I_b = \frac{-I_a + \sqrt{3} * I_\beta}{2} \]

\[ I_c = \frac{-I_a - \sqrt{3} * I_\beta}{2} \]  

(4.9)

Park's Transformation:

\[ I_d = I_a * \cos(\theta) + I_\beta * \sin(\theta) \]

\[ I_q = I_\beta * \cos(\theta) - I_a * \sin(\theta) \]  

(4.10)

Inverse Park's Transformation:

\[ I_a = I_d * \cos(\theta) - I_q * \sin(\theta) \]

\[ I_\beta = I_q * \cos(\theta) + I_d * \sin(\theta) \]  

(4.11)

Direct Transformation:

\[ I_d = \frac{2}{3}(I_a * \cos(\theta) + I_b * \cos(\theta - \frac{2\pi}{3}) + I_c * \cos(\theta + \frac{2\pi}{3})) \]

\[ I_q = \frac{2}{3}(-I_a * \sin(\theta) - I_b * \sin(\theta - \frac{2\pi}{3}) - I_c * \sin(\theta + \frac{2\pi}{3})) \]

\[ I_0 = \frac{1}{3}(I_a + I_b + I_c) \]  

(4.12)

Inverse Transformation:

\[ I_a = (I_d * \cos(\theta) - I_q * \sin(\theta) + I_0) \]

\[ I_b = (I_d * \cos(\theta - \frac{2\pi}{3}) - I_q * \sin(\theta - \frac{2\pi}{3}) + I_0) \]
\[ I_c = (I_d \cdot \cos(\theta + \frac{2\pi}{3}) - I_q \cdot \sin(\theta - \frac{2\pi}{3}) + I_0) \]  

(4.13)

Fig. 4. 2 Design of Three-Phase DSTATCOM based on SRF Theory

These transformations are used for transforming into rotating synchronous frame from stationary reference frame for isolating the harmonic frequency with the help of low-pass filters. The AC quantities (load currents) are now transformed to DC quantities and the harmonic frequency components are shifted by the nominal frequency (\(\omega\)) in the synchronous rotating reference frame. The vector diagrams of transformations are shown in Fig. 4. 3 A filter with \(\omega\) at line frequency is
used to extract the DC components from the load current to calculate harmonic component present in the signal.

![Diagram](image)

**Fig. 4. 3 Vector Diagrams of Transformations**

If the phase of d-axis current matches with line current of phase a-axis with the help of PLL, then the current \( I_d \) represents active component of current and \( I_q \) represents the reactive component of current. The active component of load current (\( I_d \)) is calculated from transformation and then added with the loss component (\( I_{\text{Loss}} \)) to increase the load reference current. \( I_{\text{Loss}} \) is calculated from the DC voltage loop i.e, DC bus voltage is
sensed across the capacitor and then compared with the reference DC bus voltage and then supplied to a PI controller to generate $I_{\text{Loss}}$ component.

\[ I_d^* = I_{\text{Loss}} + I_d \]  

(4.14)

$I_d^*$ is the reference DC component and is transformed back to AC component or reference source current ($I_s^*$) by using Inverse transformation ($dq0/abc$). The reference current is then compared with the actual sensed current and supplied to a PWM controller to generate gating pulses to the DSTATCOM.

### 4.4 IMPROVED SOGI BASED CONTROL FOR DSTATCOM

The performance of SOGI-QSG and ISOGI-PLL are already discussed earlier. The SOGI-QSG produces two orthogonal components with a phase difference of $90^0$ to estimate the magnitude and the orthogonal components are transformed to d-q components to process for estimation of phase and frequency of the given input signal. The ISOGI-PLL based control algorithm is implemented to a DSTATCOM for a three-phase three-wire distribution system as shown in Fig. 4.4.

The DSTATCOM comprises of a DC link capacitor at its DC bus feeding the inverter and followed by an inductive filter to ensure smooth flow of injected current. The main intention of DSTATCOM is to inject currents at the point of common coupling (PCC) in phase opposition to that of the harmonic currents produced by non-linear loads in order to cancel out the harmonics which results a pure sinusoidal current at the source end with
low overall THD %. To achieve the objectives mentioned earlier, ISOGI based control algorithm is employed to generate the reference currents for DSTATCOM.

![Diagram of Power Grid/Supply (Vsabc) and Linear/Non Linear Loads](image)

**Fig. 4.4 ISOGI based Control Algorithm for DSTATCOM.**

Usually, there are three building blocks for the design of proposed control algorithm.

- Phase angle estimation from grid voltage signal using SOGI-PLL.
- SOGI-QSG based reference peak current estimation.
- DC Voltage Control Loop
4.4.1 Phase angle estimation from grid voltage signal using ISOGI-PLL

Initially, a control system is employed to measure the three-phase source voltages, source currents and load currents and then ISOGI based PLL and QSG uses these measured components to design the overall control algorithm. Each of the three-phase voltage signals \( V_a, V_b, V_c \) are supplied for three single-phase ISOGI-PLLs to estimate the phase angle \( \theta_a, \theta_b, \theta_c \) respectively as shown in Fig. 4. 4.

4.4.2 SOGI-QSG Based Reference Peak Current Estimation

The phase angles estimated from the ISOGI-PLL are then used to generate reference source currents as shown in eqn. 4.15.

\[
\begin{align*}
I_{sa}^* &= I_p^* \sin(\theta_a) \\
I_{sb}^* &= I_p^* \sin(\theta_b) \\
I_{sc}^* &= I_p^* \sin(\theta_c)
\end{align*}
\]

(4.15)

Where, \( I_p \) is the peak component of current estimated by SOGI-QSG. The load currents \( I_{La}, I_{Lb}, I_{Lc} \) are supplied to three single-phase SOGI-QSGs for the estimation of magnitude of each phase respectively. SOGI-QSG generates two orthogonal signals \( I_{L\alpha}, I_{L\beta} \) for all the three phases respectively and magnitude is calculated as shown in eqn. 4.16.

\[
\begin{align*}
I_{Lpa} &= \sqrt{I_{L\alpha}^2 + I_{L\beta}^2} \\
I_{Lpb} &= \sqrt{I_{L\alpha}^2 + I_{L\beta}^2} \\
I_{Lpc} &= \sqrt{I_{L\alpha}^2 + I_{L\beta}^2}
\end{align*}
\]

(4.16)
The estimated currents are then summed and average is calculated and supplied to a low-pass filter to eliminate ripples to estimate the peak amplitude of current \( I_{\text{Avg}} \) and summed with \( I_{\text{cd}} \) (generated by voltage control loop) to estimate the reference peak amplitude of current \( I_P \) as shown in eqn. 4.17.

\[
I_{\text{Avg}} = \frac{I_{Lpa} + I_{Lpb} + I_{Lpc}}{3}
\]

\[
I_P = I_{\text{Avg}} + I_{\text{cd}}
\] (4.17)

### 4.4.3 DC Voltage Control Loop

DC voltage control loop generates the required component of current for compensation. The voltage across the DC capacitor \( V_{dc} \) is sensed and compared with the reference DC bus voltage \( V_{dc}^* \) and this error at the \( n^{\text{th}} \) sampling instant is expressed as:

\[
V_{dc}(n) = V_{dc}^*(n) - V_{dc}(n)
\] (4.18)

This voltage error is fed to PI controller to maintain or regulate the DC bus voltage of the DSTATCOM. At \( n^{\text{th}} \) sampling instant, the output of the PI controller is as:

\[
I_{\text{cd}}(n) = I_{\text{cd}}(n-1) + K_{\text{pt}} \left( V_{dcer}(n) - V_{dcer}(n-1) \right) + K_{\text{it}} V_{dcer}(n)
\] (4.19)

Where, \( K_{\text{pt}} \) and \( K_{\text{it}} \) are the proportional and integral gain constants of the PI controller. \( V_{dcer}(n) \) and \( V_{dcer}(n-1) \) are the voltage errors of the DC bus in \( n^{\text{th}} \) and \( n-1^{\text{th}} \) instant and \( I_{\text{cd}}(n) \) and \( I_{\text{cd}}(n-1) \) are the amplitude of active power component of the fundamental reference current at \( n^{\text{th}} \) and
(n-1)\textsuperscript{th} instant. The reference current estimated from the control algorithm is then compared with the sensed source current and supplied to a PWM generator to generate gating pulses for DSTATCOM for compensation.

The proposed control algorithm uses the structure of SOGI for the estimation of phase and magnitude respectively. The SOGI-QSG eliminates most of the harmonic components from the load current signal and hence eliminating the usage of additional filters in the control algorithm and the ISOGI-PLL generates exact phase even under distorted grid voltage conditions. These two additional features are making the proposed control algorithm simple, effective and suitable for power quality improvement.

4.5 RESULTS AND DISCUSSIONS

The structure of the SRF theory and proposed ISOGI based control strategies with the line diagram of three-phase distribution system are shown in Fig. 4. 2 and Fig. 4. 3 respectively. MATLAB / Simulink (R2013a) is pursued for verifying the efficacy of the proposed control algorithm. In order to test and validate the reliability and accuracy of the proposed controller, stiff grid conditions and weak / adverse grid conditions are also taken into consideration.

4.6 SYSTEM DESCRIPTION

The structure of the proposed controller and SRF controller are already discussed in the previous section. To test the control algorithms,
a three-phase three-wire distribution system is considered for MATLAB / Simulation. Initially, a balanced three-phase voltage is applied to a non-linear load (three-phase diode bridge rectifier feeding R-L load). The source side impedance ($R_s$, $L_s$), load side impedance ($L_L$), DC-link voltage ($V_{dc}$), filter inductance ($L_f$), the source voltage ($V_{sabc}$), load voltage ($V_{Labc}$), source current ($I_{sabc}$), load current ($I_{Labc}$) and the injected current by DSTATCOM ($I_{cabc}$) are the system parameters discussed in table 4.1. The DSTATCOM is connected in parallel with the grid and load at the PCC for compensation of harmonic currents. In this thesis, the performance of DSTATCOM is analyzed for both stiff grid and weak grid conditions and the test cases that are considered using MATLAB simulation are:

- A balanced Non-Linear Load is applied.
- An unbalanced linear load is applied ($t = 0.9s$ to $1s$).
- A sudden increase in non-linear load is applied ($t = 1.2s$ to $1.3s$).
- A voltage swell is applied in the grid voltage signal ($t = 1.9s$ to $2s$).
- An unbalance is created in the grid voltage signal ($t = 2.6s$ to $2.7s$).
- Harmonics are injected in the grid voltage signal ($t = 2.9s$ to $3s$).

SRF and proposed ISOGI based control algorithms are simulated for all the conditions mentioned above. The results of source voltage, source current, load current, injected/compensated current, DC link voltage and scaled source voltage and source current of phase A for power factor observation are shown.
4.6.1 A Balanced Non-Linear Load is Applied

In this test case, the source voltage is kept balanced and sinusoidal with a non-linear load consisting of a diode bridge rectifier feeding R-L load ($R_L = 24\Omega$, $L_L = 6mH$) and the DSTATCOM compensates the harmonics injected by the load as shown in Fig. 4.5. The two control strategies are mostly replicating the same results but the SRF theory has a higher THD (%) in comparison with the proposed method. Because, the SRF control theory suffers from more ripples compared to proposed method during the magnitude and phase estimation and has a source current THD of 3.17 % and the THD in the proposed method was still reduced to 2.46 % with the load current THD of 25.15% as shown in Fig. 4.5. The simulation parameters used for both SRF and ISOGI based controllers are shown in Table 4.1.

4.6.2 An Unbalanced Linear Load is Applied

In this case, a linear unbalanced load is added to the existing non-linear load. The linear load comprises of a resistance and inductance and the values are different in all the three phases creating an unbalance in the load currents ($R_{La} = 12\Omega$, $L_{La} = 3mH$, $R_{Lb} = 36\Omega$, $L_{Lb} = 6mH$, $R_{Lc} = 48\Omega$, $L_{Lc} = 12mH$) as shown in Fig. 4.6. The level of compensation is low in SRF based control (THD = 2.11%) compared ISOGI based control (THD= 1.82%). This is because of the steady state error produced during the magnitude estimation in SRF as discussed earlier in chapter 3.
5 A balanced Non-Linear Load is applied
Fig. 4. 6 An Unbalanced Non-Linear Load is applied
**Fig. 4.** A Sudden Increase in Load is applied
4.6.3 A Sudden Increase in Non-Linear Load is Applied

The load is increased suddenly to test the dynamic performance of both the controllers. The unbalance in the previous case was made zero and a non-linear load is added additionally to the existing non-linear load with $R_L = 48\Omega$ and $L_L = 12\text{mH}$. The performance of the SRF controller was low because of poor dynamic response during the tracking of sudden changes and the regulation of DC link voltage is low compared to the proposed method as shown in Fig. 4. 7. The THD % of SRF and ISOGI controllers are 4.03 % and 2.47 % respectively.

4.6.4 A Voltage Swell is Applied in the Grid Voltage Signal

If a balanced load connected to the distribution system was suddenly disconnected from the system then there is a sudden rise in the voltage more than the nominal voltage called as swell as shown in Fig. 4. 8. To test the performance during voltage swell, a 30 % increase in source voltage signal is considered (1 p.u. to 1.3 p.u.). Due to the sudden rise in voltage the SRF controller is unable to track the change in phase and magnitude of the voltage signal and therefore shows a poor performance in the source current signal compared to the proposed method. The THD is increased to 4.37 % in SRF method and it is still low (3.74 %) in the proposed method. The DC link voltage is tightly regulated in the proposed method and varying in the case of SRF method.
Fig. 4. A Sudden Increase in Source Voltage is applied
4.6.5 An Unbalance is Created in the Grid Voltage Signal

To test the performance of both the methods, the three-phases are loaded differently and also the motors connected to a three-phase system may produce unbalance in the source voltage signal. During these conditions, the load and source current may lead to unbalance if a proper control algorithm is not employed. The SRF and ISOGI methods are maintained a balanced source and load currents even under unbalance in the voltage signal. But, the level of compensation was low in SRF and THD (3.79 %) is more than the proposed method (2.53 %) as shown in Fig. 4. 9.

4.6.6 Harmonics are Injected in the Grid Voltage Signal

To test the performance of both the controllers, 5th and 7th harmonics are injected into the source voltage signal. This is because, if the grid voltage is loaded with DG sources or the distribution transformers may lead to change in the voltage waveform. As a result of such voltage variations, the controller may lead to improper tracking of voltage signal and the proposed method (THD = 2.30%) is proved effective compared to SRF control (THD = 3.20%) even under the distorted grid voltage signal as shown in Fig. 4. 10.

In all the test cases that are mentioned above, The SRF theory was bit modified to test the efficacy of both SRF and ISOGI PLLs in tracking the voltage and current signals under all conditions. Conventional SRF method uses a Unit Vecctor Template (UVT) technique for the generation
of phase signals used for transformation and has a poor performance when the grid voltage signal has distortions or unbalance in it.

Fig. 4. An Unbalance in Source Voltage is applied
Fig. 4. 10 Source Voltage Harmonics are applied
To compare the controller theory more effectively, all the control and power circuit parameters are considered same and three-phase SRF-PLL is employed instead of UVT to generate phase signals in order to compare both the theories more effectively.

The proposed ISOGI based controller was found more effective compared to the SRF theory in effective harmonic and reactive power compensation in all sinusoidal and distorted grid voltage conditions. The DC link voltage is also tightly regulated in the proposed method. The summary of the results are shown in

Table 4. 2.

<table>
<thead>
<tr>
<th>Table 4. 1 Simulation Parameters for DSTATCOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Voltage, Frequency</td>
</tr>
<tr>
<td>Non-Linear Loads</td>
</tr>
<tr>
<td>Linear Load</td>
</tr>
<tr>
<td>RL1 = 24Ω, LL1 = 6mH, RL2 = 48Ω, LL2 = 12mH</td>
</tr>
<tr>
<td>RLa = 12Ω, LLa = 3mH, RLb = 36Ω, LLb = 6mH</td>
</tr>
<tr>
<td>RLC = 48Ω, LLc = 12mH</td>
</tr>
<tr>
<td>Source Impedance</td>
</tr>
<tr>
<td>Load Impedance</td>
</tr>
<tr>
<td>Rs = 0.5, Ls = 0.5mH</td>
</tr>
<tr>
<td>RL = 0.05Ω, LL = 1.5mH</td>
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<tr>
<td>Filter Inductance</td>
</tr>
<tr>
<td>Lt = 3.5mH</td>
</tr>
<tr>
<td>DC link Voltage and Capacitance</td>
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<td>Vdc = 800V, Cdc = 4700µH</td>
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<td>DC Voltage Controller Gains</td>
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<tr>
<td>Kpdc = 0.45, KIdc = 0.4</td>
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<td>PLL Controller Gains</td>
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<tr>
<td>Kp = 67.5, K1 = KR = 100, Wc = 7</td>
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</tbody>
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Table 4. 2 Summary of Results for DSTATCOM

<table>
<thead>
<tr>
<th>Conditions / Test Cases</th>
<th>Source Voltage THD (%)</th>
<th>Source Current THD (%)</th>
<th>Load Current THD (%)</th>
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<tr>
<td></td>
<td></td>
<td>SRF</td>
<td>ISOGI</td>
</tr>
<tr>
<td>Balanced Source Voltage with Balanced Non-Linear Load</td>
<td>2.53</td>
<td>3.17</td>
<td>2.46</td>
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<tr>
<td>Balanced Source Voltage with Un-Balanced Load</td>
<td>2.48</td>
<td>2.11</td>
<td>1.82</td>
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<td>Balanced Source Voltage with Sudden Increase in Load</td>
<td>2.51</td>
<td>4.03</td>
<td>2.47</td>
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<td>Source Voltage swell with Balanced Load</td>
<td>3.03</td>
<td>4.37</td>
<td>3.74</td>
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<td>3.79</td>
<td>2.53</td>
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<tr>
<td>Source Voltage Harmonics with Balanced Load</td>
<td>24.67</td>
<td>3.20</td>
<td>2.30</td>
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</table>

4.7 CHAPTER SUMMARY

In this chapter, a three-phase three-wire distribution system with a three-leg voltage source inverter as DSTATCOM is presented. Various power quality problems and their possible solutions are explained using SRF and ISOGI based control. Both the controllers are explained clearly and a comparison is made during normal and abnormal grid conditions. The performance of the proposed control is found satisfactory than the
SRF based control because of proper estimation of phase and accurate tracking of magnitude under all simulation test cases. Finally, a summary of total harmonic distortions is presented for better comparison.