CHAPTER 1

INTRODUCTION TO EPITAXY AND LITHOGRAPHY

1.1 INTRODUCTION

Semiconductors are the raw materials for microelectronics industry, which conduct electricity more than insulators but less than the metals. The components made from semiconductors have very favorable properties such as low energy consumption, compactness and high reliability. Semiconductors are indispensable for space exploration and military application where the requirements of small size, low weight, low energy consumption and high precision are especially stringent.

Another area where semiconductors are important is the “optoelectronics”, which is an area of modern technology where light and electronics join hands to produce many semiconductor devices, which are making our everyday life easier. Optoelectronic devices consist of two or more of the suitable semiconductor layers on the substrate. As the human civilization moved from the electronic age to the information age, the demand from the common citizens for services like email, internet, video conferencing, entertainment, data transfer, mobile telephones, laptop computers require a large amount of bandwidth and high speed operation of the devices and systems. Conventional electronics is unable to cope with this demand and the present day systems are relying more on optoelectronics and semiconductor devices rather than merely on electronics.
Semiconductors are physically available as Group-IV elements of periodic table and their associated compounds. Silicon (Si) and Germanium (Ge) are the most common elemental semiconductors. In fact, largely because of its unique oxide technology, and its relatively good hole mobility, Si has become the dominant material of electronics. However, Si is an indirect band gap semiconductor which has poor light emission efficiency. Si photodetectors are available and they offer some advantages but the devices do not match the present fiber-optic communication wavelength. Although elemental semiconductors have been discovered earlier and constituted bulk of the materials used for electronic device technology, the small band gap of the elemental semiconductors impose certain restrictions in their technological exploitations, i.e. to construct efficient microwave and optoelectronic devices.

Compound semiconductors came up during the search for materials with direct band gap. Historically, for optoelectronic device applications, group III-V and II-VI semiconductors such as Gallium Arsenide (GaAs), Indium Phosphide (InP) and Zinc Sulphide (ZnS), Cadmium Telluride (CdTe) are the most widely used compound semiconductors. In case of optical communications and optoelectronics, the Group II-VI and III-V semiconductors offer the device engineer a large choice of material band gaps. This flexibility in the availability of the chosen band gap is further enhanced in case of the binary and quaternary alloys. However by alloying it is not only possible to vary the band gap continuously and monotonically but the band structure, electronic and optical properties can also be varied. These have turned out to be important advantage in realizing devices with artificially engineered band gap structures and also enable the formation of heterojunctions. The fabrication of optoelectronic devices such as lasers and
light emitting diodes with operating range selected by the material band gap. Today the energy efficient solid state lighting using III-V nitride compounds are replacing incandescent lighting in many applications. Both III-V and II-V compound semiconductors have a wide application in space based systems. Figure 1.1 shows the energy gap as a function of lattice constant at room temperature.

![Figure 1.1 Schematic sketch of energy gap as a function of lattice constant at room temperature](image)

1.2 EPITAXY AND ITS ADVANTAGES

The word epitaxy is a Greek word combining of two parts “epi + taxis”. The meaning of ‘epi’ is upon or attach and ‘taxis’ is arrangement or order. Optoelectronic devices consist of layers grown on the substrate. These layers are called epitaxial layers and follow the same crystallographic orientation of the substrate (Stringfellow 1982). There are two types of
epitaxy, if the substrate and the layer are of the same material, then it is called homoepitaxy (e.g. InAs on InAs) and if both are different then it is called heteroepitaxy (e.g. InAs on GaAs). The concept of epitaxy was first presented by Royer in 1928.

Growth of high-purity single crystalline material is possible using epitaxial growth techniques. This allows very precise control over the electrical and optical properties of the material. Ternary and quaternary alloy semiconductors, which cannot be grown in bulk crystal form, can be grown as epitaxial layers on binary substrates with alloy composition properly chosen so as to get a lattice match. Multilayered structures can also be grown by epitaxial techniques, resulting in a material with artificially engineered properties. Thus the development of epitaxial growth techniques during the last two decades has ushered in a new era of electronics with many advanced devices having fascinating properties.

The epitaxial layers have better structural and electrical properties than the bulk ones. This is mainly due to the fact that, in epitaxy, regardless of the method used, the growth is carried out at a temperature several hundred degrees lower than the melting point of the compound or alloy. This decrease in growth temperature accounts for the observed decrease in the concentration of both chemical and crystalline defects as compared with the material grown from a nearly stoichiometric melt. At lower temperature, the melt is subjected to less chemical contamination by dissolution or diffusion from the surrounding container. Also concentration of the lattice vacancy is expected to decrease at lower temperatures. In addition, there are some other advantages of epitaxial growth, with reference to the above facts, such as: (1) the ability to control material thickness and carrier concentration, (2) the possibility of growing p-n junctions and other multilayer structures
and (3) superior electrical properties particularly minority carriers due to the lower defect densities in epitaxial materials.

Most of the devices are fabricated on substrates of either the same material or a material with a compatible lattice constant and crystal symmetry. For many applications, epitaxial layers are required either for the active regions or to isolate the device from undesirable properties of the device surface or the substrate. The most fascinating advances have been in the growth of multilayered structures, super-lattices and multiple quantum well (MQW) structures.

1.3 CRYSTAL STRUCTURE

Semiconductors, in common use, are almost single crystal materials. A crystal is a periodic arrangement of atoms in 3D. A space lattice and a basis comprise a crystal structure. The periodic arrangement of points on which atoms or groups of atoms can be placed is described as the space lattice whereas the basis may consist of a single atom or an arrangement of atoms placed at each lattice. There are 14 space lattices called bravais lattices (Kittel 2004).

1.3.1 Diamond

Common semiconductors such as Ge, Si and their alloys all crystallize in diamond structure. The diamond structure belongs to face centered cubic(FCC) lattice with the basis of two atoms at each lattice point, one at (0,0,0) and the other at (a/4,a/4,a/4) where a is the lattice constant. The structure can be thought of as two FCC lattices where one lattice is displaced from the other by one quarter of the unit cell diagonal. The space group is
Fd3m(Oh). The lattice constant “a” is equal to the length of the cubic cell. The atoms in the diamond lattice are tetrahedrally and each atom is covalently bonded to its four nearest neighbours.

1.3.2 Zinc Blende

In semiconductors, a number of compounds are in zinc blende structure (e.g. GaAs, InP). The zinc blende lattice belongs to the space group of F43m(Td). The zinc blende unit lattice is similar to the diamond lattice except for the two different FCC sub-lattices that contains two different atoms. Figure 1.2 shows the crystal structure of zinc blende.

![Figure 1.2 Crystal structure of zinc blende](image-url)
Each atom has four nearest neighbours from the other type of atoms. This dual atomic arrangement will lower the symmetry and give it a generic polar nature due to partly ionic bonding.

1.3.3 Miller Index

Miller indices are the accepted means for identifying planes and directions within a crystalline lattice. They consist of triplets corresponding to the three spatial directions. The miller index for a plane is obtained as follows. The intercepts of the plane with the three orthogonal axes $a$, $b$ and $c$ are determined in terms of the lattice constant $a$. This will yield three integers which may be positive or negative. The three smallest integers having the same ratios as the reciprocals of these intercepts are the Miller indices $h$, $k$ and $l$ and the plane is denoted $(hkl)$.

Figure 1.3 shows the crossing-points of the (111) plane with the $<100>$ axis. For planes where there is no intercept for one or two axes i.e. the intercept is at infinitely the reciprocal will be zero. When the plane has an intercept along the negative portion of a coordinate axis it is customary to denote the corresponding index with an over bar rather than a minus sign. The type of brackets employed to enclose the indices has the following designation: [.] indicates a direction; (.) indicates a plane. For cubic crystals, a plane and the direction normal to the plane have precisely the same indices.
1.4 EPITAXIAL LATERAL OVERGROWTH

Growth which initially starts selectively on the openings of the mask is normal to the substrate i.e. vertical growth on single-crystal seed area is called selective area growth (SAG) and proceeds preferentially in the direction parallel to the substrate. The lateral growth over non-crystalline portion of the substrate is called epitaxial lateral overgrowth (ELOG). Figure 1.4 shows the basic principle of ELOG. The principle of this technique is used to block the dislocations which is propagating from the layer grown on III–V seed mainly in heteroepitaxy having large mismatch and high thermal expansion co-efficient values between the substrate and the grown layer.
1.5 VARIOUS EPITAXIAL GROWTH TECHNIQUES

There are several techniques available for the high quality epitaxial growth of semiconductor compounds and their heterostructures. They are Liquid Phase Epitaxy (LPE), Vapour Phase Epitaxy (VPE), Metal Organic Vapour Phase Epitaxy (MOVPE), Molecular Beam Epitaxy (MBE), Atomic Layer Epitaxy (ALE) and Chemical Beam Epitaxy (CBE). The first two growth methods are so-called near thermodynamic equilibrium techniques and the remaining techniques are far-off equilibrium. A solid heterogeneous reaction can be limited basically by one of the three steps: 1) input mass transport, 2) mass transport due to diffusion and 3) surface kinetics. In LPE and VPE it is usually step (1) which limits the growth, in MOVPE step (2) and in MBE step (3). Step (1) is typical for a process operating close to equilibrium. This feature of the VPE process arises from the reversible process occurring at the interface due to the volatility of the chlorides of group III species at the operating temperatures and where the shift from the equilibrium mainly depends on the decomposition of the hydrides transporting the V- species.
The benefits of a near-equilibrium growth process are:

(i) Growth rates are in principle determined by the mass input reactants and very high growth rates (> 20 µm/hr) can easily be achieved. This is because; being a near equilibrium process, a small change in chemical potential between the gases and the solid affects the growth rate considerably.

(ii) The volatility of group III chlorides renders their absorption on the dielectric mask with respect to the semiconductor surface difficult. This inherent property of VPE makes it an excellent technique for selective growth where certain areas are protected by dielectric masks to hinder the growth in those areas.

(iii) In the kinetically controlled regime (at low operating temperature) the growth rates are different at different crystal planes but will coincide at high temperatures in the thermodynamically controlled regime. At normal conditions, for growth on non-planar substrates there will be a natural driving force to reach stable crystallographic directions. Since (001) substrates are similar to \{hkl\} planes the resulting effect will lead to a planarization.

The main drawback is the difficulty in growing very abrupt interfaces caused by the reversible process and the slow switching between the vent and run. This makes it hard to grow very thin layers with abrupt interfaces, such as quantum wells. Since it is a hot-wall reactor there is a risk for extraneous deposition on the reactor wall.
1.5.1 Liquid Phase Epitaxy

Liquid Phase Epitaxy (LPE) involves the growth of epitaxial layers on crystalline substrate by direct precipitation from the liquid phase. The growth of many semiconductor crystals can be performed from a liquid solution at temperatures well below their melting point. Since a mixture of the semiconductor with a second element may melt at a lower temperature than the semiconductor itself, it is often an advantage to grow the crystal from solution at the temperature of the mixture. Using this technique, single crystals can be grown at low temperatures, enough to eliminate many problems of impurity introduction typical of growth at crystal melting temperature. LPE technique is particularly useful for the growth of III-V compounds in which Ga or In serve as the column III element, since these metals form solutions conveniently at low temperatures.

The LPE technique was first demonstrated by Nelson in 1963 by fabricating Ge tunnel diodes and GaAs lasers. LPE involves the growth of epitaxial films by placing a saturated solution in contact with the substrate. The physical basis of the LPE growth process is that the solubility of a diluted solute in a liquid solvent decreases with decreasing temperature. In practice, the solvent is the metallic constituent of the growing epitaxial film (for example, Ga for GaAs growth or In for InP growth), while the solute is the non-metallic constituent (for example, As in GaAs growth).

The LPE technique is the combination of solution growth and epitaxy, which takes the advantage of both the process. In solution growth, the growth takes place close to the thermodynamic equilibrium and at comparatively low temperatures. The rate determining step in LPE growth over a wide range of temperatures has been supposed to be the diffusion of solute species towards or away from the liquid-solid interface. According to
the diffusion limited growth model, the growth rates depend on the growth
time, concentration of solution and diffusion coefficient (D) of the solute
materials.

Assuming the growth from solution to be isothermal, diffusion in
the solid phase to be negligibly slow, and convective processes to be
insignificant, analysis of the growth process reduces in solving the simplified
one dimensional diffusion equation,

$$\frac{\partial C(x,t)}{\partial t} = D \frac{\partial^2 C(x,t)}{\partial t^2}$$  \hspace{1cm} (1.1)

where $C(x,t)$ is the concentration of the solute species at a distance $x$ from the
solid liquid interface at time $t$, and $D$ is the solute diffusion coefficient. The
thickness of the grown layer at time $t$ is given as

$$d(t) = \left(\frac{1}{C_S}\right)^{\frac{1}{3}} \int_{t=0}^{t_1} D \left(\frac{\partial C}{\partial x}\right)_{x=0} \, dt$$  \hspace{1cm} (1.2)

where $C_S$ is the concentration of the solute in the solid phase at the
solid-liquid interface and $C_S$ may be obtained by using the relation, $C_S= kC_0$
with $k$ and $C_0$ being the segregation coefficient and the concentration of the
solute in the liquid phase at the solid liquid interface respectively.

ELOG of III-V semiconductor has been carried out in LPE on both
III-V (Zhang et al 1990 and 1995, Naritsuka et al 1995) and Si (Uen et al
and cooling schemes of LPE are discussed in chapter 2.
1.5.2 Vapour Phase Epitaxy

There are two types of Vapour Phase Epitaxy (VPE), and they are commonly called as chloride VPE and hydride VPE. In chloride VPE, the group III source is transported from chloride (e.g. GaCl$_3$) and group V source is transported from tri-chloride (e.g. AsCl$_3$) to form GaAs. In hydride VPE, group V source is transported from hydrides (e.g. AsH$_3$/PH$_3$) and group III source is transported from metal (e.g. In) mixing with hot HCl (e.g. InCl) to form InAs or InP.

The working principle of both hydride and chloride VPE is the same but the final reaction in both techniques is given by,

$$2\text{InCl} (g) + P_2 (g) + H_2 (g) = 2\text{InP} (c) + 2\text{HCl} (g)$$

(1.3)

The vapour pressure of InCl is very small and the gas needs to be generated in situ through the reaction between Cl and molten In. In Cl-VPE the precursor PCl$_3$ acts both as a reactant for generating InCl and is also the precursor for P. In HVPE this process is separated where HCl is used to generate InCl whereas the precursor for P is PH$_3$.

For HVPE, Equation (1.3) can be rewritten as,

$$2\text{In}(l) + 2\text{HCl}(g) = 2\text{InCl}(g) + \text{H}_2(g)$$

(1.4)

$$2\text{PH}_3(g) = \text{P}_2(g) + 3\text{H}_2(g)$$

(1.5)

At low pressures, the number of collisions between PH$_3$ molecules is relatively small and the decomposition becomes limited making the growth
reaction involving \( \text{PH}_3 \) molecules instead of \( \text{P}_2 \) or \( \text{P}_4 \). The reaction at low pressure is then commonly written as,

\[
\text{InCl} + \text{PH}_3 \leftrightarrow \text{InP(s)} + \text{HCl} + \text{H}_2
\]  

(1.6)

The reaction rate constant at the equilibrium is determined by the ratio of the partial pressures is given by,

\[
K_\gamma = \frac{[\text{HCl}]_{\text{eq}}[\text{H}_2]_{\text{eq}}}{[\text{InCl}]_{\text{eq}}[\text{PH}_3]_{\text{eq}}}
\]  

(1.7)

The relative gas phase supersaturation of the reaction, \( \gamma \) can be defined as the state of advancement of the growth reaction with respect to equilibrium and can be expressed as

\[
\gamma = \frac{[\text{InCl}][\text{PH}_3]}{[\text{HCl}][\text{H}_2]} K_\gamma - 1
\]  

(1.8)

The deposition of InP can either take place as a two-dimensional nucleation or as a Burton-Cabrera-Frank (BCF) spiral growth. The 2D mechanism applies to the growth of crystals from the vapour phase when the existing substrate surface is perfect, that is dislocation free. To absorb the first nuclei on the surface from where additional species will attach to form a continuous one-atomic high layer there is a demand on a lower critical supersaturation. In this lowest level the growth rate will be exponentially with supersaturation as,

\[
\text{Gr}_{2D} \propto \exp \left( -\frac{C_1}{\gamma T^2} \right)
\]  

(1.9)

where \( \text{Gr}_{2D} \) is the 2D growth rate, \( T \) is the temperature and \( C_1 \) is constant. For the substrate containing a high density of dislocations, the surface steps where
the atoms attach themselves by providing the emergence points of the dislocations having their Burgers vector normal to the surface.

The growth rate with group of dislocations will be given by,

\[
Gr_{BCF} = C \varepsilon \left( \frac{\gamma^2}{\gamma_1} \right) \tanh \left( \frac{\gamma_1}{\gamma} \right) \tag{1.10}
\]

Where \( C \) and \( \gamma_1 \) are constants for a given temperature and \( \varepsilon \) is the dislocation density. For low supersaturation \((\gamma < \gamma_1)\) \( Gr_{BCF} \) will be approximated by \( C\varepsilon(\gamma^2/\gamma_1) \) and for higher supersaturation \((\gamma > \gamma_1)\) by \( C\gamma \).

1.5.3 Molecular Beam Epitaxy

Molecular Beam Epitaxy (MBE) is one of the important growth techniques used extensively for the formation of compound semiconductor heterostructures with abrupt interface, well controlled thickness, doping and concentration. In MBE, the constituent elements of a semiconductor in the form of ‘molecular beams’ are deposited onto a heated crystalline substrate to form thin epitaxial layers in ultra high vacuum chamber. The selective growth by conventional MBE is a little difficult due to the high sticking coefficient of group III materials on the mask.

Because of the high degree of control with MBE, it is a valuable tool in the development of sophisticated electronic and optoelectronic devices. The growth rate is very low in this technique. Figure 1.5 shows the schematic diagram of MBE. ELOG on III-V semiconductor material has been carried out in MBE on both III –V (Bacchin et al 2000a, 2000b) and Si (Matyi et al 1987, Lee et al 1988) substrates.
1.5.4 Metal Organic Vapour Phase Epitaxy

Figure 1.6 shows the schematic diagram of Metal Organic Vapour Phase Epitaxy (MOVPE). It is a powerful growth technique in the compound semiconductor industry especially due to its ability to grow heterostructures with abrupt interface and well controlled thickness, which is necessary for the formation of optical and electronic device structures. Growth is performed from the vapour phase using metal organic (e.g. Tri-methyl indium) and hydride (e.g.PH$_3$) sources to grow InP. The growth is very low in this technique. Here the disadvantage is, the vertical growth rate is higher than the lateral growth forming facets. ELOG on III-V semiconductor material has been carried out in MOVPE on both III-V (Xiong et al 2007, Zhou et al 2007) and Si (Cheng et al 2008) substrates.
1.5.5 Atomic Layer Epitaxy

Atomic layer epitaxy (ALE) is a self-limiting, sequential surface chemistry that deposits thin-films of materials onto substrates of varying compositions. ALE is similar to Chemical Vapour Deposition (CVD), except that the ALE reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. The schematic diagram of ALE is shown in Figure 1.7. As ALE film growth is self-limited and based on surface reactions, which makes possible to control the deposition in atomic scale. By keeping the precursors separately throughout the coating process, control of atomic layer film can be obtained as fine as ~ 0.1 Å per monolayer. ALE has unique advantages over other thin film deposition techniques, as ALE grown films are conformal, pin-hole free and chemically bonded to the substrate. It is possible to deposit coatings perfectly uniform in thickness inside deep trenches, porous media and around particles. The film thickness range is usually 1-500 nm. ALE can be used to deposit
several types of thin films, including various ceramics, from conductors to insulators.

![Figure 1.7 Schematic diagram of ALE](image)

1.5.6 Chemical Beam Epitaxy

Chemical Beam Epitaxy (CBE) forms an important class of deposition techniques for semiconductor layer systems, especially III-V semiconductor systems. This form of epitaxial growth is performed in an ultrahigh vacuum system. The reactants are in the form of molecular beams of reactive gases, typically as the hydride or a metal organic. The schematic diagram of CBE growth system is shown in the Figure 1.8. The term CBE is often used interchangeably with Metal Organic Molecular Beam Epitaxy (MOMBE). The CBE is sometimes called as Metal Organic Chemical Beam Deposition (MOCBD). The growths of InP-based materials were carried out using CBE technique. In the CBE reactor the gas-handling system of MOVPE and the growth chamber of MBE are employed.
1.6 LITHOGRAPHY

The formation of three-dimensional (3D) relief images on the substrate for subsequent transfer of the pattern in the substrate is called lithography. The word lithography comes from the Greek words litho’s, meaning stone, and graphia, meaning to write. It literally means quite writing on stones.

The fabrication of an Integrated Circuit (IC) involves a great variety of physical and chemical processes performed on a semiconductor (e.g. Si) substrate. In general, the various processes used to make an IC fall into three categories: film deposition, patterning and semiconductor doping. Films of both conductors (Copper, Aluminium etc) and insulators (Silicon di Oxide, Silicon Nitride etc) are used to connect and isolate transistors and their components. Selective doping of various regions of Si allows the conductivity of the Si to be changed with the application of voltage. By creating structures of these various components, millions of transistors can be built and wired together to form the complex circuitry of a modern microelectronic device. Fundamental of all of these processes is lithography (Mack 2007).
To build the complex structures that makeup a transistor and the many wires that connect the millions of transistors of a circuit pattern, lithography and etch pattern transfer steps are repeated at least 10 times, but more typically 25-40 times to make one circuit. Each pattern being printed on the wafer is aligned to the previously formed patterns in a slow manner and the conductors, insulators and selectively doped regions are built up to the final device.

Lithography is important in two ways. First, a large number of lithography steps are needed in IC manufacturing. Lithography typically accounts for about 30% of the cost of manufacturing a chip. Lithography is a bottleneck technique in all IC fabrication factories and any drop in the lithography process is a drop in output of the factory. Secondly, it technically leads to further advances in transistor size reduction and thus chip performance and area. Lithography is not only technically important and is useful in the challenging process in IC manufacturing flow, but also the cost of manufacturing is less in good lithography process.

### 1.7 DIFFERENT TYPES OF LITHOGRAPHY

There are four important lithography techniques Optical Lithography, Interference Lithography, E-beam Lithography (EBL) and Nano imprint Lithography (NIL) for the fabrication of patterns.

#### 1.7.1 Optical Lithography

Optical lithography is the lithographic process that uses visible or ultraviolet light to form patterns on the photoresist through printing. Printing is the process of projecting the image of the patterns onto the wafer surface using a light source and a photomask. Equipment used for printing is known as printers or aligners. Patterned masks, usually composed of glass or
chromium, are used during printing to cover areas of the photoresist layer that shouldn't get exposed to light. Development of the photoresist in a developer solution after its exposure to light produces a resist pattern on the wafer, which defines which areas of the wafer are exposed for material deposition or removal.

Two types of photoresist materials are available namely, negative and positive photoresist. Negative resists are those that become less soluble in the developer solution when exposed to light, forming negative images of the mask patterns on the wafer. On the other hand, positive resists are those that become more soluble in the developer when exposed to light, forming positive images of the mask patterns on the wafer.

Commercial negative photoresist normally consists of two parts: 1) a chemically inert poly-isoprene rubber and 2) a photoactive agent. When exposed to light, the photoactive agent reacts with the rubber, promoting cross-linking between the rubber molecules that make them less soluble in the developer. Such cross-linking is inhibited by oxygen. So this light exposure process is usually done in a nitrogen atmosphere.

Positive photoresist also has two major components: 1) a resin and 2) a photoactive compound dissolved in a solvent. The photoactive compound in its initial state is an inhibitor of dissolution. Once this photoactive dissolution inhibitor is destroyed by light, the resin becomes soluble in the developer.

A disadvantage of negative photoresist is the fact that their exposed portions swell as their unexposed areas are dissolved by the developer. This swelling, which is simply volume increase due to the penetration of the developer solution into the resist material, results in distortions in the pattern features.
This swelling phenomenon limits the resolution of negative photoresist processes. The unexposed regions of positive photoresist do not exhibit swelling and distortions to the same extent as the exposed regions of negative resist. This allows positive resist to attain better image resolution. Figure 1.9 shows the basic steps for positive and negative photoresists in optical lithography.

Figure 1.9  Basic steps for positive and negative photoresists in optical lithography

There are three different types of printing in optical lithography contact printing, proximity printing and projection printing.
1.7.1.1 Contact printing

Contact printing refers to the light exposure process wherein the photomask is pressed against the resist-covered wafer with a certain degree of pressure. This pressure is typically in the range of 0.05-0.3 atmospheres. Light with a wavelength of about 400 nm is used in contact printing. The schematic representation of contact printing is shown in Figure 1.10.

Contact printing is capable of attaining resolutions of less than 1 micron. However, the presence of contact between the mask and the resist somewhat diminishes the uniformity of attainable resolution across the wafer. To alleviate this problem, masks used in contact printing must be thin and flexible to allow better contact over the whole wafer.

It also results in defects in both the masks used and the wafers, necessitating the regular disposal of masks (whether thick or thin) after a certain level of use. Mask defects include pinholes, scratches, intrusions and star fractures (Ham et al 1992).

Despite these drawbacks, however, contact printing continues to be widely used. Good contact printing processes can achieve resolutions of 0.25 micron or better.
1.7.1.2 **Proximity printing**

Proximity printing is another technique in optical lithography. As its name implies, it involves no contact between the mask and the wafer and hence the mask used in this techniques have longer and useful life than those used in contact printing. During proximity printing, the mask is usually only 20-50 microns away from the wafer. The schematic representation of proximity printing is shown in Figure 1.11.

The resolution achieved by proximity printing is not as good as that of contact printing (Okazaki 1991). This is due to the diffraction of light caused by its passing through slits that make up the pattern in the mask, and traversal across the gap between the mask and the wafer. This type of diffraction is known as Fresnel diffraction, or near-field diffraction, since it results from a small gap between the mask and the wafer. Proximity printing resolution may be improved by diminishing the gap between the mask and the wafer and by using light with shorter wavelengths.
1.7.1.3 Projection printing

Projection printing is employed in most of the modern optical lithography equipment. It also involves no contact between the mask and the wafer. In fact, this technique employs a large gap between the mask and the wafer, such that Fresnel diffraction is no longer involved. Instead, far-field diffraction is in effect under this technique, which is also known as Fraunhofer diffraction. The schematic representation of projection printing is shown in Figure 1.12.

Projection printing is the technique employed by most modern optical lithography equipment. Projection printers use a well-designed objective lens between the mask and the wafer, which collects diffracted light from the mask and projects it onto the wafer (Erdmann et al 2004). The capability of a lens to collect diffracted light and project this onto the wafer is measured by its numerical aperture (NA). The NA values of lenses used in projection printers typically range from 0.16 to 0.40.
The resolution achieved by projection printers depend on the wavelength and coherence of the incident light and the NA of the lens (Ito and Okazaki 2000). The resolution achievable by a lens is governed by Rayleigh's criterion,

\[
\text{Resolution} = k_1 \frac{\lambda}{\text{NA}} \quad (1.7)
\]

where \( k_1 \) – resolution factor, dependent on resist materials, process technologies and image formation technologies, \( \lambda \) – wavelength.

Resolution defines the minimum distance between two images for them to be resolvable. Thus, for any given value of NA, there exists a minimum resolvable dimension.

Using a lens with a higher NA will result in better resolution of the image, but this advantage has a price. The depth of focus of a lens is inversely proportional to the square of the NA. So improving the resolution by increasing the NA reduces the depth of focus of the system (Owen et al 1992).

\[
\text{Depth of focus} = k_2 \frac{\lambda}{(\text{NA})^2} \quad (1.8)
\]

where \( k_2 \) – resolution factor, dependent on resist materials, process technologies and image formation technologies.

Poor depth of focus will cause some points of the wafer to be out of focus, since no wafer surface is perfectly flat (Fukuda et al 1991). Thus, proper design of any aligner used in projection printing considers the compromise between resolution and depth of focus.
In the early 1970’s the required dimensions for the ICs ranged from 2 µm to 5 µm (Henderson 1995). Replication of these patterns was simply achieved by using mercury-arc based UV-light and bringing the photomask and the substrate in close proximity or in to contact during the exposure. Systems based on this operating principle are still useful today in micro fabrication due to its simplicity, low cost, high throughput and good process quality. These systems called UV-contact mask aligners reach resolutions from a few micrometers to the sub-micron level, depending on the exposure wavelength and the contact mode (Liu et al 1990). With fully automated systems, the throughput can exceed 100 wafers per hour and reach an overlay accuracy of 0.25 µm. Because the cost of optical lithography grows rapidly as line widths get smaller, research and utilization of alternative techniques are evolved.
1.7.2 Interference Lithography

Figure 1.13 shows the schematic sketch of Interference lithography. It utilizes the interference of two or more coherent laser beams that form an interference pattern on the substrate. Using photoresists similar to those used in optical lithography, this interference pattern can be transferred to the photoresist and subsequently to the other layers on the substrate. Near-field holographic lithography is very similar to interference lithography. This uses a phase mask near the substrate to divide one beam into two diffracted beams propagating at different angles. These two beams interfere and generate a diffraction pattern. Both methods can produce cost effectively over large areas, but only allow exposure of periodic patterns whose pitch is limited by the exposure wavelength. With a high index immersion fluid system a 32 nm half-pitch has been demonstrated using an exposure wavelength of 193 nm (French et al 2005) and 12.5 nm half-pitch using an extreme ultraviolet light source at 14.5 nm (Solak et al 2007).

Figure 1.13 Schematic sketch of Interference lithography
1.7.3 Electron Beam Lithography

Electron Beam Lithography (EBL) is based on the beam of electrons focused on a small spot with a Gaussian shape or on the beam of electrons cut down to the correct size and shape with an aperture. This beam is displaced with a magnetic field that is controlled with a computer. The beam exposes the electron beam sensitive material deposited onto the substrate in a similar fashion as a photoresist is exposed in optical lithography. EBL allows replication of geometrical data structures from the computer memory to the substrate. Therefore, it is used to generate templates for other lithographic techniques.

Figure 1.14 shows the schematic sketch of EBL system. It offers high resolution since wavelength of the electron is very small (Vieu et al 2000). The resolution of EBL is mainly limited by electron-solid interaction which broadens the beam in the resist. Another major limitation is the resolution of the resist. For the narrow patterns, development of the resist is challenging, since intermolecular forces prevent dissolution of the polymer in the solvent and the mechanical stability of the polymer is too low for wet processing.

When the beam is focused into a tiny spot, it can deliver only a small current and therefore the exposure time is increased. Moreover, high resolution resist tends to require higher exposure intensity than low resolution resists. At the same time, writing of large areas is very time consuming if the density of the pattern is high or the pattern geometry is challenging. The registration of patterns in EBL is not necessarily as good as the resolution of the system because the substrate has to be moved over large distances during exposure.
This requires fast and extremely accurate mechanical stage. Although these systems produce an unprecedented direct writing throughput, it is expected that it will take a long time before these systems migrate into the main stream lithography due to their development status, complexity and cost.

1.7.4 Nanoimprint Lithography

Nanoimprint Lithography (NIL) process is a mechanical process. Surface reliefs from the templates are embossed into a thin layer on the substrate. In principle, there are two basic versions of NIL. One is based on thermal embossing of thermoplastic polymers, while the other is based on UV-curable polymers. Some special imprints chemistries require both temperature and UV-light but they are not common (Schuster et al 2009). The NIL process and imprint instruments are very simple but allow extremely good resolution and a relatively fast replication process. In principle, NIL has no limitation in pattern geometry. It can copy any pattern produced with EBL or any other techniques. If patterns have a high aspect-ratio or large
distribution in pattern density or size, they can be very difficult to imprint simultaneously.

**Figure 1.15 Processing steps in NIL**

Figure 1.15 shows the processing steps in NIL. It uses thermoplastic polymer spin coat on the substrate. The thermoplastic polymer is heated above the glass transition point of the polymer and the heated template is brought into contact with the polymer. Once the polymer has filled all the cavities of the template, the substrate and the template are cooled down and the template is separated from the substrate. The negative replica of the template is created on the polymer.

### 1.8 SCOPE OF THE THESIS

The present thesis deals with the heteroepitaxial growth of II-V compound semiconductor $\text{Zn}_3\text{As}_2$ on GaAs substrates and III-V compound semiconductor InP on Si patterned substrates using near equilibrium LPE and HVPE techniques.
The scope of the present investigation is as follows:

1. To optimize the growth conditions for $\text{Zn}_2\text{As}_2$ epilayers on GaAs(100) substrate using LPE technique. To confirm the quality of the epilayers, the grown layers have been characterized by various techniques like X-ray Diffraction (XRD), Scanning Electron Microscope (SEM), Energy Dispersive X-ray Analysis (EDAX), Hall measurement techniques and optical absorption spectroscopy studies.

2. Planarization of Indium Phosphide seed layer is very important to achieve Indium Phosphide on Si for monolithic integration of light sources on Si for Si photonics. Chemical Mechanical Polishing (CMP) can be effectively used for planarization as well as polishing the InP seed layer. Both the topography and the morphology of the polished InP seed layer have been investigated by Atomic Force Microscope (AFM). High aspect ratio patterns on optical lithography have been fabricated on different substrates for ELOG to reduce the defects and dislocations on highly mismatch heteroepitaxial system. The surface morphology and cross-section of the patterns have been characterized by using SEM.

3. ELOG of InP has been carried out on different substrates using HVPE technique and the epilayers have been characterized by using High Resolution X-ray Diffraction (HRXRD), SEM, Photoluminescence (PL), Hall measurement and Etch Pit Density (EPD). The results have been compared with planar InP.