Chapter 1
INTRODUCTION
1 INTRODUCTION

1.1 Introduction

Discrete Wavelet Transform (DWT) is a transformation technique that is used in signal and image processing applications for translating input data from time domain to wavelet domain. The wavelet domain information obtained after transformation provides information on both time and frequency resolutions of input signal. With large number of signal and image processing applications such as medical image processing, remote sensing, satellite imaging, speech processing, communication and hyperspectral image processing applications requiring image processing techniques such as compression, fusion, registration, object detection and motion estimation it is advantageous work in wavelet domain. In this chapter a detailed discussion on wavelet transform and computation complexity in wavelet transform is presented. The major challenges in computing wavelet transform and implementing the same over hardware platforms are presented. Remote sensing using Micro Air Vehicles (MAV) is one of the time critical applications that require image processing algorithms to be faster and cost effective in terms of area and power.

1.2 Image Processing in MAVs

The vital and increasing role of Unmanned Autonomous Vehicles (UAVs) for military applications has been known however, the adoption of UAV technology for commercial applications is yet to be explored [1]-[3]. It has been increasingly apparent that small or micro UAVs are emerging in numerous applications of interest to the military. Fixed wing micro-air-vehicles [4], or MAVs, have been defined as those vehicles that have a wing span less than six inches in length. Perhaps most significant are those applications relating to observation, measurement or surveillance. One of the critical capabilities for
making a Small- and Micro-Air Vehicle (SMAV) autonomous and useful is the precise estimation of the SMAV states (pose and position) and 3D mapping of its surrounding environment [5]-[6]. Among many sensors for these purposes, 3D vision by video and laser scanning has distinct advantages [7]. Unlike navigational sensors (such as Global Positioning System and gyro) that provide information of only the vehicle's own motion with respect to the inertial frame [8], vision can provide information relative to the environment how close the vehicle is to an obstacle or whether there are moving objects in the environment [9]. Unlike Global Positioning System (GPS), which does not work in the shadow of satellite visibility, vision works in a cluttered urban environment or even indoors. At the same time, camera images are view dependent, tend to be noisy, and require a substantial amount of processing in order to extract useful information from them. On the other hand, to extract useful information from the navigation of MAVs, multiple cameras or sensors are mounted and the images captured from various locations are fused. Sensors mounted on MAVs could be of various types such as visible cameras, IR camera and SAR [10]. The data could be transferred in real time or stored on board the MAV. Multiple sensor data captured are transmitted to the base station with a 21-GHz data link and a high-definition visible camera (1-g mass) that uses a silicon charge-coupled device (CCD) array or CMOS camera of 1000 × 1000 pixels. Many MAVs would be used and each of them would have different types of cameras and hence the captured data would be down linked to the base station. On board processing platforms based on FPGA and ARM controllers for data capture for small MAVs have been demonstrated by ETH Zurich and MIT. Most of the onboard system operates at 120 frames per second with 320 × 240 pixel resolution with MAV travelling speed of 13 meters per second. Considering the operating speed of 100 frames per second, with MAV moving at 10 meters per second, every frame with rich information of images is received at 1 milliseconds and distance travelled is 1 centimetres. Every decision need to be taken in less than 1 milliseconds and the onboard processor need
to process new data received every 1 centimetre. If the processing speed is increased from 100 fps to 200 fps then the onboard processor need to process new data received at every 0.5 centimetre distance. Some of the most popular applications of MAV are Reconnaissance, Surveillance, Defence applications, Weather forecast, Wildlife study and photography, Crowd control, Targeting, Border surveillance, Traffic monitoring, Tracking criminals and illegal activities, Biochemical sensing and Inspection of pipes. During surveillance operation of MAVs, the image or video data captured need to be continuously downlinked to the base station for monitoring. Downlinking of data particularly image data needs compression. The input color image (24 bits per pixel) or video data acquired by camera operating at 100 frames per second with $256 \times 256$ frame resolution would require $(256 \times 256 \times 24 \times 100 = 157 \text{ Mega})$ bits of storage space per second. Compression of image data by more than 100% will be required for storing the data on board as well as for transmission. Compression is a three step process: transformation, thresholding and quantization and encoding. Transformation is to obtain multiple sub bands using wavelet techniques for identification of redundancy, the sub bands are quantized and encoded using entropy encoding techniques.

1.3 Image Compression

Image compression process reduces input data size as compatible to channel bandwidth for transmission and also for storage. Compression of image and video sequences are governed by standards to ensure interoperability over various platforms globally. JPEG, JPEG2000, MPEG and H.263 are few of the standards [11] that provide guidelines for compression of images and video sequences. The most popular technique for compression is in the transform domain that requires Discrete Wavelet Transform for transformation of input data into frequency sub bands, the transformed data is quantized and encoded using Set Partitioning in Hierarchical Trees (SPIHT) [12]-[13].
Figure 1.1 shows the block diagram of classical compression and decompression model.

Figure 1.1. Compression and Decompression Model

The compressed data is transmitted over communication channel and is reconstructed at the receiver with minimum loss for telemedicine applications. Figure 1.2 shows the JPEG2000 standard based compression and decompression model.

Figure 1.2. JPEG2000 based compression model

As per the JPEG 2K standard guidelines:

- DWT transforms input image to sub bands
- Quantization retains important information
- SPIHT compresses the quantized sub bands

Compression ratios of 1:100 or greater is achievable as per JPEG 2000 standards [14]. Wavelet compression involves analyzing an uncompressed image in a re-
cursive fashion, resulting in a series of higher resolution images, each “adding to” the information content in lower resolution images. The primary steps in wavelet compression are performing a discrete wavelet Transformation (DWT), quantization of the wavelet-space image sub bands, and then encoding these sub bands. Wavelet images by and of themselves are not compressed images; rather it is quantization and encoding stages that do the image compression. Image decompression, or reconstruction, is achieved by carrying out the above steps in reverse and inverse order. Thus, to restore the original image, the compressed image is decoded, dequantized, and then an inverse-DWT is performed. Because wavelet compression inherently results in a set of multi-resolution images, it is well suited to working with large imagery which needs to be selectively viewed at different resolution, as only the levels containing the required level of detail need to be decompressed.

The core of image compression unit is DWT. Designing DWT-IDWT as an IP core is one of the major challenging aspect of this research work. The two-dimensional DWT is becoming one of the standard tools [15] for image fusion in image and signal processing field. The DWT process is carried out by successive low pass and high pass filtering of the digital image or images. This process is called the Mallat algorithm or Mallat-tree decomposition [16]. Figure 1.3 shows an implementation structure of the DWT-IDWT [17]. Input signals is filtered using high pass and low pass filter and are down scaled to obtain the approximation and detail coefficients of the image. The reconstruction process further uses the high pass and low pass filters to obtain the original image. The filter coefficients need to be chosen such that there is perfect reconstruction.
For processing 2-Dimensional signals such as images, the original image is passed through low pass and high pass filter for first level decomposition. The transformed image is transformed further passed through a pair of low pass and high pass filters to achieve 2 level decomposition of original image as shown in Figure 1.4. The original image is first processed along the rows by the first stage low pass and high pass filters. The second stage filtering processes the row filtered wavelet coefficients along the column. Two stage filtering of original image generates four sub bands of wavelets, of which the LL band (the wavelet coefficients obtained after filtering along rows by low pass filter and followed by filtering along columns by low pass filter) contains the intensity information of the original image. The HH, HL and LH sub bands contain the edges or high frequency components of the original image in diagonal, vertical and horizontal directions respectively. Reconstruction of original image is carried out by processing all the four sub bands as per the algorithm and inverse DWT structure shown in Figure 1.4.

The LL band which contains the intensity information can be further decomposed into level-2 sub bands to obtain the intensity and edge information at next level of resolution. Every decomposition level leads to sub bands that are of half the size than the original image.
If the input data is 3D or a video sequence, then it is required to compute DWT in all three directions. First, DWT is computed on the rows, second on the columns and third in the temporal direction. Figure 1.5 shows the block diagram of 3D DWT decomposition using wavelet filters [13].
Discrete Wavelet transform (DWT) is widely used in signal and image processing applications as it provides both time and frequency localization. Compression standards such as JPEG and MPEG recommend wavelet filters for image transformation from time domain to frequency domain. Wavelet filters 9/7 and 5/3 are popularly used in image compression as well as in registration process. The advantages of DWT over Fourier and Cosine Transforms are that in DWT blocking artefacts are avoided in the processed image and the compression ratio achieved is higher than other techniques. Limitations of DWT are it is shift variant, directional insensitive and lacks phase information. Dual Tree Complex Wavelet Transform (DTCWT) is shift invariant and directional selective.
1.4 DTCWT

DTCWT is similar to DWT as computes wavelet sub bands that represent the low frequency and high frequency information in different wavelet bands. In comparison to DWT, DTCWT requires two tree structures the real tree filter band and imaginary tree filter bank to decompose the original image into complex wavelet sub bands [20]. The real tree is similar to DWT, the imaginary tree computes imaginary coefficients of the input image and corresponds to phase information and contains the structural information of input image. The DTCWT filters are Hilbert pair of DWT filters that are used in parallel to produce complex coefficients of input image being processed. The shift invariant property supported by DTCWT implies that the impulse response from the forward transform to inverse transform is independent of shift and aliasing[21]. With DTCWT supporting shift invariant property the sub bands of DTCWT are interoperable and can be interpolated in representation of shifted signals in spatial domain. This property is advantageous for image registration and fusion. The computation of 2D DTCWT coefficients produces directional selective sub bands in the complex domain which is useful in estimating motion information from the input image. DTCWT is similar to Fourier Transform as the shift in spatial domain is analogues to linear phase change in frequency domain. The DTCWT sub bands are one octave wide and hence aid detection of edges which provides compression techniques to eliminate redundancy and achieve higher compression with minimum loss of data. DTCWT uses $h_0$ and $h_1$ low pass and high pass filter respectively for the H tree computation, $g_0$ and $g_1$ the low pass and high pass filters for G tree computation[23].
Figure 1.6. Kingsburys-dual-tree-CWT

Figure 1.7. Kingsburys-inverse-dual-tree-CWT
Figure 1.6 shows the analysis structure for dual tree CWT and Figure 1.7 shows the inverse dual tree CWT structure. The inverse transform of CWT is computed by inversing the real and imaginary part of the forward transform filters. The low pass filters in the H tree (g0) and G tree (h0) need to satisfy half sample delay property [24] as given in “Equation. (1)”

\[
G_0(e^{jw}) = e^{-0.5jw}H_0e^{jw}
\] (1)

The expression in “Equation. (1)” can be rewritten in terms of magnitude and phase function as shown in “Equation. (2)”.

\[
|G_0(e^{jw})| = |H_0e^{jw}|
\]

\[
\angle G_0(e^{jw}) = \angle H_0e^{jw} - 0.5w
\] (2)

Selection of DTCWT filter coefficients need to satisfy half delay property, perfect reconstruction, good vanishing moments and linear phase.

In DTCWT, the input image is decomposed into real and imaginary parts at every level and thus provides not only frequency resolution but also phase information. As mentioned the advantages of DTCWT is it is shift invariant and directional selective. DTCWT computation is carried out by performing row processing and column processing on input image. Each of the processing generates real and imaginary wavelet coefficients. The two dimensional DTCWT algorithm [25] is shown in Figure 1.8
The input image $S$ comprising of $z_1$ and $z_2$ number of rows and columns respectively is decomposed into complex wavelet sub bands. The first level comprises of row processing and column processing stage. The first level decomposition produces sixteen sub bands. The four top most sub bands representing the low pass outputs are further processed in the second level to produce another sixteen sub bands. The real coefficients are indicated with the markers r, the row and column imaginary coefficients are indicated by $i_1$ and $i_2$ respectively. The DTCWT filters are represented by $H$ are used in decomposition process.
The major challenges in DTCWT computation is the selection of filter coefficients. Nick Kingsbury [23] has listed 7 types of filters Type-A to Type-G. Filters A is odd/even filters, B-G are Q-shift filters. Type A-C filters are (13,19)-tap and (12,16)-tap near orthogonal odd/even filter sets, Type-D-F are (9,7)-tap Antonini filters and Type-G is (5,3)-tap LeGall filters. These filters have been extensively used for various image processing applications such as motion estimation, denoising, texture analysis, segmentation, classification and watermarking. For image registration compression and fusion it is required to analyze the filter properties and choose appropriate filters. Secondly, it is required to design suitable architectures with optimum area, timing and power requirement. Thirdly, it is required to customize the designed architectures to be reconfigurable compatible to FPGA resources.

With advances in technology leading to scaling of transistors below 10nm, hardware platforms such as FPGAs and ASICs need to be designed to operate at very high speed and consume low power. DTCWT has advantages due to its abilities to analyze signal in multi-dimension, multiple scales and directions is spatially adaptive and does not suffer from aliasing artefacts. With more and more signal processing and image processing algorithms using DTCWT for analysis, the only requirement is the computational cost which is higher in DTCWT. The focus of this research is design of optimum architectures for DTCWT customizing its use in image processing techniques.

1.5 Need and Motivation

Considering and uncompressed gray scale (8-bits per pixel representation with intensity range between 0-255) image of size 640 × 480 contains 2457600 bits. With video recording of gray scale images at 24 frames per second the number of bits per second is 58982400 bits. The storage space for a one hour video sequence with 640 × 480
frame size captured at 24 frames per second requires 212336640000 bits of storage space. For high resolution video sequences with frame size greater than 1024 × 1024 color image (24 bits per pixel) storage sizes for a one hour data is 2174327193600 bits. If the frame capture rate is increased from 24 frames per second to 30 frames per second the storage space also increases and the storage space for one hour of video data will be 2717908992000 bits. Transmitting the raw data over communication channel with data rate of 64kbps requires 42467328 seconds or 11796.48 hours. Compression of image or video data improves transmission time and hence there is need for image or video compression that can help in transmission of data over existing transmission lines with minimum delay. In 3D data or video data a group of image defined by N1 × N2 × M (where N1 and N2 represents the number of rows and columns respectively and M represents the number of frames) it is required to compress the 3D data to ensure that there is very less transmission delay and also the data occupies very less storage space. For real time data transmission, with frame rate of 30 frames per second, every frame needs to be processed to obtain the compressed data in less than 33 mili seconds (1/30 fps). The compression process is two step: transformation and data encoding. Transformation of 3D data into level sub bands needs to be performed in less than 15 milliseconds assuming equal time distribution to both transformation and encoding.

In less than 15 milliseconds, 67 million multiplications and 58 million additions along with memory read and write operations need to be carried out for one-level DWT computation. Assuming data to be represented in 2’s complement 10-bit number system, in every 30 milliseconds multiplication, addition and memory operations have to be carried out. Power dissipation is another major challenge in high speed operations as power is directly proportional to frequency. Existing systems use software environment for telemedicine applications, image compression is also carried out using
software programs designed based on compression standards.

Discrete Wavelet Transform (DWT) is a transformation technique that provides information both in time and frequency domain for a given signal for analysis purpose. The input signal that can be 1-Dimensional (1D), 2-Dimensional (2D) or 3-Dimensional (3D), DWT transforms from spatial domain to time-frequency domain. Inverse DWT (IDWT) performs the inverse process of transforming form time-frequency domain to time domain. Thus DWT and IDWT form a transform pair [26]-[28]. DWT computation at every level is achieved with sub band filtering technique, where in the input data is processed using low pass and high pass filters and the filtered output is down sampled to obtain low and high frequency sub bands [29]. The filter coefficients are predefined and depend upon corresponding wavelet selected. Biorthogonal 4.4 or 9/7 filter bank for image compression [30] comprises of 9 filter coefficients for low pass and 7 filter coefficients for high pass. If the image size is $N \times M$ (N is the number of row pixels, M is the number of column pixels), it is required to perform N 1D DWT row wise and M 1D DWT column wise. Thus it is required to perform N+M 1D DWT computation. Each 1D DWT computation on the N rows requires low pass filtering and high pass filtering. Computation of every output of low pass filter requires 9 multiplications and 8 addition operations as there are 9 filter coefficients for low pass filtering. As there are M pixels in each row, 1D DWT computation of each row requires 9M multiplications and 8M additions. As there are N rows thus it is required to perform 9NM multiplications and 8NM addition operations. Similarly for computing high pass filter coefficients for the row elements it requires 7NM multiplications and 6NM addition operations. Computation of 1D DWT on the columns also requires 9NM multiplications and 8NM additions for low pass and 7NM multiplications and 6NM additions for high pass. Thus for a $N \times M$ image the total number of multiplications are $2(9NM+7NM)$ and $2(8NM+7NM)$ additions for level 1
decomposition. \( N \times M \) size image after low pass and high pass filtering and down sampling the data size reduces to \( N/2 \times M/2 \) and there are four sub bands. Level 2 decomposition operates on LL sub band which is of size \( N/2 \times M/2 \). The number of multiplications and addition operations for level 2 is \((9NM + 7NM)\) and \((8NM + 7NM)\) respectively. Thus for computation of \( i^{th} \) level DWT the number of multiplications and additions required are \( 2 \times (9NM + 7NM) \times 2^{-j} \) and \( 2 \times (8NM + 7NM) \times 2^{-j} \), where \( j = 0, 1, 2, 3, \ldots i \), for low pass and high pass respectively. The total number of multiplications and additions for computation of \( i \)-level DWT of input image of size \( N \times M \) using 9/7 wavelet filter is as given by,

\[
\left( \sum_{j=0}^{i} 2(9NM + 7NM) \times 2^{-j} \right)_{\text{mul}} + \left( \sum_{j=0}^{i} 2(8NM + 6NM) \times 2^{-j} \right)_{\text{addn}}
\]

for \( j = 0, 1, 2, 3, \ldots i \).

Video data consists of 2D sequences captured at successive time intervals. If a camera has a capture speed of 30 frames per second, which implies that there are 30 successive frames captured in one second. Video sequences can be represented as \( N \times M \times K \) data, which indicates that there are \( K \) frames each of size \( N \times M \). Video data is also termed as 3D data [31]. DWT computation of 3D data is carried out by performing 2D DWT computation of every frame and DWT computation of all frames[32]-[34]. Figure. 1.9 shows the representation of 3D DWT computation.
The input 3D data has eight frames and each frame has $8 \times 8$ elements. After 3D DWT computation the $8 \times 8 \times 8$ input data is decomposed into eight sub bands each of size $4 \times 4 \times 4$. In general for computation of level 1 DWT of 3D data requires

$$K \times \left[ \left( \sum_{j=0}^{i} 2(9NM + 7NM) \times 2^{-j} \right)_{\text{mul}} + \left( \sum_{j=0}^{i} 2(8NM + 6NM) \times 2^{-j} \right)_{\text{addn}} \right]$$

for $j = 0, 1, 2, 3, \ldots i$.

For an input image of size $512 \times 512 \times 8$, requires 67 million multiplications and 58 million additions for one-level decomposition. Apart from arithmetic operations, memory operations and data control operations for data storage and synchronization are required for DWT computation respectively. Computation complexity of DWT increases with increase in data size and number of levels.

Similar to DWT computation DTCWT computation complexity is increased...
by more than twice compared with DWT computation complexity. With DTCWT comprising of real and imaginary filters at each level, computing 3D DTCWT will generate four octaves with each octave comprising of 8 sub bands. Each octave will be of real and imaginary sub bands. The DTCWT computation consumes time and memory space, in order to reduce computation complexity several schemes and architectures such as lifting based scheme, distributive arithmetic algorithm are proposed and implemented for DWT. Many of the research papers focus on use of DTCWT for image processing applications rather than design of efficient architectures. Since 2001 there are more than 600 papers published in reputed journals on DTCWT for image processing applications, only 8-10% of these papers focus on hardware design and optimization. DTCWT computation complexity is twice higher than DWT computation. For hardware implementation of DTCWT it is required to design efficient architectures that is optimum in terms of area, timing and power requirements. It is required to analyze the DTCWT filter properties, design optimum filter coefficients and customize efficient implementation schemes for DTCWT implementation on FPGAs supporting reconfigurability. With DTCWT replacing DWT in image and signal processing applications, design of DTCWT-IP on FPGA platform will be of advantage for hardware designers.

1.6 Problem Statement

DWT being most popular scheme for image transformation, to reduce computation complexity several algorithms have been proposed. Most popular scheme is the lifting scheme algorithm that reduces the number of multipliers and adders in computation of DWT. Lifting scheme algorithms have been successfully implemented on FPGA platforms and have been demonstrated to operate at frequencies more than 100 MHz. Data dependency in lifting scheme reduces operating speed further and thus novel
techniques that can eliminate data dependency need to be designed. With development in parallel processing technology, use of multi core schemes can further improve computation speed. Distributive algorithm based approach have been proven to be a successful method for realization of filtering algorithms on FPGA platform, redundancies in filter coefficients and logic utilization on configurable logic blocks need to be utilized for improvement in performance of distributive algorithm architecture. Design and development of optimized algorithms and customized architectures for computation of 2D and 3D DWT is one of the major challenges for providing real time access to telemedicine applications with high speed network connectivity. DTCWT gaining popularity over DWT for signal and image processing applications, the major challenges is the design of high speed architectures that can process data faster and reduced computation complexity of DTCWT architecture that can occupy reduced area and consume less power dissipation. Design of high speed low power architectures for computationally intensive transformation technique such as DTCWT will enable designers to use DTCWT block in place of DWT for image processing applications. It is required to customize high speed low power algorithms and architectures for computation of DTCWT with suitable modification and customization. The focus of this research work is of two-fold: design of high speed architectures for DWT and extending the designed architectures for design of DTCWT.

1.6.1 Aim

The primary aim of this research work is to design and develop optimized algorithms and architectures for computation of 2D and 3D DWT,DTCWT for image compression over reconfigurable platform.
1.6.2 Objectives

From the discussion presented in the previous section and to meet the aim of this research work the following are the major objectives that have been completed:

- Design of improved architecture for DWT computation based on distributive arithmetic algorithm with parallel and pipelining schemes.
- Design and implementation of multicore platforms on FPGA for computation of 2D and 3D DTCWT.

1.6.3 Methods and Methodology

In order to meet the aim and objectives, the following methods are adopted:

- Extensive Literature survey was done referring to standard journals and online resources for image processing and image compression based on DWT for various applications. Review of various low power high speed VLSI implementation techniques have been carried out by referring to IEEE journals, books, manuals and related documents.
- Specifications and algorithms for image compression have been identified for software and hardware implementation and also building blocks for compression schemes are identified for VLSI implementation.
- Software reference model using Matlab and Simulink for image compression is developed and functionality is verified based on various input sources and compression ratios.
- Performance analysis of image compression in terms of MSE, PSNR and Maximum Error is carried out based on the developed software reference model.
• Internal architecture of configurable logic blocks and FPGA architectures from Spartan, Virtex have been studied to evaluate resource utilization of distributive arithmetic algorithm schemes.

• Advanced synthesis options and strategies for optimization of hardware resources on FPGA have been evaluated using Xilinx ISE.

• Numerical methods and data dependencies of lifting scheme algorithms have been evaluated and suitable modifications are derived to reduce data dependencies.

• HDL code for proposed algorithm and designed architecture are developed in Verilog HDL, suitable test vectors and test benches have been developed for functional verification.

• Test vectors for validation of logic correctness of DWT algorithm and architecture are identified and suitable methods for feeding data vectors for validations are derived.

• Design of novel architecture for DWT computation is carried out on FPGA platform optimizing area, power and speed performances. Verilog model is developed and is verified using ModelSim and synthesized using Xilinx ISE targeting Virtex FPGA.

• Pipelined architecture for DWT is designed on FPGA platform optimizing speed and power. HDL model developed is synthesized using Xilinx ISE and real time validation is carried out on FPGA development kit.

• Multi core architecture for implementation of DWT and DTCWT architecture is designed and Verilog HDL code is developed that is functionally verified for its logic correctness.
Suitable optimization schemes are set in advanced synthesis options in Xilinx ISE tool for improvement of power, area and speed performances.

Results obtained are compared with existing results and further improvement in architecture is carried out.

1.6.4 Thesis Organization

The major contributions in this research work are organized in four chapters and the conclusion is presented in last chapter. The thesis is organized as follows:

- Chapter II discusses in detail the concepts of DWT and DTCWT. There are several wavelet filters that have been reported for image compression, in this chapter analysis of wavelet filters highlighting the properties of filters and evaluation of filter coefficient representations for efficient hardware implementation is carried out. The recommendations presented in this chapter on DWT and DTCWT filters are used in succeeding chapters for DWT and DTCWT architecture design.

- Chapter III discusses, design and implementation of 2D and 3D DWT architectures for image and video encoding algorithm. A detailed discussion is presented on distributive arithmetic algorithm and pipelining schemes for improving the processing speed of DWT computation of 2D and 3D data.

- Chapter IV presents the concepts of DTCWT and its advantages over DWT. With complexity of DTCWT higher than DWT, novel algorithms based on systolic array schemes are proposed and high speed architecture for DTCWT computation is presented in this chapter. The major research contributions is design of high speed DTCWT architecture and development of the proposed architecture on hardware platform is presented in this chapter.
• Chapter V presents the discussion on distributive arithmetic based DTCWT architecture, the design approach and methodology adopted for customization of DTCWT architecture based on DA algorithm on FPGA platform is presented in this chapter. The results obtained in terms of area, power and timing are compared with existing references.

• Chapter VI is formulated to discuss the conclusion drawn out of the research work. The major contributions of this present research work are discussed in detail and the relevance of the current research work and its technical contributions are presented. A detailed discussion on scope for future work is also presented.