CHAPTER 7
Summary, Conclusions and Future Scope

7.1 Summary:

In this thesis, generation of various carrier comparison based scalar PWM algorithms for Voltage Source 2-level and 3-level Inverter fed Induction Motor Drive to reduce ripples in stator currents, switching losses, common mode voltage and acoustic noise have been carried out experimentally. The proposed PWM algorithms do not require complex computation such as sector identification and reference angle computation at every instant; hence complexity involved in implementation has been reduced.

7.2 Conclusions:

Nowadays, the induction motors become the workhorses of the industry due to their advantages. To achieve good speed control, induction motors requires variable voltage and variable frequency supply. However, required supply for induction motor can be obtained from pulse width modulated voltage source inverters. Hence, pulse width modulation (PWM) algorithms are very important for speed control applications.

In this thesis various Continuous and Discontinuous PWM algorithms has been implemented, and compared the performance characteristics of various CPWM and DPWM Algorithms at different modulation index experimentally on VSI fed Induction Motor Drive. The space vector approach requires the sector and angle computation for calculating gating sequence of the inverter, consequence burden on the processor and needs more execution time. Hence in order to reduce complexity of the traditional algorithm, a simplified PWM has been presented by using zero sequence signal, which gives exactly the same pulse pattern as the conventional SVPWM. From the experimental results it is observed that CPWM algorithm generates continuous pulse-pattern where as remaining DPWM modulators clamp to either positive or negative dc bus for 120° period in a fundamental cycle resulting reduction of switching losses by 33.33%. Furthermore it is also concluded that SVPWM gives CMV variations between ±Vdc/2, where as the proposed Reduced CMVPWM algorithm gives the reduced CMV variations between ±Vdc/6.
In order to reduce acoustic noise and total harmonic distortion, various Random PWM algorithms namely; RZVDPWM, DZVRPWM and VDRPWM have been implemented along with the conventional SVPWM for voltage source inverter fed induction motor drive. It is observed that in SVPWM algorithm the harmonic magnitudes are high at and around switching frequency; consequence more acoustical noise and harmonic distortion. Based on the experimental results, it is concluded that the Random PWM algorithms minimizes harmonic distortion and also confirms the superiority in the form of distributed spectra consequence reduced acoustic noise. Furthermore to reduce acoustical noise along with minimum switching loss the proposed algorithm uses Discontinuous PWM algorithms in conjunction with VDRPWM, the use of DPWM schemes reduces 33.33% of the switching loss of the inverter, it means that number of on and off of the inverter switch is reduced by 33.33% by clamping each of the pole voltage to either positive or negative bus for a period of 120°.

The two-level inverters are not capable of handling medium and high power applications. Hence, to meet these requirements, implementation of level shifted based CPWM and DPWM algorithms for a cascaded multi level inverter configurations has been carried out.

In this thesis, level-shifted carrier based scalar CPWM and DPWM algorithms for Cascaded 3 level Inverter fed v/f controlled Induction Motor Drive is presented. Four various level-shifted carrier control schemes have been evaluated and experimental results are presented. From the results it is concluded that the common carrier control scheme gives less harmonic distortion, but gives higher common mode voltage variation Vdc/3 which causes motor bearing currents effecting motor performance. Moreover the proposed later schemes reduce higher common mode voltage from Vdc/3 to Vdc/6 with lesser harmonic content. Finally, it can be concluded that among all the four control schemes inverted carrier control scheme gives lesser harmonic with reduced common mode voltage. It is also concluded that CPWM algorithm generates continuous pulse pattern which causes in the increment of switching losses of the inverter, where as DPWM algorithms clamps dc bus for a period of 120° in a fundamental cycle. Hence, the DPWM method minimizes the
switching losses of the inverter by 33.33% along with common mode voltage reduction.

Furthermore it is observed the harmonic magnitudes are high at and around the switching frequencies consequence in vibrations and more acoustical noise. Three types of random PWM algorithms namely random modulator, random carrier and random modulator-carrier PWM schemes have been implemented for the reduction of harmonics magnitude. Among all the three types of random PWM techniques, Random modulator-carrier PWM algorithm shows superior performance for cascaded inverter fed induction motor in terms of distributed harmonic spectra consequence reduced acoustic noise.

Finally, it can be concluded that proposed work implements various PWM algorithms and provide solutions to the problem of harmonic distortion, switching loss, acoustic noise and common mode voltage.

7.3 Future Scope:

A couple of conceivable proposals for future work to the present work carried out in this thesis are given beneath:

- The proposed PWM algorithms and multilevel inverter topology can be extended for grid connected P.V. System.
- These PWM algorithms can also be extended to modified multilevel inverter topologies like dual inverter and 2-level cascaded fed open end winding induction motor drives.
- These PWM algorithms can also be extended to closed loop controlled schemes such as vector controlled and direct torque controlled based three level and multilevel induction motor drive using Artificial Intelligence and Soft Computing techniques.