CHAPTER 5
Level Shifted based Scalar PWM Algorithms for Cascaded Multilevel Inverter fed Induction Motor Drive

5.1 Introduction:

In chapter-3 and 4, various PWM algorithms such as CPWM, DPWM, RCMVPWM and RPWM algorithms for 2-level inverter fed induction motor drive have been implemented. The performance studies also have been carried out and the results are presented.

It is demonstrated well that the voltage source inverter fed drives are more popular in modern applications. With the progression in control schemes of AC drives, PWM finds a tremendous development in AC drive applications and it is conceivable to diminish the total harmonic content. Today, it is difficult to connect a solitary power semiconductor device straightforwardly to medium voltage networks (3.3 kV, or 6.9 kV, and so forth). The 2-level inverters are not capable of handling medium and high power applications, hence multilevel inverter configurations are gaining importance.

Multilevel inverters integrate a variety of power semiconductors devices and capacitors, the yield of which, produce voltages with stepped waveforms. The multilevel inverters might be grouped extensively as:

- Diode clamped multilevel inverter
- Capacitor clamped multilevel inverter
- Cascade multilevel inverter

In the proposed work, in order to meet high power requirements, reduced harmonics and CMV implementation of level shifted based CPWM and DPWM algorithms for a cascaded multilevel inverter configuration has been carried out. These level-shifted based PWM algorithms give better performance in terms of common mode voltage reduction when compared with common carrier CPWM and DPWM techniques.

To validate the proposed PWM algorithms, experimental test has been carried out in cascaded 3-level inverter configurations and results has been presented and compared with other algorithms.
5.2 Cascaded three level Inverter:

Nabae, A., Takahashi, I. and Akagi, H introduces three level inverters which attracts the attention of researchers. The neutral-clamped circuit configuration suggested is simple and elegant but has few disadvantages. The neutral point fluctuation is a commonly encountered problem in this configuration. In flying capacitor topology, a capacitor is connected across the diodes. This method, alleviates the problem of the neutral-point fluctuations, but does not eliminate the problem.

Among the various multilevel inverter topologies, this chapter describes cascaded multilevel inverter drives. In the proposed circuit, 3-level voltage is obtained by cascading two 2-level inverters as shown in Fig. 5.1. In this circuit DC-link capacitors do not carry the motor currents and hence the voltage fluctuations in the neutral point are absent.

An isolated DC supply voltage of $V_{dc}/2$ is fed to each inverter. The notations $V_{a1o}$, $V_{b1o}$, $V_{c1o}$ individually denote the output voltages of inverter-1 with respect to the point 'O'. Similarly, the notations $V_{a2o}$, $V_{b2o}$, $V_{c2o}$ individually denote the pole voltages of inverter-2 with respect to the point 'O'. In inverter-2 of any phase, the pole voltage of $V_{dc}$ is obtained when top switching device of that phase in inverter-2 is turned on and the top switching device of the corresponding phase in inverter-1 is turned on. Similarly the pole voltage of $V_{dc}/2$ of inverter-2 of any phase is obtained when the top switching device of that phase in inverter-2 is turned on and the bottom switching device of the corresponding phase in inverter-1 is turned on. Furthermore, the pole voltage of zero in inverter-2 of given phase is obtained, if the bottom switching device of the corresponding phase in inverter-2 is turned on.

Therefore, the pole voltage of 0, $V_{dc}/2$ and $V_{dc}$ which is the feature of a three level inverter operation is obtained given in Table 5.1.

The general expression for the common mode voltage can be obtained from the inverter pole voltages as

$$V_{com} = \frac{V_{a2o} + V_{b2o} + V_{c2o}}{3}$$
Fig. 5.1 Proposed three-level cascaded inverter configuration

Table 5.1: Pole Voltage of Inverter-2

<table>
<thead>
<tr>
<th>Switches turn on Inverter-I</th>
<th>Switches turn on Inverter-2</th>
<th>Pole voltage of Inverter-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11 or S13 or S15</td>
<td>S21 or S23 or S25</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>S12 or S14 or S16</td>
<td>S21 or S23 or S25</td>
<td>$V_{dc}/2$</td>
</tr>
<tr>
<td>S11 or S13 or S15</td>
<td>S22 or S24 or S26</td>
<td>0</td>
</tr>
<tr>
<td>S12 or S14 or S16</td>
<td>S22 or S24 or S26</td>
<td>0</td>
</tr>
</tbody>
</table>

The main advantage of the proposed cascaded inverter is that if any of the top switching device of inverter-1 fails, it can be operated as a conventional 2-level inverter. This is accomplished by turning on the bottom switching devices of Inverter-1, i.e. the devices S14, S16 and S12 (Fig. 5.1) and only the devices of Inverter-2 (S21 through S26) are utilized. Another advantage is to obtain three level output, it requires only two DC power supplies of $V_{dc}/2$ each while the H-bridge topology requires three isolated DC power supplies (of $V_{dc}/2$ each). Nevertheless, The switches of inverter-2 in the top bank need not be rated for the full DC-link voltage of $V_{dc}$ because when the
corresponding bottom switch of inverter 1 and inverter 2 is turned on, the top switch of inverter-2 blocks the input voltage to \( V_{dc}/2 \) only.

### 5.3 Level Shifted PWM Algorithms for Reduced CMV:

Together with the advancement of multilevel inverter configuration showed up the test to stretch out conventional modulation strategies in the multilevel inverters. In the proposed approach, N-level output voltage is obtained by comparing N-1 carrier waveforms of the same frequency and amplitude with the modulator. The intersection point of these modulators with carrier signals gives the switching instant. The realization of these PWM techniques is obtained by taking SVPWM for the cascaded multilevel inverter configurations. The intersection points of reference signals with carrier signals give the switching instants. In the proposed carrier comparison approach, the modulating control signals have been obtained by adding a zero sequence signal to the sinusoidal reference signal as shown in Fig. 5.2. This chapter focused on some high frequency switching control carrier comparison schemes such as Common Carrier Control Scheme, Inverted Common Carrier Control Scheme, Phase Shifted Carrier Control Scheme and Inverted Phase Shifted Carrier Control Scheme for cascaded three level inverter fed AC drive.

![Fig. 5.2 Block diagram of scalar PWM technique for cascaded three level inverter configuration](image)
5.3.1 Common Carrier Control Scheme (CC):

Common carrier control scheme as shown in Fig. 5.3 is one of the PWM algorithm for multilevel inverter. For three level output two carrier waveforms and a reference signal with the amplitude $V_m$ and the 50 Hz frequency are required.

![Fig. 5.3 Proposed CC Control scheme for cascaded three level inverter](image)

The control idea is the top carrier and bottom carrier signal are in phase with each other and are compared with a three phase modulating reference signal to acquire three level operation. Top carrier signal generates the pulse pattern for inverter-1 and similarly bottom carrier signal generates pulse pattern for inverter-2.

5.3.2 Inverted Carrier Control Scheme (ICC):

In the inverted carrier control scheme as indicated in Fig. 5.4, top carrier and bottom carrier signal are in out of phase ($180^\circ$) with each other and are compared with a three phase modulating reference signal to obtain three level operation. Top carrier signal generates the pulse pattern for inverter-1 and similarly bottom carrier signal generates pulse pattern for inverter-2.

![Fig. 5.4 Proposed IC Control Scheme for cascaded three level inverter](image)

5.3.3 Phase Shifted Control Scheme (PS):

In the proposed phase shifted control scheme carrier signals of each leg are phase shifted by $120^\circ$, but whereas in the earlier scheme for all the three legs of the
inverter carrier signals are in the same phase. As shown in Fig. 5.5, it may be noted that top and bottom carrier signals are in the same phase.

![Diagram](image1)

**Fig. 5.5 Proposed PS Control Scheme for cascaded three level inverter**

### 5.3.4 Inverted Phase Shift Control Scheme (IPS):

In inverted phase shift control scheme, carrier signals of each leg are phase shifted by 120° and also the top and bottom carrier signals of same leg are in out of phase (180°) as shown in Fig. 5.6.

![Diagram](image2)

**Fig. 5.6 Proposed IPS Control Scheme for cascaded three level inverter**
5.4 Experimental Results:

To validate the performance of the proposed level shifted based carrier PWM algorithms, experimental tests have been conducted on 1 HP, 415 V, 1.8 A and 50 Hz induction motor drive and is fed by two 9.2 kVA DC-link converters. dSPACE 1104 control board has been used to generate switching pulses (1 kHz) for both inverters.

A DC voltage of 255 V is applied to inverter-1 and inverter-2, so that an effective DC voltage of 510 V is applied. To measure line voltage and current on a digital storage oscilloscope (DSO), a voltage sensor (LV20-P) and current sensor (LA20-P) regulator respectively is used. The obtained results are shown from Fig.5.7 to Fig.5.46.

Fig. 5.7 Common Carrier Control Scheme at \( M_i=0.81 \): Modulating Signal, Pulses for Inverter-I & II

Fig. 5.8 Common Carrier Control Scheme at \( M_i=0.81 \): Line Voltage, Stator Current
Fig. 5.9 Common Carrier Control Scheme: Harmonic distortion of line Voltage

Fig. 5.10 Common Carrier Control Scheme: Harmonic distortion of stator current

Fig. 5.11 Common Carrier Control Scheme: Common mode voltage
Fig. 5.12 Inverted Carrier Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II

Fig. 5.13 Inverted Carrier Control Scheme at $M_i=0.81$: Line Voltage, Stator Current
Fig. 5.14 Inverted Carrier Control Scheme: Harmonic distortion of line Voltage

Fig. 5.15 Inverted Carrier Control Scheme: Harmonic distortion of stator current

Fig. 5.16 Inverted Carrier Control Scheme: Common mode voltage
Fig. 5.17 Phase Shifted Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II

Fig. 5.18 Phase Shifted Control Scheme at $M_i=0.81$: Line Voltage and Stator Current
Fig. 5.19 Phase Shifted Control Scheme: Harmonic distortion of line

Fig. 5.20 Phase Shifted Control Scheme: Harmonic distortion of stator current

Fig. 5.21 Phase Shifted Control Scheme: Common mode voltage
**Fig. 5.22** Inverted Phase Shift Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II

**Fig. 5.23** Inverted Phase Shift Control Scheme at $M_i=0.81$: Line Voltage and Stator Current
Fig. 5.24 Inverted Phase Shift Control Scheme: Harmonic distortion of line Voltage

Fig. 5.25 Inverted Phase Shift Control Scheme: Harmonic distortion of stator current

Fig. 5.26 Inverted Phase Shift Control Scheme: Common mode voltage
Fig. 5.27 Common Carrier Control Scheme at $M_i=0.81$:
Modulating Signal, Pulses for Inverter-I & II: DPWM

Fig. 5.28 Common Carrier Control Scheme at $M_i=0.81$: Line Voltage, Stator Current: DPWM
Fig. 5.29 Common Carrier Control Scheme 1: Harmonic distortion of line voltage

Fig. 5.30 Common Carrier Control Scheme: Harmonic distortion of stator current

Fig. 5.31 Common Carrier Control Scheme: Common mode voltage :DPWM
Fig. 5.32 Inverted Carrier Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II: DPWM

Fig. 5.33 Inverted Carrier Control Scheme at $M_i=0.81$: Line Voltage, Stator Current: DPWM
Fig. 5.34 Inverted Carrier Control Scheme: Harmonic distortion of line

Fig. 5.35 Inverted Carrier Control Scheme: Harmonic distortion of stator current

Fig. 5.36 Inverted Carrier Control Scheme: Common mode voltage: DPWM
Fig. 5.37 Phase Shifted Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II :DPWM

Fig. 5.38 Phase Shifted Control Scheme at $M_i=0.81$: Line Voltage and Stator Current :DPWM
Fig. 5.39 Phase Shifted Control Scheme: Harmonic distortion of line Voltage

Fig. 5.40 Phase Shifted Control Scheme: Harmonic distortion of stator current

Fig. 5.41 Phase Shifted Control Scheme: Common mode voltage: DPWM
Fig. 5.42 Inverted Phase Shift Control Scheme at $M_i=0.81$: Modulating Signal, Pulses for Inverter-I & II: DPWM

Fig. 5.43 Inverted Phase Shift Control Scheme at $M_i=0.81$: Line Voltage and Stator Current: DPWM
Fig. 5.44 Inverted Phase Shift Control Scheme: Harmonic distortion of line voltage

Fig. 5.45 Inverted Phase Shift Control Scheme: Harmonic distortion of stator current

Fig. 5.46 Inverted Phase Shift Control Scheme at $M_i=0.81$: Common mode voltage: DPWM
### Table 5.2: Comparison of Line Current THD & Common Mode Voltage

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Control Scheme</th>
<th>SVPWM</th>
<th></th>
<th></th>
<th>DPWM1</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Voltage %THD</td>
<td>Current %THD</td>
<td>$V_{cm}$ (V)</td>
<td>Voltage %THD</td>
<td>Current %THD</td>
<td>$V_{cm}$ (V)</td>
</tr>
<tr>
<td>1</td>
<td>Common Carrier</td>
<td>29.46%</td>
<td>8.59%</td>
<td>$V_{dc}/3$</td>
<td>29.36%</td>
<td>8.54%</td>
<td>$V_{dc}/6$</td>
</tr>
<tr>
<td>2</td>
<td>Inverter Common Carrier</td>
<td>32.89%</td>
<td>9.22%</td>
<td>$V_{dc}/6$</td>
<td><strong>29.80%</strong></td>
<td><strong>9.07%</strong></td>
<td>$V_{dc}/6$</td>
</tr>
<tr>
<td>3</td>
<td>Phase Shifted</td>
<td>40.33%</td>
<td>12.41%</td>
<td>$V_{dc}/3$</td>
<td>37.28%</td>
<td>15.08%</td>
<td>$V_{dc}/6$</td>
</tr>
<tr>
<td>4</td>
<td>Inverted Phase Shifted</td>
<td>36.45%</td>
<td>10.81%</td>
<td>$V_{dc}/3$</td>
<td>36.02%</td>
<td>14.42%</td>
<td>$V_{dc}/6$</td>
</tr>
</tbody>
</table>

From the experimental results it is observed that the discontinuous PWM algorithm, clamp to DC bus for a total period of 120 degrees in a fundamental cycle, consequence the switching losses reduced to 33.33%.

As the proposed inverter configuration is capable of generating 3 level output (0, $V_{dc}/2$ and $V_{dc}$) for an input DC voltage of 510V. Fig. 5.7 to Fig.5.46 shows evaluation of four various multi carrier control schemes and experimental results shows that common carrier based conventional SVPWM algorithm causes a higher common mode voltage of $V_{dc}/3$ to $-V_{dc}/3$ shown in fig. 5.11, which causes motor bearing currents effecting motor performance. However, experimental results validates that by using proposed inverted carrier control scheme common mode voltage is reduced from $V_{dc}/3$ to $V_{dc}/6$. Therefore, the CMV is reduced by 50% with the discontinuous modulating signal based inverted carrier control schemes. The FFT analysis was carried out for the line voltage and phase current and the total harmonic distortion (THD) for various control schemes is presented and it is observed that among various control schemes, inverted carrier control scheme minimizes common mode voltage with fewer harmonic distortions.
5.5 Summary:

In this chapter, level-shifted carrier based scalar CPWM and DPWM algorithms for cascaded 3 level inverter fed v/f controlled induction motor drive is presented. The traditional approach requires sector and angle computation results increased complexity consequence burden on the processor for program execution, but whereas by using scalar approach, the same modulating control signals have been obtained without calculating angle and sector. This can be achieved by adding a zero sequence signal to the sinusoidal reference signals. In this chapter four various multi carrier control schemes have been evaluated and experimental results are presented. From the results it is concluded that the common carrier control scheme gives less harmonic distortion, but gives higher common mode voltage Vdc/3 which causes motor bearing currents effecting motor performance. Moreover the proposed later schemes reduce higher common mode voltage from Vdc/3 to Vdc/6 with less harmonic content. Finally, it can be concluded that among all the four control schemes inverted carrier control scheme gives lesser harmonic with reduced common mode voltage.

This chapter also concluded that CPWM algorithm generates continuous pulse pattern which causes in the increment of switching losses of the inverter, where as DPWM algorithms clamp to dc bus for a total period of 120° in a fundamental cycle. Hence, the DPWM diminish the switching losses of the inverter by 33.33% along with common mode voltage reduction.