CHAPTER 6

This second last chapter talks about the novel circuit of DVCC, which is compact and provides great results as per the expectations. The simulation results of this circuit are discussed in detail.
Chapter 6

LOW VOLTAGE DVCC: IT'S NOVEL CMOS REALIZATION

6.1 Introduction

Low voltage and low power mixed mode circuits design has gained importance in recent times due to the advent of portable electronics systems and mobile communication systems. The CC can be classified into three categories namely CCI, CCII and CCIII. The differential voltage current conveyor is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith. The CCII has a disadvantage that only one of input terminals has high input impedance (Y terminal). This disadvantage becomes evident when CCII is required to handle differential signals, as in the case of instrumentation amplifier. The design of such an amplifier requires two or more CCII’s.

6.2 Low Voltage DVCC

The DVCC is a defined to handle differential signals. This DVCC is a five-part building block which is explained by the following matrix equation:

\[
\begin{bmatrix}
V_X \\
I_{Y1} \\
I_{Y2} \\
I_{Z1} \\
I_{Z2}
\end{bmatrix} =
\begin{bmatrix}
0 & 1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 \\
-1 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_X \\
V_{Y1} \\
V_{Y2} \\
V_{Z1} \\
V_{Z2}
\end{bmatrix}
\]

Voltage and current relation for DVCC are as follows

\[V_X = V_{Y1} - V_Y \quad (a)\]

\[I_{Y1} = I_{Y2} = 0 \quad (b)\]
I_{Z1} = +I_x  \quad (c)
I_{Z2} = -I_x  \quad (d)

V_{Y1} = \text{voltage at node Y1}
V_{Y2} = \text{voltage at node Y2}
V_x = \text{voltage at node X}
I_x = \text{current at node X}
I_{Z1} = \text{current at output node Z1}
I_{Z2} = \text{current at output node Z2}

Figure 6.1 Schematic Diagram of DVCC
6.3 Novel CMOS DVCC

The DVCC as a block is used for application, which requires floating inputs. A novel CMOS realization of this block is given in figure 6.2.

![Diagram of Novel CMOS DVCC]

Figure 6.2 CMOS Realization of Novel DVCC

All MOSFET operate in saturation region and the sources are connected to bulk(substrate) to reduce body effect. MSFET M5 and M6, work as a current mirror which are set to drive two differential amplifier consist of MOSFET M1, M2, M3 and M4. The analysis of this circuit is also very much similar to the circuit of novel CMOS DVCC of chapter 5.
6.4 Simulation Results of DVCC

6.4.1 DC Analysis of DVCC

PSPICE simulation on the CMOS implemented circuit of modified DVCC, using level 3 model parameter give the good agreement with the theoretical results. This simulation has been done at supply voltage of 2.5V and ground voltage has been taken at -2.5V with bias voltage of -1.80V. The below Figure below shows the DC characteristic of modified DVCC; it shows that when DC voltage of 100mV is applied at input node Y_1 (V_1) and 60mV of voltage at node Y_2 (V_2), it gives the voltage of 40mV at node X (V_3). In this way it verifies the voltage relationship of the very first equation.

Figure 6.3 and Figure 6.4 shows the DC characteristic obtained by simulation. Figure 6.4 proves that equation (a) is correct. It is obtained by fixed V_{Y1} and varying V_{Y2}. By making Vin_1 fixed at 0 mV and varying the Vin_2 the variation in Vx is obtained which is shown in figure 6.4. This figure also verifies equation (a).

![Diagram](image)

Figure 6.3 Various Voltages’ Responses (DC)
Figure 6.4 Input Voltage Relations with $V_x$

Figure 6.5 Output Current Responses
Figure 6.5 shows the current relationship of DVCC. It can be obtained by putting $V_{Y1}$ as constant and varying the value of $V_{Y2}$. It shows that device get saturated when $V_{Y2}$ lies in between -1V to +1V i.e. $-1V < V_{Y2} < +1V$. The Figure 6.5 also shows output Current relation at terminal $Z_+$ and $Z_-$. In this case by making $V_{in1}$ constant and varying the value of $V_{in2}$, the current responses can be observed. This clearly shows that current’s variations are linear between -1V and +1V.

6.4.2 AC Analysis of DVCC

AC analysis of DVCC has also been done and simulation result is given in figure 6.6 and figure 6.7. Figure 6.6 verifies the voltage relation between input nodes. It also shows the range of frequency suitable for operation i.e. up to frequency 200MHz, the voltage relationship is fine. Figure 6.7 show that current relationship is also satisfying the equations (c, d) up to the frequency of 200 MHz.

![Figure 6.6 Frequency Responses of Voltages](image-url)
**Figure 6.7 Frequency Responses of Various Currents**

**Figure 6.8 Various Voltage's Responses**
6.4.3 Transient Analysis of DVCC

PSPICE simulation is also carried out for sinusoidal inputs. These results also give a good agreement between theoretical and experimental results. The results also verify the basic equations (a, c and d) for DVCC in time domain as in Figure 6.8. The THD was found out to be as 1% up to the frequency of 200 MHz.

6.5 Conclusion

A CMOS realization of DVCC has been described. The circuit is based on voltage and current mirror circuits. By cascading few more current mirrors in the output section of this circuit we can use this circuit in the applications which require high bandwidth. The simulation results using PSPICE program exhibit that the presented circuit design offers practical alternative solution to use the CMOS DVCC in application circuits instead of the DVCC elements. The circuit can be utilized in a number of interesting applications such as integrators, differentiators, filters and oscillators etc.
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References


