CHAPTER 3

PERFORMANCE ANALYSIS OF PIPELINED RADIX-2 SDF-SDC FFT USING MODIFIED CARRY SELECT ADDER

Wireless communication technology has enlarged the demands for signal processing operations such as Convolution, Correlation, Filtering and frequency transformation techniques. Fast Fourier Transform (FFT) is the basic implementation of the Discrete Fourier Transform (DFT) used in some communication systems PHY layer and DSP. The FFT algorithm started a new period in digital signal processing by reducing the orders of complexity of DFT multiplications compared to a normal DFT. Since multipliers and adders are very powerful hungry elements in VLSI designs, they result in consequent power consumption. In this work, pipelined Radix-2 SDF-SDC FFT using modified carry select adder, which is used to high processing speed and high performances of FFT processor.

3.1 Radix-2 FFT

Radix-2 FFT algorithm (Mactaggart et al.,) retaining to divides the N-point DFT into two N/2 point DFTs and a complex multiplication in between. The DFT of N-point time domain signal is represented by

\[ X_k = \sum_{n=0}^{N-1} x_n W_N^{nk} \]

\[ 0 \leq k \leq N-1 \]  

(3.1)

Where \( X_k \) is the DFT (frequency) representation of discrete signal \( x_n \), \( W_N^{nk} \) denotes the twiddle factor and \( N \) represents the number of points. The FFT has a hierarchical computation and the butterfly plays a central role in this computation. For the Radix-2
FFT algorithm with decimation in time, the butterfly allows the calculation of complex terms.

![Figure 3.1 Structure of Radix-2 FFT](image)

Radix-2 FFT algorithm calculates the FFT in following three levels a) Decompose an N-point time domain signal into N number of separate signals such that each consists of a single point. It is a multistage interlaced decomposition where odd indices and even indices get separated. b) Calculate the N frequency spectra corresponding to N time domain signals. C) Synthesize the resulting N number of spectra into a single frequency spectrum. In Radix-2 FFT consists of two types, one is Decimation in Time (DIT) FFT and next one is Decimation in Frequency (DIF) FFT. Input bits are given in reversing order and output is obtained as a normal order, in DIT FFT. But in DIF FFT, the input is given to normal order and the output is obtained as bit reversing the order.

The Radix-2 algorithm is used for finding frequency response of original discrete time domain signals. Discrete Fourier transform (DFT) calculates the frequency spectrum of discrete time signals. The complex multiplier is required for all stages (0 to N-1) to multiply input signal with twiddle factor values. Timing representation of frequency oriented signals is determined by using Inverse Discrete
Fourier Transformation (IDFT) technique, which is the reverse process of DFT processor. The complexity of DFT and IDFT processors (Meher et al.,) is founded as $O(N^2)$. Transformation period is long for finding the transformation process either time to frequency or frequency to time. From Figure 3.3, it is clear that some computational paths are required to perform FFT computation by using generalized Radix-2 DIF FFT. To reduce the computational path of FFT computation, input of each stage is divided into two streams and then they are processed with proper delay elements.

### 3.2 Single Path Delay Feedback- Single Path Delay Commutator (SDF-SDC) FFT

The SDF FFT is a serial processor which provides high-speed operation. The inputs are given into serial manner, in R2SDF FFT (Dickson et al.,). In this FFT (Fan et al.,) N/2 point input data is sequentially controlled with the help of Flip-Flop circuit. This FFT structure consumes some hardware utilization and power consumption due to utilizing or storing the bulk of unwanted intermediate processing signals. Hence, large power consumption is one of the main disadvantages of R2SDF FFT. Single Path Delay Commutator FFT has some single delay commutators at one stage. But in the case of SDF FFT, a single number of large delay feedbacks are used to implement the functions of FFT. Both SDF and SDC architectures are used in the proposed design. In the place of multiplier unit, Bit-Parallel Multiplier is used for multiply the subtracted data into corresponding twiddle factor values.

Complex input data is considered to perform the FFT function. In every step, there is single delay commutating function has been used to process the appropriate data points. The Multiplexer units have been used to provide control signals for performing Commutator functions. Further signed addition and signed subtraction units are used to perform accumulation and subtraction functions. When compared to SDF structure, SDC architecture has more computational paths to perform FFT function.
Hence, to improve the architectural performances of FFT combined Single-path Delay Feedback (SDF) – Single-path Delay Commutator (SDC) FFT architecture has been designed in this research work. This can be achieved by utilizing 50% of the same hardware resources for computing multiple functions. The architecture of 16 point Radix-2 SDF-SDC FFT is illustrated in Figure 3.2.

![Figure 3.2 Architecture of 16 point Radix-2 SDF-SDC FFT](image)

3.3 Carry Select Adder

A carry select adder is a combinational logic of arithmetic circuit, which adds the binary value of 2 N-bit numbers and outputs their N-bit binary sum and a 1-bit carry (Mohanty et al.,). Carry select adder comes in the group of conditional sum adder. Sum and carry are computed by assuming input carry as 1 and 0 prior the input carry comes. When the input value of carrying arrives, the actual calculated values of sum and carry are selected using a multiplexer. The FFT processor, the computational procedure includes a vast number of multiplications and additions. To implement the addition operation in the FFT processor, carry select adder has been used. In the existing method of SDF-SDC FFT using carry select adder, which is used to reduce the
power consumption of the FFT processor. The architecture of Carry select adder is illustrated in Figure 3.3.

![Figure 3.3 Architecture of Carry Select Adder](image)

In this research work, study the carry select adder, an adder group that introduces redundant hardware to create the carry calculations go considerably faster. The carry select adder consists of three 4-bit adders (4 Full adders) and one Multiplexer. Figure 3.3 shows the idea of an 8-bit carry select adder. The 8-bit adder is dividing in half. The upper half is executed by two self-determining 4-bit adders, one whose carry-in is hardwired to 0 (low adder), an additional carry-in is hardwired to 1 (high adder). In similar, these calculate two different sums for the higher-order bits. The carry-out of
the lower-order 4-bit adder controls multiplexers that choose between the two different sums. The Cout could be a 2:1 multiplexer, however a more straightforward circuit that diminishes the gate count. 4-bit adders in Figure 3.3 take four gate delays to process their sums and three gate delays to calculate the stage carry-out. The 2:1 multiplexers add two gate delays to the path of the high-order sum bits.

Carry select Adder (CSLA) is one of the greatest adders used in many data processors to achieve fast arithmetic functions (Tiwari et al.,). The carry select adder partitions the adder into some groups, each of which performs two additions in parallel using dual RCA's. The carry-select adder is based on module replication. The n-bit adder is separated into 'k' ripple-carry adders of n/k bits each and all these adder blocks are replicated. The simplest n-bit carry select adder is built using three n/2-bit ripple-carry adders. The first adder (Nagaraj et al.,) is utilized to calculate the lower half of the n-bit sum, while the other two calculate the higher half, one based on the assumption that the input carry is zero, the other based on the assumption that is one. In this manner, the calculation of the higher half can start instantly there is no need to wait for the lower half to finish. When the lower half of the sum is calculated and the next stage of the carry input value is available, the exact higher half of the sum is chosen by a multiplexer. It is not complicated to see that the overhead of this adder is quite dramatic. The required area and power consumption of this type of adder doubles on the RCA, because of the replication technique.

The simulation result of Existing Radix-2 SDF-SDC FFT using carry select adder is shown in Figure 3.4 and synthesis result of existing Radix-2 SDF-SDC FFT using carry select adder to determine the area consumption is illustrated in Figure 3.5. The Figure 3.5 shows that the number of LUTs and Slices required for existing Radix-2 SDF-SDC FFT using carry select adder. The number of Lookup tables (LUTs) required for implementing existing Radix-2 SDF-SDC FFT using carry select adder is 1714 and required number of occupied slices is 984.
Figure 3.4 Simulation Result of Existing Radix-2 SDF-SDC FFT using carry select adder
Figure 3.5 Synthesis Result of Existing Radix-2 SDF-SDC FFT using carry select adder to determine the area consumption
Similarly, the synthesis result for existing Radix-2 SDF-SDC FFT using carry select adder regarding delay is shown in Figure 3.6.

![Figure 3.6 Synthesis Result of Existing Radix-2 SDF-SDC FFT using carry select adder to determine the delay consumption](image)

In the case of existing Radix-2 SDF-SDC FFT using carry select adder, the time required for performing operation is 43.760ns.
Similarly, the synthesis result for existing Radix-2 SDF-SDC FFT using carry select adder regarding power consumption is shown in Figure 3.7.

**Figure 3.7 Synthesis Result of Existing Radix-2 SDF-SDC FFT using carry select adder to determine the power consumption**

In the case of existing Radix-2 SDF-SDC FFT using carry select adder, the power consumption is 3.778W.
Table 3.1 Performance analysis of Radix-2 SDF-SDC FFT using carry select adder

<table>
<thead>
<tr>
<th>Types /VLSI Concerns</th>
<th>Number of Occupied Slices</th>
<th>Number of LUTs</th>
<th>Delay(ns)</th>
<th>Power(W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radix-2 SDF-SDC FFT using carry select adder</td>
<td>984</td>
<td>1714</td>
<td>43.760</td>
<td>3.778</td>
</tr>
</tbody>
</table>

3.4 Proposed Method of Modified Carry Select Adder

In the carry select adder circuit, full adder circuit is reduced to improve the performances of the structure. A full adder is the important block of CSLA circuit. The carry select adder circuit consists of the three 4-bit adders and one multiplexer. The 4-bit adder consists of four Full adder structures. In the carry select adder, the full adder circuit has been reduced, so it is called modified carry select adder (MCSLA). In CSLA, the full adder has been used and in the MCSLA, the reduced full adder has been used.

3.4.1 Reduced Full Adder

Full Adder circuit has been realized and redundant functions are eliminated to improve the architectural performances. The Full Adder circuit consists of two XOR gate, two AND gate and a single OR gate to perform the 3-bit addition operation. Reduced Full Adder (RFA) circuit has been designed by using a minimal number of
logic gates. Also, Multiplexer (MUX) based RFA circuit has been designed in this work to further alleviates the performances of digital adder circuits.

Gate Count of Full Adder is determined as follows,

Gate Count of FA = Gate Count \[ (2 \times \text{XOR}) + (2 \times \text{AND}) + (1 \times \text{OR}) \]

Gate Count of FA = \[(2 \times 5) + (2 \times 1) + (1 \times 1)\] = 10 + 2 + 1 = 13

Gate Count of Reduced Full Adder = Gate Count \[ (2 \times \text{AND}) + (1 \times \text{OR}) + (2 \times \text{NOT}) + (1 \times \text{MUX}) \]

Gate Count of Reduced Full Adder = \[(2 \times 1) + (1 \times 1) + (2 \times 1) + (1 \times 4)\] = 2 + 1 + 2 + 4 = 9

The structure of Full Adder (FA) and Reduced Full Adder (RFA) is illustrated in Figure 3.8 and Figure 3.9.

Figure 3.8 Full Adder Circuit

Figure 3.9 Reduced Full Adder Circuit
Full Adder structure is simplified by using some Boolean logic. General expression to find the Sum and Carry of Full adder is given in Equation (3.2) and (3.3)

\[
\text{Sum}= A\oplus B\oplus C \tag{3.2}
\]

\[
\text{Carry}=AB+C(AB' +A'B) \tag{3.3}
\]

Reduced Full Adder structure is simplified by using of demorgan’s theorem and some Boolean logic. General expression to find the Sum and Carry of Reduced Full adder is given in Equation (3.4) and (3.5)

\[
\text{Sum} = \sum_{A=0}^{1} [X \overline{A} + XA] \tag{3.4}
\]

Where

\[
X = (B+C).\overline{BC}
\]

\[
= \overline{B}C + \overline{C}B
\]

\[
= B \oplus C
\]

\[
\overline{X} = (B+C).\overline{BC}
\]

\[
= (\overline{B}C + \overline{C}B)
\]

\[
= BC + \overline{BC}
\]

\[
= \overline{B} \oplus C
\]

\[
\text{Carry} = \sum_{A=0}^{1} [BC\overline{A} + (B+C)A] \tag{3.5}
\]

In Figure 3.10 shows that the architecture of modified carry select adder structure. The 4-bit adder consists of 4 full adder circuits. The full adder is a logical circuit that performs an addition operation on three binary digits and just like the half adder, it also generates a carry out to the next addition column. Then a Carry-in is a
possible carry from a less significant digit, while a Carry-out represents a carry to a more significant digit. Then the full adder circuits are reduced in this architecture.

![Diagram of Modified Carry Select Adder Structure](image)

**Figure 3.10 Architecture of Modified Carry Select Adder Structure**

In the modified carry select adder, the full adder circuit is greatly reduced. The number of gate counts is reduced in full adder circuit. The reduced full adder circuit is incorporated into carry select adder circuit, which is called as modified carry select adder (MCSLA). In modified carry select adder the area consumption has been reduced than the carry select adder.
3.4.2 Pipelined 16 point Radix-2 SDF-SDC FFT using Modified Carry Select Adder

In this research work, the pipelined 16 point Radix-2 SDF-SDC FFT using modified Carry Select Adder has been proposed. In the existing method of FFT, the power consumption is large and also the processing speed is low. The proposed architecture of pipelined 16 point Radix-2 SDF-SDC FFT using Modified CSLA has been illustrated in Figure 3.11.

In the proposed architecture consists of butterfly elements, delay and multiplexer. In the butterfly elements, addition and subtraction operation has been done. The multiplexer is used to control the signals. In this architecture, the modified carry select adder is used for adder operation. In the proposed method, 16 point inputs are given to real and imaginary part of first stage. In the first stage, Single path delay feedback has been used. The real and imaginary input values are delayed by 8. The input values and delayed values are considered to adder and subtractor operation. In the adder operation, the modified carry select adder has been used. The output of first stage is given to the input of second stage. Single path delay Commutator is used in second, third and final stages. In these stages, additionally the Commutator structure is used for convert the one signal into another signal.
Figure 3.11 Proposed Architecture of pipelined 16 point Radix-2 SDF-SDC FFT using Modified CSLA
The pipelined SDF-SDC FFT using carry select adder has been designed, that is used to reduce the power consumption but it increase the hardware slices. So, modified the carry select adder circuit, which is used to reduce the hardware slices, LUTs, delay and also power consumption. In the modified carry select adder, the full adder circuit is reduced. So, the number of logic gates also reduced. Finally, the modified carry select adder circuit is integrated into 16 point Radix-2 SDF-SDC FFT processor. When compared to traditional equivalents, the proposed architecture which is used to improve the high processing speed and high performances of FFT processor. By using modified carry select adder the FFT processing time is reduced and also the speed can be improved.

3.5 Results and Discussion

The proposed design of pipelined Radix-2 SDF-SDC FFT using Modified CSLA has been made by using Verilog Hardware Description Language (Verilog HDL). The simulation results have been evaluated by using ModelSim 6.3c and Synthesis Performances are estimated by using Xilinx 10.1i (Package: pq208, Family: Spartan-3, Device: Xc3s200) design tool. The simulation result of proposed pipelined Radix-2 SDF-SDC FFT using Modified CSLA is illustrated in Figure 3.12.
The synthesis result of proposed Radix-2 SDF-SDC FFT using modified carry select adder to determine the area consumption is illustrated in Figure 3.13. The Figure 3.13 shows that proposed Radix-2 SDF-SDC FFT using Modified Carry Select Adder, the required number of LUTs is 1679 and required Slices is 945.
Figure 3.13 Synthesis Result of proposed Radix-2 SDF-SDC FFT using modified carry select adder to determine the area consumption
Similarly, the synthesis result for proposed Radix-2 SDF-SDC FFT using modified carry select adder regarding delay is shown in Figure 3.14.

![Synthesis Result](image)

**Figure 3.14 Synthesis Result of Proposed Radix-2 SDF-SDC FFT using Modified carry select adder to determine the delay consumption**
In the case of proposed Radix-2 SDF-SDC FFT using modified carry select adder, the time required for performing operation is 41.456ns.

Similarly, the synthesis result of proposed Radix-2 SDF-SDC FFT using modified carry select adder regarding power consumption is shown in Figure 3.15.

![Synthesis Result of Proposed Radix-2 SDF-SDC FFT using Modified carry select adder to determine the power consumption](image)

**Figure 3.15 Synthesis Result of Proposed Radix-2 SDF-SDC FFT using Modified carry select adder to determine the power consumption**

In the case of proposed Radix-2 SDF-SDC FFT using modified carry select adder, the power consumption is 1.370W.
The proposed Radix-2 SDF-SDC FFT using modified carry select adder in terms of LUTs, Slices, Delay and Power values are shown in Table 3.2. The main goal of the research work is to reduce the area, delay and power consumption of the architecture.

**Table 3.2 Performance Analysis of Proposed Radix-2 SDF-SDC FFT using Modified Carry Select Adder**

<table>
<thead>
<tr>
<th>Types /VLSI Concerns</th>
<th>Number of Occupied Slices</th>
<th>Number of LUTs</th>
<th>Delay(ns)</th>
<th>Power(W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed Radix-2 SDF-SDC FFT using modified carry select adder</td>
<td>945</td>
<td>1679</td>
<td>41.456</td>
<td>1.370</td>
</tr>
</tbody>
</table>

Table 3.2 shows that the proposed Radix-2 SDF-SDC FFT using modified carry select adder offers 3.95% reduction in occupied slices, 2.04% reduction in LUTs, 5.26% reduction in delay and 63.7% reduction in power consumption than the existing method. The performance evaluation of both Radix-2 SDF-SDC FFT using carry select adder and proposed Radix-2 SDF-SDC FFT using modified carry select adder is pictorially represented in Figure 3.16.
3.6 Summary

The proposed pipelined Radix-2 Single Path Delay Feedback (SDF) – Single Path Delay Commutator (SDC) FFT using Modified Carry Select Adder has been designed through Very Large Scale Integration (VLSI) System design environment. In modified carry select adder, the reduced full adder is designed using less number of gates compared to the conventional Full adder. These reduced adders are applied to the carry select adder to analyze and improve the performance. The modified carry select adder is incorporated into Radix-2 SDF-SDC FFT processor. The main goal of this research work is to reduce the processing time and improve the speed of the FFT.
processor. The proposed method is used to reduce the slices, LUTs, delay and power consumption. The proposed pipelined Radix-2 SDF-SDC FFT offers 3.96% reduction in hardware slices, 2.04% reduction in the number of LUTs, and 5.26% reduction in delay and 63.79% reduction in power consumption than the existing Radix-2 SDF-SDC FFT. In future, the proposed architecture will be useful in OFDM-based digital communication to perform the function of frequency transformation and to analyze the spectrum characteristics of digital inputs. In this chapter, the numbers of computational stages are increased and also the delay elements are increased. Therefore, the Radix-4 SDC FFT will be discussed in the next chapter.