CHAPTER 6

HARDWARE IMPLEMENTATION OF THE LIFTING DISCRETE WAVELET TRANSFORM

For high speed, less area utilization and minimum delay, the Lifting Scheme based Image Compression is incorporated into the Discrete Wavelet Transform (DWT). The hardware implementation of the proposed Lifting Wavelet Transform (LWT) has been designed and implemented in Spartan-3 based Field Programmable Gate Array (FPGA) board. The specification of hardware is shown below:

**Family** : Spartan-3
**Device** : XC3S200
**Package** : PQ208
**Speed**  : -5
**Software** : Xilinx 10.1 ISE design

Spartan-3 FPGA device has 208 pins for input and output, 123 pins among this act as I/O pins. Flat Ribbon Cable (FRC) is used for interconnection of external devices into Spartan-3 FPGA device. It consists of a crystal oscillator which provides 16 MHz frequency as operating frequency. For validating the output in Spartan-3 FPGA device, external devices for LED is interconnected through FRC cable which is demonstrated in below Figure.6.1. Input data is given to the Spartan-3 FPGA board, and the results are displayed in LED external device shown in figure.6.1. The process of OFDM techniques are implemented by using sequential logics.

An FPGA contain three main types of resources:

- Logic blocks;
- I/O blocks for interfacing with the pins of the package;
- Interconnection wires and switches
6.1 Field Programmable Gate Array (FPGA) Implementation

FPGA is unique in relation to other logic technologies like CPLD and SPLD because FPGA do not contain AND or OR planes. Rather, FPGA comprises of logic blocks for actualizing the required functions. At the point when a circuit is executed in a FPGA, the logic blocks are modified to understand the essential functions and the routing channels are customized to make the required interconnections between logic blocks. The FPGA device is designed by utilizing the In-System Programming (ISP) method, which implies that the FPGA can be customized while the chip is as yet connected to its circuit board. The capacity cells in the LUTs in a FPGA are unstable, which implies that they lose their stored contents whenever the power supply for the chip is turned off. Thus the FPGA must be programmed each time power is applied.

Figure 6.1 Hardware implementation of VLSI Architecture based Lifting Scheme
Of this, a small memory chip that holds its information permanently, called a programmable read-only memory (PROM) is incorporated on the circuit board that houses the FPGA. The storage cells in the FPGA are loaded consequently from the PROM when power is connected to the chips. Present day FPGA families develop the above abilities to incorporate larger amount functionality settled into the silicon. Examples of these incorporate multipliers, generic DSP blocks, embedded processors, high speed I/O (Input/output) logic and embedded memories. Therefore, current FPGAs (large-scale) are PSoC (programmable system-on-chip) with heterogeneous modules. Some of these basic functions are discussed below. With embedded hard digital signal processing blocks, FPGAs are a perfect solution for high-performance, high-precision DSP applications.

The DSP block architecture executes different basic DSP functions with greatest performance and least logic resource utilization. Notwithstanding multipliers, each DSP block has functions that are frequently required in typical DSP algorithms. These functions incorporate pre adders, adders, subtractors, accumulators, coefficient register storage and a summation unit. With these rich elements, the DSP blocks in FPGAs are ideal for applications with superior and computationally intensive signal processing functions. For example, Finite Impulse Response (FIR) separating, FFT/IFFT and computerized up/down conversion. Also on a similar topic, some FPGAs have simple components notwithstanding advanced capacities.

The most widely recognized simple component is programmable slew rate and drive quality on each output pin, permitting to set moderate rates on softly stacked pins that would somehow or another ring or couple unsatisfactorily, and to set more grounded, quicker rates on intensely stacked sticks on fast channels that would some way or another run too gradually. Another generally regular simple component is differential comparators on information pins intended to be associated with differential signaling channels.
A few "mixed signal FPGAs" have incorporated peripheral analog-to-digital converters and digital-to-analog converters with analog signal conditioning blocks enabling them to work as a system-on-a-chip. High-performance, high-density FPGAs support a assortment of differential and single-ended I/O standards, and effectively interface with backplanes, host processors, buses, and memory devices. FPGA I/O pins have the system-level performance and flexibility required to communicate with a large number of devices.

The variant of Discrete Wavelet Transform (DWT) named Lifting Wavelet Transform (LWT) based image compression is applied into the various image processing applications. The proposed codec is applied into the decomposed image to view the compressed image. By using the Integer wavelet transform (IWT), the given input image will be decomposed and then the decomposed image is encoded and decoded by using the ODCHS (Orthogonal Diagonal Cross Hair Search) Algorithm codec. By using the ALTERA DE2 board, the decoded image is to be displayed. The implementation is carried out in FPGA. This implementation is examined corresponding to the clock period through delay and resource utilization is calculated through slices, slice Flip Flops, Look up tables, I/O Blocks and Global clock pins. The resource consumed by implementation is listed in table 6.1 shown through figure 4.9. This implementation performed well with the clock time of 4.873ns which is shown in figure 4.10.

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Utilization</th>
<th>Available</th>
<th>Percentage Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slices</td>
<td>27</td>
<td>3584</td>
<td>0%</td>
</tr>
<tr>
<td>Number of slice flip flop</td>
<td>49</td>
<td>7168</td>
<td>0%</td>
</tr>
<tr>
<td>Number of 4 input LUTs</td>
<td>34</td>
<td>7168</td>
<td>0%</td>
</tr>
<tr>
<td>Number of bonded IOBs</td>
<td>30</td>
<td>141</td>
<td>21%</td>
</tr>
<tr>
<td>Number of GCLKs</td>
<td>1</td>
<td>8</td>
<td>12%</td>
</tr>
</tbody>
</table>
Similarly when implementing Multiband Wavelet Transform in FPGA it was observed that it occupies 10 Lookup Tables and 5 slices.

![Simulation Waveform for the Multi-band Wavelet transform](image)

**Fig: 6.2 Simulation Waveform for the Multi-band Wavelet transform**

### 6.2 Summary

The hardware implementation of the lifting scheme based on Discrete Wavelet Transform (DWT) has been designed and implemented in Spartan-3 based Field Programmable Gate Array (FPGA) board. The device used in Spartan-3 is XC3S200, package is PQ208 and the speed fixed is -5. The lifting scheme based image compression incorporated into Discrete Wavelet Transform (DWT) is simulated by using Modelsim XE III 6.3c and the number of slices, LUT’s and delay have been calculated by Xilinx 10.1 ISE design.