CHAPTER VII

CONCLUSIONS AND FUTURE SCOPE OF WORK

7.1 Conclusions

The overall goal of this research work is to implement Filter Bank Multicarrier (FBMC) transceiver architecture on FPGA hardware and to emphasize various aspects of physical layer for future communication system. In order to meet the desired goals, different multicarrier modulation techniques such as FBMC and OFDM schemes were thoroughly examined. The background of this study includes evaluation of present and future developments in the field of wireless communication system and applications were presented in Chapter 1. Simulation results and analytical expressions were used for the study. Based on compatibility and inherent features, FBMC was identified for further study. Information on previous work, present work, and literature survey was presented in Chapter 2. There was a various exploration on existing multicarrier modulation techniques related to future applications and development. FBMC was identified still in the research stage and can be considered potential candidate for future wireless communication applications by avoiding some of the drawbacks of OFDM. The main contribution of this work extends over the present research gap of existing multicarrier modulation techniques and its hardware implementation.

The design and implementation of suitable architecture for FBMC transmitter and receiver is a challenging task. In this thesis efficient FBMC transceiver architecture is designed and implemented on Artix 7 FPGA for future communication system as an alternative to conventional OFDM schemes. FBMC transmitter and receiver are designed starting from signal model using VHDL code and synthesize in Xilinx ISE Design Suite. An implementation employing on the transmitter part consist four modules which are SIPO, IFFT, PISO and polyphase filter modules. Each of these modules was tested using ModelSim software and chipscope pro tool in the development stage. This is to guarantee that the designed module was effectively working when executed in the FPGA hardware. The working of IFFT module was simulated and results would be compared with Matlab software.
The same process was done at the receiver side apply the same modules as the transmitter, but using a pipelined FFT instead of IFFT module. Similarly, working of FFT module was simulated and results would be compared with Matlab software during implementation stage. The synthesized results show that proposed FBMC transmitter and receiver design better area results in terms of slice registers, LUT’s and DSP slices compared to previous design. Finally, both the FBMC and OFDM transceivers architectures have been described and implemented for pair comparison purpose. The simulation based results conclude that the FBMC technique have the potential to enhance the performance in terms complexity overhead, transmit power, latency(57.54%), throughput(48.90%), BER and SNR compared to OFDM system.

Both OFDM and FBMC strategies depend on the basic working principles of IFFT/FFT computational engines. However, the procedure of adding CP in OFDM prompts an overhead that adversely impacts on the transmission bandwidth efficiency. Though cyclic prefix is absent in case of FBMC and blend of filter banks prompts greatest productivity and information transmission speed. A similar channel bank can be utilized for transmission and reception in FBMC transceiver architecture which ensures low BER and high performance compatibility in terms latency and throughput. The out-of-band reduction of the prototype filter amplitude curve in FBMC system assures spectral preservation of other subscribers which leads to new physical layer containment for future communication system. FBMC also offers additional functionalities and performance gain compared to conventional multicarrier techniques. Hence consequently it fulfills the criteria for presence and aggregate acknowledgment for new ideas for future wireless communication systems such as 5G and cognitive radio.

7.2 Future Scope of Work

This examination work can be considered as an underlying point for some different zones of research which are focused towards advancement of filterbank based communication frameworks. In this thesis, we presented an implementation of FBMC transceiver on FPGA for FBMC based communication system. The next step of this research work demonstrate the usefulness and practicality of FBMC based transceivers in real time applications such as spectrum sensing in cognitive radio and vehicle to vehicle
communication. The enhancement of this work can be carried out in terms of coding efficiency using some other suitable FFT/IFFT architectures. Even the latency can be further reduced by using suitable computing algorithms in both transmitter and receiver side, which ensures higher throughput of data stream. For the future works, it is recommended to create different modules, for example, interleaving block, error detection and correction module, and RF part in the transceiver. These modules will make an entire arrangement of FBMC system for transmission and reception of signals in the communication system. For further verifying of simulation results of FBMC transceiver, Universal Radio Peripheral, which is Software Defined Radio platform, can be utilized for acknowledgment of complete framework of communication system.