CHAPTER II

LITERATURE REVIEW

The primary objective of literature survey is to gather basic information with the current literature and related research subject. The research work reported in this thesis comprises of investigation of multicarrier modulation technique for Cognitive Radio environment. It includes study of conventional multicarrier techniques like OFDM, and FBMC techniques. Discuss the implementation aspects of these techniques in to the hardware platform. Then, do a comparative analysis of both the techniques with existing literature and find the research gaps to adopt the new technology. The source of literature survey is from Journals, books, Internet and from other accessible sources.

OFDM is generally utilized multicarrier modulation technique in today’s portable mobile communication system. There have been a many architectures that have been presented to develop the performance of the OFDM system. Due to spectral leakages in OFDM based multicarrier modulation techniques this can be considered as not a suitable applicant for 5G and Cognitive Radio environment. Hence in this thesis, a novel FBMC transceiver architecture is presented for future communication system. The FBMC transceivers make utilization of Inverse Fast Fourier Transform and Fast Fourier Transform (IFFT/FFT) blocks along with polyphase filter banks. The compiled literature to design and implement an efficient transceiver for future communication system is covered in the following sections.

2.1 Multicarrier Modulation Technique
   2.1.1 OFDM (Orthogonal Frequency Division Multiplexing)
   2.1.2 FBMC (Filter Bank Multicarrier)
   2.1.3 FBMC v/s OFDM

2.2 FFT/IFFT Architectures

2.3 Polyphase Filtering Technique

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2.1 Multicarrier Modulation Techniques

Various multicarrier modulation techniques are utilized for present wireless communication system. Some of the dominant multicarrier modulation techniques and its literatures are described below.

2.1.1 Reported Work on Orthogonal Frequency Division Multiplexing (OFDM)

Robert W. Chang (1966) presented the concepts of orthogonal frequency division multiplexing for transmitting of various information through a band constrained transmission channel at greatest information rate without any interference. A guideline of orthogonal multiplexing is utilized for transmitting \((N \geq 2)\) Amplitude Modulated information through a direct band-restricted transmission medium. The channels work on same center frequencies and transmit information in synchronized manner. Each channel can transmit binary digits, M-ary digits, or real numbers. Inter channel and intersymbol interferences are eliminated by a new method of synthesizing the transmitting filter characteristics (i.e., designing band-limited orthogonal signals). The strategy presents one to combine an expansive class of transmitting channel attributes in an exceptionally advantageous way by integrating the phase and amplitude features independently.

The transmitting filter characteristics obtained in this method are:

(i) The amplitude characteristics may have gradual rolloffs, and the phase characteristics need not be linear.

(ii) The transmitting filters may be identically shaped and can be accomplished by uniform filter structures.

(iii) Permitting the use of a narrowband band pass filter at the input of each receiver to reject noise and signals outside the band helps in suppressing impulse noise and in preventing overloading the front ends of the receivers.

The method introduced in this paper utilizes band-constrained orthogonal instead of other non orthogonal multiplexing techniques.

Parallel quadrature AM transmission gives a technique for transmitting advanced information at speeds near the Nyquist rate of band restricted channels without utilizing sharp cutoff channels. Burton R. Saltzberg (1967) described implementation of parallel
quadrature amplitude modulation information transmission framework, with various overlapping channels, each conveying a signaling rate b, and signals are separated by b/2 distance. This transmission strategy accomplishes great execution at high data rates over band constrained dispersive transmission media. The two end channels will have significantly less contortion since crosstalk from just a single channel can exist. This impact is useful in utilizing a higher frequency range of transmission media.

Yu-Wei Lin et.al (2007) proposed a varying size Fast Fourier transform and Inverse Fast Fourier transform engines for the use of MIMO technique. These algorithms are based on the multipath delay feedback structure. Results and analysis shows that by adopting this approach for FFT /IFFT engines leads reduced hardware utilization and resources for DFT calculations.

OFDM baseband transceiver architecture developed by, Ryoji Hashimoto et.al (2009) for the purpose of spectrum access. OFDM transceiver architecture utilizes larger size FFT/IFFT engines to facilitate dynamic spectrum access. With the help of FFT processor, carrier sensing can be accomplished in desired way. A prototype system is constructed for the compatible use IEEE 802.11g wireless communication standers. The implementation results shows that this architecture utilizes lower area in terms of slice registers and logic gates.

M.A. Mohamed (2012) described the implementation aspects of orthogonal frequency multicarrier communication system. All the modules of OFDM are programmed by using hardware description language. This research work mainly focused towards SNR performance of OFDM system. The experimental result proves that after some frequency range, performance would not be affected for the abrupt SNR values.

Shaminder Kaur et al. (2012) presented the plan and execution of OFDM based transceiver architecture on a FPGA platform. It utilizes Radix-2 based 512-point FFT calculation that upgrades its throughput. The framework configuration is improved as far as both cost and speed. The developed OFDM has been implemented on Virtex-2Pro
based xc2vp30- 5ff896 target device using Xilinx ISE (10.1) tool. The results show that the developed OFDM can operate at maximum frequency of 227.355 MHZ by consuming very less number of resources to provide cost-effective and high performance solution for wireless communication applications.

Foisan Ahmed (2014) proposed the outline of a High Speed OFDM based transceiver architecture. The main execution block of the OFDM system is FFT and IFFT engines which are utilized for computational purpose. The eight- point FFT and IFFT with radix-2 calculation has been examined and used in the design. The outline has been recreated on the FPGA hardware platform. The simulation result of proposed architecture is same as that of MATLAB results, which is simulated using similar inputs.

James Chacko (2014) presented applications of OFDM in the field of wireless communication system. OFDM framework is composed by including various modules such as coder, decoder, channel identification etc. Each phase of OFDM framework can be arranged at configuration time or at runtime to oblige diverse wireless communication standards. This adaptability in device is accomplished by planning every individual stage with scaling/change. The general pipelined engine architecture is implemented in FPGA hardware. In future work, to reduce further end-to-end latency of OFDM system the input buffer sizes can be optimized within each stage.

Budi Setiyanto et.al (2014) outlined the hardware implementation of orthogonal frequency division multicarrier approach. Each module of the system is configured by utilizing VHDL code. The outcomes of this work demonstrate that the combinational circuit’s works too quick however requires excessive resources. The primary goal for future work includes obtaining enhanced accuracy using sequential circuits. With this, short range vehicle-to-vehicle communication is possible.

2.1.2 Reported Work on Filter Bank Multicarrier (FBMC)

Márius Caus et.al (2012) analyzed the digital modulation technique based on the filterbank multicarrier (FBMC) approach. The strategy of adding cyclic prefix in OFDM
system adds more complexity and degrades bandwidth efficiency. The work introduced in this research work gives understanding the concept of MIMO with the usage of FBMC technique. Simulation results prove that FBMC based MIMO technique has capability to overcome the limitations associated with previous MIMO technique.

Lajos Varga and Zsolt Kollár (2013) analyzed and presented overview of Filter Bank Multicarrier (FBMC) modulation technique for communication system. It introduced a novel, transmitter architecture for FPGA implementation. Transmitter architecture is configured by utilizing IFFT, polyphase filter and some computational blocks. A nearly less complexity architecture introduced to overcome the drawbacks of previous architecture. This can be considered as an augmentation of an OFDM transmitter with extra computational blocks.

Yonghong Zeng et.al (2013) designed the parallel algorithms and FBMC Systems based on Normalized prototype filter. The coefficients are pre-computed and stored in memory. The transmitter module here uses a parallel architecture which includes Fast Fourier Transformation (FFT). This achieves better performance over OFDM. Unified structure and Parallel algorithm is better than the conventional serial algorithms.

Esteban Gutiérrez et.al (2014) developed adaptable FBMC technique which is a replacement for existing OFDM technique. FBMC architecture is modeled usage of multirate signal processing to improve the productivity of transmitter and receiver. Strategy that has been adopted issues related to previous system and changes required for FBMC frameworks. At the end, the comparative analyses of different multicarrier modulation schemes are presented.

Vincent Berg et.al (2014) developed the FBMC transceiver architecture for exploiting immediate opportunities sensing of spectrum in television white space regions. A complexity analysis is performed with respect to OFDM system. The research work carried out in this paper under the grounds of filterbank multicarrier approach. Adaptable hardware architecture for radio spectrum access in the combination of filters and RF
environment was also presented. The hardware implementation result proves that proposed system has improvement in the flexibility and ACLR reduction. The complexity overhead presented by the FBMC technique is confined in terms of logic utilization compared to OFDM system.

Most application like Communications, Digital Radio, and Wireless Networks use relaxed synchronization for future generation communication system. To reduce signaling overhead in communication system A. S Kang et.al (2014) suggested non-orthogonal multicarrier waveforms. This technique is unconventional to OFDM technique. Hence, FBMC technique is a better approach and it is non-orthogonal multicarrier in nature.

Rajalekshmi Sanal et.al (2014) implemented End-to-End Latency Analysis of FBMC using FPGA. Here, composite of filters and O-QAM are utilized for the enhancement of transmission rate. FBMC Transmitter and Receiver are designed in Simulink System Generator. The VHDL code generated is used to synthesize in Xilinx ISE Design Suite 14.7 and latency is analyzed. The designed SoC architects strive to create FBMC architectures that deliver optimum latency for efficient applications compared to OFDM multicarrier system. This paper concluded that, polyphase implementation of FBMC can be done to reduce the latency since it requires less number of resources compared to OFDM but FBMC has more complexity overhead.

Jeremy Nadal et.al (2015) proposed FBMC transmitter architecture implementation with low complexity overhead compared to OFDM scheme. This transmitter is fit for supporting a fewer channel lengths with polyphase system structure. It depends on the utilization of IFFT engine along with polyphase network. The implementation and synthesis result show that proposed transmitter has considerable complexity reduction in the sense of hardware resources.

In many advanced communication systems, the best medium access technique is Power Line Communications (PLC) and also it is one of the multicarrier approaches. For PLC in FBMC system implementation, Pablo Poudereux et.al (2015) has used three different
architectures which are applied for polyphase filtering. By using different Filter forms, they analyzed quantization errors for both FBMC Transmitter and receiver.

Hyungju Nam, Moonchang Choi, et al (2016) presented FBMC system for transmitting and receiving of information without interferences. The proposed framework is produced with two distinctive channel banks. One channel bank is utilized for the even subcarrier and one more channel bank for the odd numbered subcarrier. The proposed system satisfies the suggested Orthogonality conditions. Numerical results of proposed system have two favorable circumstances against the conventional cyclic prefix based OFDM systems ie, spectral efficiency can be improved and intrinsic interference is reduced by removing cyclic prefix.

Chanhong Kim (2016) described the suitable multicarrier modulation techniques for 5G technology. This article describes features and implementation aspects of different waveform for future communication system. The execution assessment demonstrate that the proposed QAM-FBMC framework gives much lower range leakage and additionally improved performance against the CP-OFDM. Finally conclusion is given QAM-FBMC is better choice for 5G mobile communication.

2.1.3 Reported Work on FMBC v/s OFDM

Dirk S et.al (2006) described comparative analysis of diverse multicarrier modulation schemes. It described MDFT- based (modified DFT transmultiplexer) TMUX transmitter and OFDM based transmitter. MDFT-based (modified DFT transmultiplexer) TMUX transmitter is implemented using filter banks. The simulation results prove that MDFT TMUX-based transmitter has more appropriate than OFDM approach.

Y. Medjahdi et.al (2009) analyzed the performance comparison between cyclic prefix oriented OFDM technique and prototype filter oriented filter bank multicarrier scheme. In the existence of interference both the systems timing and phase attributes are evaluated. And also the average noise power of cyclic prefix oriented OFDM technique and prototype filter oriented filter bank techniques were presented. A performance assessment has shown that filter bank based multicarrier scheme present lower noise interference
compared to cyclic prefix oriented multicarrier scheme. This can be incorporated in future wireless communication system.

Bidyalaxmi Devi et.al (2014) presented the comparative analysis of multicarrier modulation techniques and its usages. For the pair compaction purpose they have considered three parameters such as error rate in the transmitted bit, transmitted signal versus noise ratio and data delivery ratio. Simulation and analytical results prove that FBMC system gives overall performance improvement in terms of BER and SNR compared to conventional OFDM system. By considering these parameters FBMC can be appraised as an ideal applicant for future wireless communication systems.

Tomas Gotthans, Roman Marsalek et.al (2015) presented experimental study and comparison of FBMC and OFDM signals distorted by real non-linear power amplifiers, and which have been tested and presented. The experiment was trying to give an answer whether the FBMC signals would keep their beneficial properties even as real non-linear power amplifiers were employed. In order to guarantee higher accuracy of presented results, three power amplifiers have been used. In this paper, it is experimentally proved that using FBMC signals, lower (adjacent channel power) ACP can be achieved. However, lower resistance than OFDM signals to non-linear distortions must be taken into the account. The results indicate that FBMC modulation can achieve better ACP than OFDM signals.

2.2 Reported Work on FFT/IFFT Architectures

In large areas of communication system, it is important to construct high speed FFT engines for computations of DFT of signals. Most of the FFT engines are modeled based on pipelined operation. VLSI usage has distinctive requirements which change from those of discrete time domain to frequency domain signals. Therefore requirement of diverse FFT engines are very essential in the field of wireless communication.

Fast Fourier and Inverse Fourier transform are the well known algorithms utilized for computation of DFT of signals in efficient manner. These algorithms were introduced by
Cooley-Tukey (1965) to enhance the computational speed of conventional methods. The main cause of utilizing FFT/IFFT engines in communication system is to reduce the number of computations needed.

Erling H. Wold et.al (1984) implemented the Pipeline architectures for the Cooley-Tukey technique. This paper proposed pipelined FFT architecture which requires less hardware compared to Winograd technique. These forms are appropriate for use in VLSI executions because of the productive utilization of chip I/O data transfer and simple steps in FFT calculations.

S Sukhsawas et.al (2004) described the hardware execution of efficient pipelined FFT technique on FPGA platform. It consumes the less number of the multipliers and storage. They selected language for implementation is Handel-C. They are designed 1024-point FFT with input 16-bit and same Twiddle factors length. The outlined architecture is tangible for varying input and Twiddle factors. The design is reconfigurable for 8-point, 16-point, and 256-point till 1024-point also the design of debugging and verification is also simple.

Mian Sijjad Minallah et.al (2006) discussed about the implementation aspects of a 64 point FFT Processor in FPGA. This device can be used spectrum estimation and measurement applications. The architecture mainly consists of DRAM, ROM, controller, address generator unit and processing unit. The overall design is synthesized and implemented on FPGA.

Ahmed Saeed (2009) presented the plan and execution of Radix2² based FFT/IFFT engines. The entire module is configured by using VHDL code and operation checked with the help of ModelSim. Results demonstrate that the processor accomplishes higher throughput and lower delay compared to earlier processors.

K.Harikrishna, T.RamaRao (2011) developed compatible FFT algorithm to enhance the execution speed & efficiency of OFDM system. The developed OFDM architecture is
suitable for wireless communication standard devices such as WiMAX, IEEE802.11 etc. The architecture is configured by utilizing Verilog code. The results proves that speed of proposed configuration effortlessly fulfill most of the wireless communication applications. Also, the proposed design occupies lesser area in terms of logic gates with low power consumption.

Yousri Ouerhani et.al (2013) proposed implementation of optimized FFT algorithms for low-cost FPGA. In this paper, they utilized short length structures of FFT in order to obtain higher length transforms. To develop the VLSI architecture, two techniques are suggested for the implementation purpose. Implementation results proves that lesser area oriented FFT processors exhibits better performance compared to higher order FFT. The enhancement of this architecture in future is towards optimization of computational blocks and utilization of embedded multipliers for multiplication.

2.3 Reported Work on Polyphase Filtering Technique

In the applications of wired and wireless data transmission, multirate digital filters are widely used for the purpose of data compression and data processing. P Vaidyanathan (1990) presented usage of decimation and interpolation filters in multicarrier communication system. And also described the detailed structure and working principle of analysis and synthesis filter banks. The basic concepts of polyphase representation and implementation aspects were also reviewed. Research studies also elaborated subband coding of waveforms in presence of noise.

H. I. Saleh et.al (2002) proposed a multistage single frequency low pass filter with two path polyphase multiband filter. A dual channel framework is described on FPGA hardware platform. The polyphase multiband filter includes various filter stages. The implementation of a one channel FM filter consumes more area compared to two channel filter system. The usage of a one FM channel requires larger area compared to two channel filter system. The conclusion of this work is that, proposed multistage Low pass channel offers the most productivity.

M. A. Ashour et.al (2002) presented systematic design of polyphase architecture by the utilization of half and multi band decimated filters. The implementation of the two
channel system using poly phase Multiband Filters gives overall 2% reduction in area on FPGA.

A multichannel digital receiver continuously down converts high frequency data content into lower data streams. To accomplish these tasks efficiently, polyphase filter bank architecture is the best choice. Fredric J. Harris et.al (2003) presented basic polyphase structure which includes prototype filter. The proposed system acknowledges efficient data conversion mechanism for the purpose of data compression and transmission. The result shows that a multichannel polyphase filter bank has more performance compared to single channel communication system.

LiuQing et.al (2007) proposed a novel system for high speed data conversion for the usage of wireless communication applications. This device includes various modules for the specific usage of signal processing applications. Results of proposed architecture demonstrate that lesser operations needed for efficient data conversion mechanism compared to earlier mechanisms.

Noura Ben, Ameur Maher Soyah et.al (2009) presented efficient implementation of multistage filter bank based on delta sigma audio DAC mechanism. The design based on the polyphase structure for range of 1 to 128 interpolator linear phase filter scheme strategy. The architecture also incorporated subband filters at each stage of interpolation. At the end obtained optimized area to meet the constraints of delta sigma audio DAC applications.

The decimation and interpolation filters are also called as Multirate filters. These are the essential blocks of digital signal processors for the down and up sampling of digital data. Jason Xin Zheng et.al (2010) described multi stage filter design architecture with the utilization of decimator, interpolator, and finite impulse response filters. The multi stage filter design architecture provides higher throughput compared to single-stage designs. The FPGA implementation results can be optimized for required manner to accomplish less resource utilization.
Mehmood Awan et.al (2010) analyzed different implementation structures for multirate filter bank. The multirate filter structure includes square root shaping filter and various processing blocks for computational purpose. Presented different design structures for FFT/IFFT modules based on Radix-2 algorithm. Different design techniques were described for filter bank channel mapping and up and down sampling of digital data. Based on the above concepts they accomplished better utilization of area, time and speed.

Suhaib A. Fahmy et.al (2010) implemented system for spectrum sensing based on reconfigurable polyphase Filter Bank architecture. They also discussed the usage of proposed technique with respect to earlier spectrum estimation approaches. The polyphase filter bank approach exploits usage of advanced multipliers on recent FPGA hardware. This architecture allows use of single filter structure for each sub-band in successive clock cycles. Thus it can have the same computational resources for each subband with reduced sample rate. This architecture can also be scaled for the requirement of specific spectrum sensing purpose. Finally reconfigurable feature of this structure can be adopted for cognitive radio applications.

Polyphase filterbank approach is one of the eminent techniques to reduce the clock frequency of DSP and FPGA hardware. This can be achieved with the help of multirate filter structure and FFT engines. A.Melis (2011) outlined the architecture of polyphase filter bank structure with overlapping bands to overcome the problem of the holes between adjacent subbands. A particular spectrometer composed of two-stage PFB has been implemented on a FPGA hardware that is contained into theCore2 boards of the Digital Base Band Converter (DBBC). The overall system will be part of a scanning FFT spectrometer in which the flat parts of each band are achieved automatically avoiding waste of resource.

Xiaohong Huang et.al (2012) described about polyphase filter bank structure and its FPGA implementation. They are improving the basic multi sampling concept to get the polyphase filter design. This design improves the computation speed of the filter. They use direct structure FIR filters to fulfill filter’s hardware realization. The multi
dimensional architecture of discrete Fourier transforms has been designed using synthesis and analysis filter structure. Finally, reconstruction procedure were adopted for both synthesis and analysis module. The results prove that, this architecture achieves more computation speed and improves the operating speed of the DFT filter bank.

This document (XAPP1161 (v1.0) March 20, 2013) exhibits how to utilize the Xilinx FIR Compiler IP center in conjunction with the Xilinx FFT center to plan and execute a polyphase channel bank. This application note presents the polyphase channel bank and gives three usages of the transmitter and receiver architectures.

Fernando Cruz–Roldán et.al (2011) presented novel technique for performing multicarrier modulation (MCM) in wireless communication system. This approach works on the algorithmic procedures of IFFT/FFT engines. The transmultiplexer system facilitates simple equalization of the transmission channel with the utilization of cyclic prefix and IFFT/FFT module. To develop multicarrier based modulation technique in digital communication standards, IFFT/FFT are utilized at transmitter/receiver side respectively. With this technique, better spectrum segregation can be achieved across each subband. And also robustness and lower bit error probability can be accomplished.

In wireless communication applications Multirate filtering method is broadly utilized for various applications and it is a capable in DSP, which brings about ease executions of subband processing mechanism. Multirate filtering approach minimizes the execution procedure by incorporating parallel mechanism in communication system. Gopal S.Gawande et.al (2016) presented the efficient multirate filter bank architecture for the development of polyphase structure. The outlined algorithm is adopted for polyphase structure and it influences on reduction of power. The fundamental target of of this architecture is to minimize power consumption in the hardware platform.

2.4 Summary

Literature review was done on various multicarrier modulation techniques and suitable transceiver architecture implementation for future communication system. Literature survey identified that OFDM and FBMC differ with respect to their suitability for various
applications. It is noted that OFDM is a perfect choice for many applications whereas FBMC may be alternative choice for other applications. For applications like cognitive radios, digital subscriber lines, power line communications and the uplink of multiuser multicarrier systems FBMC is ideal choice compared to OFDM. It was also noted that in the design of FBMC frameworks in light of polyphase channels, the range of each subcarrier can be confined inside a restricted transmission bandwidth. Since the primary polyphase structures will be based on smaller size IFFT/FFT blocks the complexity of both transmitter and receiver will be reduced. Hence, a best FBMC transceiver can be designed and implemented by considering following factors.

- Using smaller size pipelined IFFT/FFT engines for transceiver implementations in an FPGA to improve the execution speed, hardware design effort, system cost, and flexibility.
- To reduce the system latency and increase throughput by implementing polyphase filters with IFFT/FFT. Due to polyphase structure, corresponding group delay of the filters is reduced.