Chapter 2

Literature survey

2.1 Introduction

This chapter peeps into the extensive literature survey that has been done for this research work. The purpose and the advent of MLI are discussed and the evolution of classical topologies of MLI, their merits and demerits are also discussed. The modern topologies, most of which are either partial or full hybrid of classical topologies are discussed. Their power ranges and areas of applications of these topologies are discussed. The modulation strategies which are mostly extension of that used two-level inverter are discussed. The only PWM technique, which stands out unique for MLI, is SVPWM which is discussed in detail. Then capacitor-balancing techniques for 3L-NPC and 5L-DCMLI are discussed. Most of the balancing techniques for 3L-NPC fall under Inherent-balancing technique, while that of 5L-DCMLI fall under source-side balancing techniques as inherent techniques did not give good result for 5L-DCMLI.

2.2 Topologies

2.2.1 Classical Topologies

Improvement in energy efficiency, reliability and flexibility at medium-high power levels is a potential area to conserve energy, economy and automate industrial process [11][12]. MLI have contributed a great deal in this area, they have been prime focus of research for past 3 decades. Many academicians, scientists and industrialists have tested with the best of their abilities to up bring this technology. Several
topologies, control techniques and modulation techniques have been developed and still the research is ON in overcoming limitations of existing technology.

The era of MLI started in late 60s where multi-stepped converter was realized using series connection of H-Bridge converters proposed in [13], which are now popularly called as, cascaded H-Bridge (CHB) converters shown in Fig. 2.1c. Later in the same year [14] low power flying capacitor (FC) converter was developed shown in Fig. 2.1b. In early 80s 3L-Diode clamped converter popularly called 3L-Neutral point clamped converter(3L-NPC) was developed [15]-[16] shown in Fig. 2.1a.

The 3L-NPC was first introduced by Nabae in 1981 [17] the authors proposed a new breed of inverters called NPC-PWM inverter which later on became popular as NPC-MLI. It has been introduced with the moto of overcoming the drawbacks of conventional two-level inverter. The conventional two-level Inverters which introduce lot of harmonics into AC motor drive cause losses and increase the torque ripple. Later on with the advent of PWM techniques, the harmonics induced into the motor drives have been reduced which in turn reduce the losses. But the increased switching frequency has led to high switching stress, switching losses and electromagnetic interference effect. Authors have proposed a modified selective harmonic elimination technique to eliminate all the harmonics below 13th order. It has been proved that the proposed inverter can provide high power with lower torque pulsation and higher drive efficiency compared to conventional two-level inverter.

However, it was only in late 90s [18] that technology has matured enough to make it realize for an industrial application. The CHB and FC converters have
Table 2.1: Comparing commercial classical multilevel inverter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>3L – NPC</th>
<th>CHB</th>
<th>4L – FC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum power</td>
<td>27MW, 31.5MVA,</td>
<td>120MW,</td>
<td>22.4MW</td>
</tr>
<tr>
<td></td>
<td>40MVA, 44MW,</td>
<td>15MW, 11.1MVA,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33.6MW, 3.7MW</td>
<td>6250kVA</td>
<td></td>
</tr>
<tr>
<td>Output voltage (kV)</td>
<td>2.3/3.3/4.0/4.16,</td>
<td>2.3-13.8, 3.3/6.6,</td>
<td>2.3/3.3/4.16</td>
</tr>
<tr>
<td></td>
<td>2.3/3.3/4.16,</td>
<td>3/3.3/4.16/6/6.6/10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3/6.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Modulation method</td>
<td>PWM, SHE, SVM</td>
<td>PS-PWM</td>
<td>PS-PWM</td>
</tr>
<tr>
<td>Cooling system</td>
<td>air/water, water,</td>
<td>air/water, air</td>
<td>air</td>
</tr>
<tr>
<td></td>
<td>air</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Semiconductor devise</td>
<td>IGCT, MV/HV-IGBT,</td>
<td>LV-IGBT</td>
<td>MV-IGBT</td>
</tr>
<tr>
<td></td>
<td>IEGT</td>
<td></td>
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</table>

the advantage of modularity or then called multi-cell structure [19]. But these structures have their own limitations that they couldn't compete with 3L-NPC converter. CHB converter requires multiple separate regulated DC source for each cell, which was realized using phase shifting transformers or DC-DC converters at the source side. The phase-shifting transformers made the circuit bulky and costly, but this transformer could also be used to improve the power quality. Similarly usage of DC-DC converters adds to the cost and complexity of the circuit. Thereby CHB converters were used where stiff power quality regulations were imposed. FC converters used more no. of capacitors, there by their packaging becomes very difficult and apart from this, the pre-charging of capacitors is also a tedious process which makes their usage impractical. It was 3L-NPC which gained lot of prominence in many applications as it uses a simple rectifier transformer combination with less no. of capacitors and device count. But these converters faced capacitor voltage imbalance problem which has led to low frequency oscillation at the neutral point [20][21]. Keeping in view the potential applications of this converter, extensive research has been done to overcome capacitor imbalance problem which will be discussed in the section II.

For levels higher than 3, the name NPC cannot be used for DCMLI as it has
multiple junctions clamped rather than just neutral point being clamped for three-level. Due to increased no. of junctions and capacitors, the control over balance in capacitor voltage using modulation techniques or with passive front end has become very difficult \cite{22}. Hence active source-side control like separate DC source or Back to Back rectifier inverter connections were employed. Apart from this, they have unequal loss distribution among the switches due to difference in conduction duration and the clamping diodes which are used in series to block the voltage, pose reverse recovery current during turning off which increases the switching loss \cite{23}-\cite{24}. Despite its advantages like less component count, all the aforementioned drawbacks have limited the application of DCMLI beyond three-level.

For higher power levels CHB has become popular due to its modular structure the switching stress is less. Thereby conventional semiconductor devices like LV IGBT could be used. The increase in levels reduce the switching frequency as good harmonic profile is obtained at lower switching frequency \( (m - 1) \times m_f \). The average switching frequency \((< 500Hz)\) which reduces the switching loss thereby can be air-cooled. But the problem with CHB is the requirement of separate DC sources which have to be fed by more costly and bulky phase shifting transformers than conventional transformer used for NPC \cite{22}.

Even though FC converter is modular in structure for higher levels, it needs more no. of capacitors and maintaining balance among these capacitors is a very complex control task and their package is also very difficult. Thereby, these converters couldn’t advance in the market. The commercial ratings and specifications of the classical topologies are shown in Table 2.1.

### 2.2.2 Modern Topologies

In the last section it has been discussed at length the merits and demerits of conventional MLI topologies. It has been identified that 3L-NPC was popularly accepted in many applications. But when it comes to converters beyond three-level, none of the converter could really penetrate the market due to one or the other drawback. This has been the point of research for the last decade. \cite{3} focuses on providing a new way to classify all the available MLI. The author discusses the evolution of different MLI and their areas of applications, merits and demerits of various configurations of MLI. The author concludes that the future scenario of research for medium voltage MLI would be based on combination of FLC, NPC, Active Neutral
Figure 2.2: Five-level H-bridge NPC

point clamped converter (ANPC) converters for medium voltage applications and for high voltage MLI the challenge would be to reduce both volume and weight of passive components.

Many new topologies, most of which are either full or partial hybrid of conventional MLI topologies have been proposed [13]. The inverters which have gained practical significance will only be discussed. Amongst are the modern topologies five-level H-Bridge NPC (5L-HNPC), the three-level Active NPC (3L-ANPC), five-level ANPC, the Modular Multilevel converter (MMC) and the Cascaded Matrix Converter (CMC). These popular converters will be discussed in the subsequent sections.

**Five-level H-Bridge NPC (5L-HNPC)**

It is a H-Bridge connection of two 3L-NPC legs as shown in Fig. 2.2, the schematic of single phase of such inverter. It was first introduced in [25], this configuration can be used to realize five-levels and individual phase being 3L-NPC the modulation techniques developed to balance capacitor voltage for 3L-NPC can be applied effectively [26]-[27]. From source side point of view, it is similar to CHB i.e. it requires separate isolation transformer supplied from a 36 pulse diode rectifier for each phase, if not isolated, there is a chance of short circuit. This converter generates five-levels of output with a slight balance in improvement of both CHB and DCMLI. From source-side perspective, it reduces the no. of sources but still it has to employ three different sources i.e. three phase shifted transformers, three 36 pulse diode bridge
rectifiers. This makes the circuit complex and costly, even though it comes with an advantage of improving source power quality [18]. From circuit point view when it is compared with five-level CHB it employs same no of components except extra 12 diodes. In addition the control logic becomes complex as it has to ensure to balance capacitors similar to 3l-NPC. These converters are practically employed in converters of power range 2 to 7 MW with air cooling and 5 to 22MW with water cooling [20, 28].

Three-level Active NPC (3L-ANPC)

The classical 3L-NPC although is very popularly used in many applications. It has a draw-back of uneven loss distribution among the switches. This requires a special design of heat sinks to moderate the junction temperature difference among the switches. This special design of heat sink limits the maximum power rating, output current and switching frequency of the converter [29, 30]. To overcome this problem, the clamping diode of classical NPC has been replaced with an active switch and such topology is called 3L-Active NPC(3L-ANPC) the schematic of which is shown in Fig. 2.3a. In 3L-NPC the current free wheels through upper or lower diode based on the polarity of the current during a zero level. But with the usage of active clamping switch, the current can be forced to be directed in a desired manner so that the loss distribution among the switches becomes uniform. This modification has improved the power levels of the converter and the additional switches used are called active clamping switches thereby the name 3L-ANPC [31]. It is designed to cater 20 to 200MVA power range applications and can be connected to a 6kV to
220kV grid with a transformer[20].

**Five-level Active NPC (5L-ANPC)**

As an extension to 3L-ANPC a new topology, which is a hybrid of 3L-ANPC and 3L-FC have been developed schematic of which is shown in Fig. 2.3b. This converter can produce 5 levels($V_{dc}/2, V_{dc}/4, 0$). Unlike 5L-DCMLI, this converter has modularity and as this converter uses only 3L-NPC supply DC capacitors can also be balanced[32]-[33]. But the problem with this converter is the complexity in topology and the control. It needs to control both source side capacitors and flying capacitors as well; apart from this the pre-charging of flying capacitors is also a problem. Unlike CHB topology, the increase in level of this converter doesn't come with increase in power level, The FC structure added only adds inner voltage levels and hence it improve the power quality but not the power levels[34]. The product available in the market is of medium voltage and power levels rated at 6 to 6.9kV and 0.4 to 1MVA. The modified version to this converter is the inclusion of common cross converters (CCC) [35]. On selecting the CCC capacitor to be $V_{dc}/8$, the ratio of ANPC dc link voltage to FC voltage to CCC voltage will be $V_{dc}/2 : V_{dc}/4 : V_{dc}/8=1:0.5:0.25$, 9 different levels of output voltage[36]. As the no. of stages of CCC increases, the power quality also increases but it comes at the cost of increased complexity and the necessity to balance source-side capacitors, FC-Capacitors and CCC capacitors make control very complex[36]. Even in this case, the no. of levels increases but the power range remains the same. But compared to CHB, it uses fewer components to produce similar power quality. It uses single DC source with a much simpler transformer rectifier system.
Modular Multilevel Converter (MMC)

It is a recent origin; this topology is an interconnection of no. of two-level half bridge converter which is treated as a cell as shown in Fig. 2.5 [37]. There will be even no. of cells in a leg which are equally distributed to produce positive and negative half cycles and these cells are separated by inductors so to avoid short circuit during transitions. These converters are found being applied in industry especially in HVDC system [38]-[39]. The main advantage of this converter is its modularity and its scalability to reach any power level. This topology was reported to be implemented in 400MW application with 200 power cells [40] and is commercialized up to 1GW [41].

Multilevel Matrix converters

Matrix converters which are direct ac-ac converters have been in research for long time, but weren't able to establish in the market due to no. of switches used, complexity in control, low conversion factor and chance of short circuit between the phases. The idea of matrix converter is to avoid the intermediate energy storage stage that exists in DC link AC-AC conversion. This reduces the weight/volume ratio with inherent four quadrant operation. Such conversion finds many applications in electro-mobility (electric vehicles, aircraft systems). Without presence of energy storage devices, its difficult to split the supply into various voltage levels. This is why this topology is limited to narrow application scope. However many multilevel matrix converter topologies using conventional MLI were proposed [42]-[43]. Among
them, only cascaded multilevel matrix converters have gained some practical significance [44].

Other popular topologies

Open ended winding induction motor drives where two inverters are used to supply stator and rotor windings separately [45]. This connection gives the possibility of multiple voltage levels being applied to motor [46]. Initially two 3L-NPC converters were used to supply, later on this has been extended to many other combinations of converters [47]-[48]. The other hybrid which has gained prominence is NPC-CHB multilevel converter where the output of 3L-NPC is connected to no of series connected CHB cells as the capacitors are floating the CHB part of converter can only increase the levels but not the power levels [49][50]. The other possibility was based on duality principle if VSC exists than multilevel current source converters should also exist many topologies [51]. The underlining principle was connection of capacitors voltages to stepped shunt connection of inductor currents. These converters improve the current quality and large current supplying capability; thereby they find applications in current sensitive loads [52].

2.3 Modulation Techniques

As discussed in the previous section extensive work has been done in developing new topologies of MLI. The focus wasn’t shown in exploring modulation techniques as most of the modulation techniques are simple extension of existing technique for two-level inverter. The conventional sine PWM technique has been applied in different variants like level shifted (LS) carrier PWM technique, phase shifted (PS) carrier PWM technique. In either of these techniques (m-1) carriers are used and the harmonics are shifted to side bands of \((m-1) * m_f\) [53][54]. Thereby at lower frequencies good harmonic profile is obtained. Phase Disposition (PD) is quite suitable for CHB as all the H-bridges are equally utilized [55][56].

The other technique popularly applied is Selective harmonic elimination technique (SHE) [57][58]. In this technique the level transitions take place at specific angles, these are calculated by equating Fourier component of the harmonic to be eliminated. In this way switching frequency reduces thereby switching losses and makes the converter more efficient. The angles are calculated off-line and stored as
lookup table in PROM. This PWM technique cannot be applied to closed loop control as an error sensed any feedback sensor would lead error in the output produced by the inverter. An extension to this technique is Selective harmonic norms.

The PWM technique which gives multiple degrees of freedom to control MLI is Space vector PWM (SVPWM). This technique explores the multiple switching states possible in MLI \[26\][59].

### 2.4 Capacitor balancing techniques

#### 2.4.1 Introduction

In the previous sections, it has been discussed at length about various popular MLI topologies. It has been identified that the classical DCMLI although is very popular for medium power applications in its three-level form as 3L-NPC, but for higher levels the problem of capacitor imbalance aggravates. This section discusses various techniques proposed to balance the capacitor voltages of three-level and five-level DCMLI. These techniques can be broadly classified as below:

a. Inherent control techniques
b. Source-side control techniques

#### 2.4.2 Inherent Control Techniques

These techniques do not use any extra components for balancing the capacitor voltages. They enhance the modulation techniques applied to the respective converter to balance the capacitor voltages. These techniques can further be classified as:

a. Carrier based PWM techniques (CBPWM)
b. Space Vector PWM techniques (SVPWM)
c. Hybrid PWM techniques (HPWM)

**Carrier based PWM techniques (CBPWM)**

The carrier based PWM applied to 3L-NPC leads to 3 modes of operation namely dipolar, partial dipolar and unipolar modulation modes.

The schematic for generating control pulses through CBPWM for 3L-NPC is shown in Fig. [2.6]. Using the reference voltages \(V_{x}^{*}\) (x = a, b, c) put in by a load, two auxiliary commands \(V_{xp}^{*}\) and \(V_{xn}^{*}\) are derived to control the complementary pairs of
switches 1, 3 and 2, 4. To increase the range of under modulation, a third harmonic voltage $V_{TH}$ is injected into the reference voltage. The value of the bias term $B$ relative to the peak value $V_p$ of the commanded voltages determines the modulation mode dipolar ($0.5 > B > A/2$), partial dipolar ($B < V_p/2$), and unipolar ($B = 0$). In dipolar mode all the 3 levels (P, O, N) are produced in every switching cycle. This involves both the capacitors; thereby balancing capacitors in this mode is easy. In partial dipolar for a given reference half cycle there are certain switching cycles where all the three levels are produced and rest where only two levels are produced. In unipolar mode in a single half cycle of reference only two-levels of output voltage i.e. P, O are produced and in the other half cycle N, O levels are produced. In this mode the output voltage magnitude and switching frequency are high compared to dipolar. Unipolar mode involves only single capacitor at a time thereby it is difficult to balance the capacitor voltages.

Most of the carrier based PWM schemes proposed to balance capacitor voltages are based on the concept of adding zero sequence components to the reference \[60\]. Different CBPWM schemes differ in the way the dc-offset is determined and added. Usage of carrier based PWM for balancing capacitor voltages was first proposed by \[61\]. It could balance the capacitor voltages in dipolar mode only. Later observing this limitation, the authors \[62\] have provided correction for all the modulation modes. But in this technique as the modulation index increases after certain range, the compensation reaches saturation if it is increased beyond this value, the output
approaches 2-level thereby increasing the stress on the switches and capacitors. However authors in [62] failed to explain how neutral power flow is determined, does it require extra sensors and voltage balancing is limited in this scheme especially at high modulation index. To overcome the draw backs of previous scheme the authors [60] have developed a redundant state selection (RSS) table using which the polarity of the off-set F to be added can be determined as from the polarity of neutral voltage and phase current. Unlike the previous cases [63] and [64] where the polarity of off-set to be added was decided based on instantaneous power flow between inverter and motor which requires extra measuring devices. Besides the motor currents, they require the knowledge of motor current pf. In [60] authors have used currents fed by inverter to motor as they are anyhow measured for motor, control loop, It doesn't add to extra measuring components. Based on the sector in which reference is present, a correlation is established between phase currents and neutral current. This technique is effective but still has a limitation on modulation index, which can be applied. The technique proposed [60] needs to be operated at high switching frequency thereby adding to increased switching loss.

**Space Vector PWM techniques (SVPWM)**

The basic concept in utilizing SVPWM technique is to utilize the redundant vectors. The vectors which produce same voltage but induce current into the junction in opposite directions to each other are so as to charge the undercharged capacitor and discharge the overcharged capacitor thereby maintaining the balance. It can be observed from Fig. 1.2 the small vectors POO and ONN are redundant in nature, on applying POO current flows into the neutral point i.e. $i_n$ is -ve and on applying ONN current leaves the neutral point making $i_n$ +ve. [65]. The first attempt to solve the problem using SVPWM came as near three vector (NTV) strategy. This was proposed simultaneous in two different publications [66, 67]. These publications have identified the effect of small redundant vectors in a sector on neutral current are opposite. Thereby their proposal is to utilize these vectors for equal duration of time in a sector so that capacitors get balanced, similar analysis was also proposed in [68]. The authors doesn't mention anything about the duty calculation of these small vectors. In parallel times research was also rampant in CBPWM technique. The authors of [69] have proposed addition of common mode off-set voltage to reference to balance the capacitor voltages [69]. Later it was [66] who correlated the
CBPWM and SVPWM techniques for balancing capacitor voltages and proposed that addition of dc-offset has similar effect as modulating the redundant state. It also suggests that the duty of redundant doesn’t have to be fixed, and proposes a method to calculate the duty of redundant small vectors based on load conditions. The zero-sequence component gives rise to 3 times the fundamental frequency ripple at neutral point. Right after has proposed hysteresis control technique, As per this technique the duty of the redundant state is varied based the hysteresis limits of neutral point voltage to balance the capacitor voltages. A common conclusion from SVPWM publications was that equal duty of redundant small vectors in a particular sector is only going to counterfeit the unbalance caused due to small vectors but couldn’t suffice the effect of medium vectors. In hysteresis control only one of the redundant states of the controllable small vector is switched depending on the value of $V_n$. This was the simplest of implementations. Some authors have used P/PI controller to determine the duty cycle split but the procedure for determining gain has become quite cumbersome. Later the gain calculations focused on mathematically modelling the neutral currents and selecting the gain such that the average neutral current approaches zero ($I_n = 0$). The implementations differed in non-minimal switching transitions, synchronous optimal SVM. Despite all these efforts the neutral point control schemes using redundant states, fail at high modulation index and low pf angles. At high modulation index the effect of small redundant vectors is minimal and the effect of medium vectors on capacitor voltage imbalance dominates. proposes a new space-vector PWM technique based on current space vector d-q theory. The novelty is to identify the uncontrollable and controllable components of neutral point current, based on the particular space vectors that affect the neutral point voltage i.e. small and medium vectors. This neutral current is expressed as function of load current which would be split into d-q components and can be controlled. Higher $i_d$ indicates more chances of controlling neutral point voltage and higher $i_q$ indicates lower chances of controlling neutral point voltage. It further classifies the NTV (near three vector) SVPWM techniques proposed in the literature for neutral point voltage balance into passive, hysteresis and active. It concludes that passive techniques fail to balance the capacitor voltages for unbalanced loads and they are applicable for strictly balanced SVPWM which is practically not possible. On the other hand, hysteresis SVPWM techniques are very affective but introduce a current ripple at half the switching frequency. While active SVPWM techniques perfectly balance the capacitor voltage, they increase the
switching losses of the system. In [78] the authors have suggested equal split of duties between the redundant states. This strategy was termed as center space vector PWM and is shown in Fig. 2.7 how the addition of non-linear common mode signal to the original 3-phase references produce the CVSVPWM references [79]. CVSVPWM performs similar to zero sequence added reference CBPWM. These works prove that CBPWM/CVSVPWM only differ in terms of duty cycle split between two vectors.

In [78] it was proposed to split the duty of the redundant states equally or in other words centering the intermediate vectors to obtain better harmonic profile. This technique is termed as centered space vector PWM (CSVPWM). The feed forward technique proposed doesn’t compensate the neutral point oscillation but reduces the distortion in the output. These techniques strike balance between capacitor sizing and switch voltage rating [80, 81].

The limitation on NP balance using redundant small vectors is due to medium vector. This exceeds its limit if the duty of medium vector is more than small vectors. In order to tackle this [82, 83] have eliminated medium vector and the modified Space vector diagram of sector-1 is shown in Fig. 2.8.

The same idea was visualized in a different way by [84] introducing a concept called virtual vectors, that do not exist. The popular among these virtual vector techniques is proposed by [85] called Nearest Three Virtual Vector (NTVV) which
Figure 2.8: SV diagram illustrating elimination of medium vector in sector 1

Figure 2.9: SV diagram illustrating nearest three virtual vectors in sector-1
Table 2.2: Virtual vector realization in terms of real vectors for sector-1

<table>
<thead>
<tr>
<th>Virtualvector</th>
<th>Actualstates</th>
<th>NPcurrent</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{virtsmall1}$</td>
<td>$\frac{V_{211}}{3} + \frac{V_{110}}{3}$</td>
<td>$-\frac{I_A}{2} + \frac{I_A}{3} = 0$</td>
</tr>
<tr>
<td>$V_{virtsmall2}$</td>
<td>$\frac{V_{221}}{3} + \frac{V_{110}}{3}$</td>
<td>$\frac{I_C}{2} - \frac{I_C}{3} = 0$</td>
</tr>
<tr>
<td>$V_{virtsmall3}$</td>
<td>$\frac{V_{100}}{3} + \frac{V_{210}}{3} + \frac{V_{221}}{3}$</td>
<td>$\frac{I_A}{3} + \frac{I_B}{3} + \frac{I_C}{3} = 0$</td>
</tr>
</tbody>
</table>

is extended as a PWM technique by [86]. As shown in the Fig. 2.9 and Table 2.2, the virtual vectors are selected as function of real vectors upon switching these combinations results in zero neutral current. It guarantees zero neutral current for all load conditions including non-linear loads. Thereby these techniques minimize the size of capacitors. However an unbalanced capacitor operation will be preserved, which makes it essential to employ a NP balancing algorithm. [87] has developed an optimal control algorithm. To improve THD [88][89] has developed optimized NTVV(ONTVV) PWM. ONTVV has reduced THD with increased switching loss.

Hybrid PWM techniques (HPWM)

Hybrid modulation strategies were introduced with an idea of extracting the best features of the two existing techniques. An example would be to use conventional SVPWM in the region where it can control the NP for its superior THD output equality. When it is an undesirable load condition i.e. high modulation depths and low load power factor angles, NTVV is used [90]. In [91] a well CBPWM which is a NV strategy combined with non-NV strategy, implemented as carrier-based PWM with two carrier wave forms. A variable D which control the duty for which NV CBPWM is applied and is controlled. It is important to note that unless D=0, NP voltage ripple appears at the dc link.

A different approach was proposed in [82] which is a combination of both NTV and non-NV strategy is proposed. In this technique hysteresis of neutral voltage $V_n$ is taken as the limit to shift between the two techniques. Even this technique has a neutral point voltage oscillation within the set hysteresis limits. Any ambitious effort in making $V_n = 0$ will require to set the hysteresis band to zero thereby enabling the modulation to have frequent shifts between both the techniques and hence increased switching losses.
Orfanoudakis 2013 [92] deals with application of near vector (NV) and non near vector (NNV) PWM strategies. The technique is designed in such a way that the application of NNV PWM is minimized so that the losses get reduced and efficiency improves. To achieve this, authors have divided the neutral point current ($i_{np}$) into range called $i_{nphi}$ and $i_{nplo}$. It has been identified that if $i_{nphi} > 0$ and $i_{nplo} < 0$ it becomes controllable range and $i_{np}$ can be made zero with NV PWM. If it goes beyond this range NNV PWM strategy will be applied. At near to zero pf 100% NNV strategy will be applied and there will not be any difference with existing NNV techniques. But for less reactive loads both the strategies will be conditionally applied and it reduces losses thereby improving efficiency. This method is complex and incurs extra cost in implementation as it has to switch between two techniques.

### 2.4.3 Source side balancing technique

In these techniques, extra elements are added to balance the capacitor voltages. For levels higher than three-level DCMLI, it was observed that it is becoming very difficult to balance the capacitor voltages using modulation techniques. Thereby extra components were used to balance capacitor voltages. These techniques, even though they increase the cost, they were found effective. This section will be dealing with popular techniques in this category.
Back to Back converters

The capacitors of a 5L-DCMLI can be compensated by back-back connection of two such converters as shown in Fig. 2.10. The converter connected to the source side acts like a rectifier and the one connected to the load acts as an inverter. The capacitor junctions are interconnected and this interconnection provides a path for over discharging inner capacitors a path to charge. This happens because the rectifier will have a component of line current which is in phase with the voltage and thereby provide a charging path for the capacitors.

The authors of [93] have proposed to balance the capacitor voltages with optimized converter efficiency. The authors want to prove here that the total energy of a capacitor bank, composed of $n$ equal capacitances $C$ and characterized by a constant dc-link voltage $V_{dc}$ assumes its constrained minimum exactly when all capacitor voltages are equal i.e. balanced. They have developed equations for the energy stored in the capacitor bank in terms of rectifier and inverter modulation index. These equations when solved to get minimum energy for rectifier and inverter modulation index will automatically balance capacitor voltages. The other technique proposed to balance capacitor voltages was by [94] where two five-level inverters were used to supply induction motor in open ended winding fashion. The dual five-level inverter open-ended-winding induction motor drive provides more redundant states. The authors have identified the appropriate switching redundant state combinations to balance the capacitor voltages. Both of these techniques are very complicated in implementation and adds to the cost of the inverter as two five-level converters are essential. But the advantage of this connection is power quality would be improved.

DC-DC converters

Usage of Buck-Boost converter at the source end is proposed in [95][96]. Even though this technique increases the cost and complexity of control, it provides more reliability, transient stability and doesn't have any limits in balancing like other balancing techniques. The basic converter circuit proposed in [95] using buck converter is shown in Fig. 2.11. It can be identified that a basic buck converter allows current to flow only in one-direction thereby limiting the control range of balancing. To overcome this problem [97] has proposed a buck-boost converter shown in Fig. 2.12. For five-level DCMLI it has been concluded in chapter 1 that the outer capacitors will
Figure 2.11: Source-side Buck and Buck-Boost converter schematic for five-level DCMLI

share more voltage and inner capacitors will share less voltage. There by in this technique the excess charge in the outer capacitors i.e. $C_1$ and $C_4$ will be transferred to inner capacitors $C_2$ and $C_4$ through inductor. The resistors shown in the Fig. 2.12 are internal resistances of inductors. As an improvement to employment of Buck-boost converter to reduce the switching frequency, improve the dynamic response of the circuit and lower the current rating of the semiconductor devices, [97] has proposed four different control techniques to control the duty of buck-boost converter employed at front-end. Each technique serves a different objective.

A 5L-DCMLI has become a best option for DSTATCOM applications as there is no need of employing a transformer at the point of common coupling. This is because a 5L-inverter can supply sufficient voltage to the grid directly without usage of transformer [97]. The source-side balancing circuit proposed in [95] and shown in Fig. 2.11b works well as a DSTATCOM when supplying unbalanced, non-linear loads but when a DC component is induced, it will fail to balance. Even if there is a balance amongst the capacitors the voltage $V_{c1} + V_{c2}$ is not equal to $V_{c3} + V_{c4}$ there a neutral point voltage oscillation which occurs similar to 3L-NPC. To overcome this problem [97] has proposed two new control schemes one using extra components and the other without using extra components. But the one without using extra components had to carry very high current during energy exchange compared to one with extra components.

Another development in this area is usage of Resonant switched capacitor con-
Figure 2.12: Modified Buck-Boost converter schematic for 5L-DCMLI

Figure 2.13: Single leg Schematic of RSCC for 5L-DCMLI
verter (RSCC) proposed in [98]. It has been proposed that the usage of buck-boost converters for capacitor balancing is restricted to applications where regenerative action is not required and the inductor of the voltage balancing circuit requires to carry very high currents thereby adding to size weight and cost of inductor. The RSCC is capable of bi-directional power flow and the size of inductor is also reduced to one tenth size of buck-boost converter. Many control techniques were proposed for these type of converters [99][100].

2.5 Concluding Remarks

Multilevel inverters are the promising technologies for all medium high power applications owing to available ratings of the semiconductor switching devices, output THD and EMI effect. At three-level, the popular topology is 3L-NPC which has gained lot of prominence in many industrial, utility applications like HVDC, FACTS, Renewable energy etc. But these converters face capacitor voltage imbalance problem which leads to low frequency oscillation at the neutral point which overloads the switches capacitors and increases the output THD. Many solutions have been proposed for this problem. It can be observed that the level shifted reference PWM, although simple to apply, fails at high modulation index. This technique is similar to NVSVPWM and even it fails at high modulation index because as discussed the effect of medium vector on neutral point voltage deviation cannot be nullified by redundant small vectors. To overcome this problem (non near virtual vector) NNVV SVPWM techniques were proposed even they suffer from high switching loss. The switching sequence selected doesn’t lead to single switch change. The hybrid PWM techniques proposed would solve the problem to certain extent but are very complicated to implement.

Among the conventional MLI of levels, higher than Three-level, only cascaded could gain significance. But even it involves usage of many phase shifting transformers at the supply end followed by diode rectifier which makes the circuit bulky and costly. The DCMLI even though very simple in construction and doesn't require extra transformers on the supply side like cascaded MLI and neither needs very large no. of capacitors like FCMLI suffers from capacitor voltage imbalance problem. The problem is severe in five-level as it involves multiple capacitor junctions. The inherent modulation techniques proposed for three-level wasn't fail at five-level. The source balancing techniques as discussed use back-back five level rectifier inverter
topologies which makes the circuit very costly and increase the complexity. The usage of buck boost converter at source side does not allow bi-directional power flow and needs very high current carrying inductor which makes the circuit costly and bulky. On the other hand the resonant switched capacitor technique also requires extra no of switches, inductors and capacitors. The modern topologies, which are mostly hybrid, are very complicated to implement. But the one which is gaining more prominence is Modular multilevel converter (MMC).

### 2.5.1 Problem description

1. Unbalance in capacitor voltages for DCMLI is majorly dependent on load, which is not in the hands of the designer.
2. The unbalance effect reduces the level of inverter and thereby over loading the switches and capacitors.
3. The unbalance in capacitors limits the practical application of NPC MLI, which hitherto finds many applications.
4. The inherent balancing techniques proposed for 3L-NPC fail at high modulation index.
5. No successful inherent technique exists for 5L-DCMLI and the source side techniques proposed in literature employ extra components which make the circuit either costly or bulky.