**Chapter 2**

**A CRITICAL REVIEW OF SILICON-ON-INSULATOR (SOI) TECHNOLOGY**

### 2.1 Introduction

The nano-electronics industry is driven by the need of high performance devices and circuits for digital and analog applications, which is acquiring very rapidly the electronic productions markets [2.1]. From many years, bulk MOSFETs were considered as the only viable solution to satisfy the well-known Moore’s Law, which states that the performances of processors are doubled every eighteen months. Historically, device scaling remains the primary method by which the semiconductor industry has improved performances and productivity [2.1][2.2]. In nano-scale technologies, the reduction of the dimension of the devices increases the numbers of technological challenges to be solved. The short-channel effects (SCEs) and the increase of junction leakage current make difficult for the industry to follow the Moore’s Law with bulk devices [2.3].

As shown in Fig.2.1, the performance of bulk devices and circuits will not be able to follow the Moore’s Law. But, as it can be seen from Fig. 2.1 that the use of SOI can help to improve the performances [2.1]. Although it was considered twenty years ago as an exotic technology, now SOI has reached maturity. This technology has been widely demonstrated and recognized for realization of high speed and low power digital [2.2] and analog [2.3] CMOS circuits, as well as for well performance under extreme high temperature [2.4] or radiation conditions. The explosion of portable devices for wireless communication systems has opened up a great interest for SOI technology [2.3]. With advancement in state-of-the-art electronic systems and a huge
demand for low-cost high-speed mixed-signal integrated systems, a considerable effort has recently been made to migrate from GaAs to CMOS silicon process [3.3]. Since SOI CMOS devices present a very good high frequency behavior and low-power consumption, it is of great interest to use them in RF circuit design [2.1].

**Figure 2.1:** Evolution of the relative performance of SOI and bulk MOSFETs compared to the Moore’s Law.

In the last decade, the MOS transistor channel length scaled down to deep sub-micron and improved device performance in terms of cut-off frequency $f_T$. has been achieved. Recently, a 45 nm partially depleted (PD) SOI CMOS technology with $f_T$ of $\approx 485$ GHz has been reported [2.3]. Such value of $f_T$ well above 100 GHz offer a comfortable frequency margin for designers. Recently, many designs of different RF blocks have demonstrated the interest of this technology for low-voltage and low-power applications [2.3]. Fig.2.2 shows the evolution of transition frequency $f_T$ and maximum frequency of oscillation $f_{\text{MAX}}$ in the CMOS technologies. Moreover, the SOI technology has many advantages compared to the conventional bulk technology such as: lower substrate parasitic capacitances, smaller devices without latch-up phenomena, reduction of SCEs, improved sub-threshold slope (S) and possibility to use high resistivity substrate to improve the quality factor of passive
elements and RF performance matrices ($f_T$ and $f_{\text{MAX}}$) [2.5] [2.6]. All these advantages make the SOI a competitive technology for RF applications. The factors of merit comparison of bulk, partially depleted (PD)-SOI and fully depleted (FD)-SOI are summarized in Table 2.1.

![Figure 2.2:](image)

**Figure 2.2:** Evolution of transit-time frequency ($f_T$) and maximum frequency of oscillation ($f_{\text{MAX}}$) of nMOSFET vs. gate length $L_G$ (nm) for SOI and bulk technology [2.3].

The aim of this chapter is to present a critical review of SOI technology. This chapter has been organized as follows: Section 2.2 gives an overview of SOI and bulk technologies. The comparisons of FD and PD-SOI MOSFETs including their structures have been presented in section 2.3. In addition, their theoretical aspects and mathematical expressions for electrical characteristics of the SOI-MOSFETs have been carried out in section 2.4. Section 2.5 introduces how SOI wafers are fabricated? Why FD-SOI preferred in this work is discussed in section 2.6. The commercial prospective of FD-SOI MOSFETs has been discussed in section 2.7 and finally conclusions are given.
Table 2.1: Factor of merit for comparison of Bulk, PD and FD-SOI MOSFETs [2.1].

<table>
<thead>
<tr>
<th>Transistor type</th>
<th>Bulk</th>
<th>PD-SOI</th>
<th>FD-SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Approximate substrate die cost (300nm)</td>
<td>$ 300</td>
<td>$ 1000</td>
<td>$ 1000</td>
</tr>
<tr>
<td>Active silicon thickness (nm)</td>
<td>&gt; 1000</td>
<td>≦ 100</td>
<td>&lt; 40</td>
</tr>
<tr>
<td>Sub threshold swing (mV/dec)</td>
<td>&gt;120</td>
<td>80 - 120</td>
<td>65 - 80</td>
</tr>
<tr>
<td>Junction capacitance</td>
<td>Large</td>
<td>Small</td>
<td>Small</td>
</tr>
<tr>
<td>Diode leakage</td>
<td>Large</td>
<td>Small</td>
<td>Small</td>
</tr>
<tr>
<td>Vth sensitivity to Si thickness</td>
<td>None</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Extreme environment performance (upto 300°C)</td>
<td>Poor</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>Series resistance</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Vth sensitivity to buried oxide (BOX) charges</td>
<td>None</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Transconductance</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Kink effect</td>
<td>None</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Linearity</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Integration</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Noise</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Floating body effect</td>
<td>None</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>Circuit design</td>
<td>Difficult</td>
<td>Difficult</td>
<td>Easy</td>
</tr>
</tbody>
</table>

2.2 Comparison Between SOI and Bulk Technologies

The success of the SOI technology is due to its buried oxide (BOX) superiority compared to the conventional bulk silicon technology. The advantages of the BOX make this technology one of the most promising candidates in the future [2.7] [2.8].
In SOI structures (see Fig. 2.3), the top active silicon region is separated from the underlying substrate by a thick insulator layer (BOX) where a bulk MOSFETs is built a top the surface of a monocrystalline silicon wafer (see Fig. 2.4).

Thanks to the BOX layer, the SOI devices are insulated from the substrate [2.9]. So, there is no need to further isolate the devices from one another as in the case of bulk silicon. This technique in SOI minimizes the area occupied by the MOSFETs and offers a higher integration density and avoids crosstalk in telecommunication devices [2.10]. Moreover, the source/substrate and drain/substrate junction’s capacitances and leakage currents are radically reduced. The reduction of the parasitic capacitances of the MOSFET increases the $f_T$ and $f_{MAX}$ of the transistor, allowing very high speed devices compared with the bulk silicon devices. Another way of comparing the devices is that, for the same speed of SOI and bulk CMOS technologies, the SOI CMOS devices have a lower power-consumption due to lower parasitic and improved SCEs [2.10]. The insulation from the substrate also provides immunity against the unwanted thyristor triggering (also called latchup parasitic effect) [2.4] [2.10].

In the SOI-MOSFET, the space charge in the thin film of silicon $T_{si}$ is well controlled by the gate. As a consequence, the well known SCEs are reduced when compared to classical bulk MOSFET. As discussed in [2.1], the SOI MOSFETs exhibit, the inverse sub-threshold slope is lower than in a bulk MOSFET, allowing better performances in particular at low power applications. In addition, the SOI technology provides a good insulation from substrate injection noise (crosstalk) due to the oxide insulation between devices especially between the analog and digital devices on same chip [2.11] [2.12]. As seen earlier, the BOX layer offers a isolation between the active device region and the bulk substrate. This provides an additional degree of freedom when selecting the resistivity of the substrate. Using nearly intrinsic substrate to reduce the capacitive coupling and the losses whereas it is impossible in bulk technology due to latch up problem.
2.2.1 Reduction of substrate parasitic capacitances

Capacitances are a key factor for the high frequency performances considerations of devices [2.12]. Any reduction of the total capacitances of MOSFETs will increase the $f_T$ and $f_{MAX}$ of the transistor, and allowed to use the circuits at higher frequency range. In the bulk devices, due to higher doping level in the source and drain region the parasitic capacitance between source and drain to substrate are high[2.1]. With properly engineered processes and devices, the main benefit of SOI technology consisted of the fact that the drain and source capacitance to the body of the MOS
transistors are dramatically reduced [2.3], due to inherent suppression of SCEs, these types of devices can be operated at lower supply voltage. Another advantage in SOI, the maximum capacitance between junctions and the substrate is the capacitance of the BOX. This capacitance is fixed by the thickness of the BOX layer. Thanks to the lower value of its permittivity, compared to silicon, these capacitances are smaller than what we can expect for bulk MOSFET [2.6].

2.2.2 Small devices without latchup

The most important effects in bulk devices is latchup effects problem. This effect consists in the triggering of an unwanted PNPN thyristors which is present in the bulk structure (see Fig. 2.5(a)). In SOI, there is no path for any current between the terminals of the devices. Therefore, there are no any latchup effects in SOI devices as shown in Fig.2.5 (b).

![Figure 2.5: Cross section of a CMOS inverter in (a) bulk and (b) SOI technology. The parasitic thyristor in bulk inverter has been highlighted.](image)
2.2.3 Reduction of short-channel effects (SCEs)

The reduction of the SCEs is necessary to increase the operating frequency of devices and circuits at low power. This effect is related to the loss of control of the channel by the gate. In the case of SOI MOSFET the space charge in the thin film of silicon is well controlled by the gate. As a consequence, the SCEs are reduced when compared to classical bulk MOSFET and more details can be found in [2.8] [2.13].

2.2.4 Better inverse sub-threshold slope

The inverse sub-threshold slope is defined as the inverse of the slope of the $I_{DS}$ vs. $V_{DS}$ characteristics curve in the sub-threshold regime. Also, it indicates how effectively the flow of drain current of a device can be stopped when $V_{GS}$ is decreased below threshold voltage $V_{TH}$. It has been proved and demonstrated in [2.5] that the SOI MOSFET has a lower inverse sub-threshold slope than a bulk MOSFET, allowing better performances, and particular in low power applications. The more details about the SCEs (e.g. S and DIBL) can be found in [2.13]. In the next section different types of SOI devices have been explained.

2.3 Different Types of SOI-MOSFETS

The physics of SOI-MOSFETs is highly dependent on the silicon film thickness $T_{si}$ and the doping concentration of the $T_{si}$ in which they are made. Two types of devices can be distinguished: devices in which the $T_{si}$ film in the channel region is completely depleted (“fully depleted device” or “FD device”) and devices where the $T_{si}$ in the channel region never completely depleted (“partially depleted device” or “PD device”). In this section the influences of the thickness of the $T_{si}$ has been shown with comparing the FD and the PD structures. In bulk device (see Fig.2.4), the depletion zone extends from the Si-SiO$_2$ interface to the maximum depletion width $d_{max}$, which is classically expressed by (2.1) as discussed in [2.1]:

27
\[ d_{\text{max}} = \sqrt{\frac{4\varepsilon_{\text{si}}\varphi_{\text{F}}}{qN_A}} \]  

(2.1)

Where \( \varphi_{\text{F}} \) and \( \varepsilon_{\text{si}} \) are the Fermi potential and the permittivity of the silicon, \( q \) is the charge of the electron and \( N_A \) is the density of acceptors doping.

2.3.1 Fully Depleted SOI MOSFETs

In this type of device (Fig. 2.6(a)), the silicon film thickness, \( T_{\text{si}} \), is smaller or equal to \( d_{\text{max}} \). In this case, the silicon film is fully depleted at threshold, irrespective of the bias applied to the back gate (with the exception of the possible presence of thin accumulation or inversion layers at the back interface, if a large negative or positive bias is applied to the back gate, respectively) \[2.1\]. FD device is virtually free of kink effects, if their back interface is not in accumulation. In addition, this type of device exhibits the most attractive properties, such as low electric fields, high transconductance, excellent short-channel behavior, and quasi-ideal sub-threshold slope characteristics \[2.14\].

2.3.2 Partially Depleted SOI MOSFETs

In the PD-SOI device as shown in Fig.2.6 (b), \( T_{\text{si}} \) is larger than twice the value of \( d_{\text{max}} \). In such a case, there is no interaction between the depletion zones arising from the front and back interfaces \[2.1\]. A neutral region exists beneath the depletion regions. If this neutral piece of silicon, called the “body”, is connected to ground by a “body contact”, the characteristics of the device will exactly be those of a bulk device. If, however, the body is left electrically floating, the device will present some effects called the “floating body effects”, such as the “kink effect”. In addition, the presence of a parasitic open-base NPN bipolar transistor between source and drain influences the device properties. The structures of these two devices (FD and PD) are presented in Fig 2.6 (a) and (b) and their properties are described in the next section.
2.3.3 Properties of FD and PD Devices

In SOI technology, on the basis of device structure there are two distinct families of devices have been categorized: the FD-SOI and the PD-SOI. The difference
between these families is the thickness of the maximum depletion zone $d_{\text{max}}$ as discussed in the previous section. In the SOI devices above the BOX there is a silicon film thickness and oxide layer similarly below the BOX a silicon substrate (Body) is situated as shown in Fig. 2.6 (a) and (b). Front gate of the SOI structure imposes a potential on its Si/SiO$_2$ interface and as a results induces specific working modes (accumulation, depletion or inversion). When the MOSFET is working in inversion mode, the thickness of the depleted zone is maximum. The maximum thickness of each depleted zone is approximately calculated using (2.1).

In the FD-SOI-MOSFET, the depletion zone is controlled by the front-gate potentials via the gate-oxide ($C_{\text{ox1}}$) and buried oxide capacitances ($C_{\text{ox2}}$), respectively. In FD-SOI $C_{\text{si}}$ is due to completely depleted region, whereas in PD-SOI, it is mainly due to undepleted part of silicon region as shown in Fig. (2.6(a) to (b))[2.15]. $V_{GS}$ is the front-gate potential whereas $C_{\text{si}}$, $C_{\text{OX2}}$ and $C_{\text{sub}}$ are the capacitance of silicon film, BOX and the substrate capacitance, respectively. In FD-SOI, where body is grounded therefore, $C_{\text{SUB}}$ has negligible effects.

Interface coupling induces a dependence of the electrical properties of one interface from the bias applied to the other interface. So, the characterization of the front interface depend on the back interface and then on the quality of the BOX and Si/SiO$_2$ interface. Each transistor family presents specific effects: kink effect in PD devices and interface coupling phenomenon in FD devices. In thicker film FD-SOI coupling phenomenon has been avoided due to absence of coupling of front to gate. In this work relatively thicker $T_{\text{si}}$ has been used to avoid coupling effects. The PD and FD devices have some limitations such as kink effect (in PD) and sensitivity of process parameters (in FD) which are discussed below:

The kink effect in PD-SOI device is due to majority carriers, generated by impact ionization, which collects in transistor body. The body potential is raised which reduces the threshold voltage $V_{\text{TH}}$. This feedback gives rise to extra drain current (kink) in $I_{DS}$-$V_{DS}$ characteristics, which is quite annoying in analog circuits design. By taking one example with $L_G = 0.25\mu\text{m}$ and device width $W = 80\mu\text{m}$ the kink effects in PD-SOI is demonstrated as shown in Fig. 2.7. Whereas in the FD transistors, the
$T_{si}$ has a direct influences on device $V_{TH}$. Therefore, it becomes necessary to carefully control $T_{si}$ thickness to avoid some possible $V_{TH}$ dispersion.

Furthermore, $T_{si}$ thickness has a strong impact on series resistance, higher value for thinner thickness and vice-versa. As discussed in [2.16]-[2.18] the FD-MOSFETs are known to provide superior characteristics than their PD counterparts in-terms of $f_T$, $g_m$ and noise. Therefore, in this work FD-SOI MOSFET is preferred.

![Kink effects](image)

**Figure 2.7:** Output characteristics of partially depleted SOI MOSFETs with a gate length $L_G=0.25 \mu m$ and device width $W=80 \mu m$, simulated with ATLAS.

### 2.4 Theoretical Insights

Some of the parameters like threshold voltage, $V_{TH}$, sub-threshold slop $S$, drain-to-source current $I_{DS}$ and transconductance $g_m$ are the important part of the design. Therefore, in this section mathematical expressions of these electrical characteristics of FD-SOI MOSFETs have been presented.
2.4.1 Threshold voltage

In SOI MOSFET, the threshold voltage \( V_{TH} \) is defined in the same way as for the conventional bulk MOSFET. The \( V_{TH} \) can be considered as the limit for which the channel is in depletion mode [2.19]. In case the body is floating, the potential of the substrate can be neglected and the expression of \( V_{TH} \) for an n-channel transistor as discussed in [2.1] [2.20] is given below:

\[
V_{TH} = V_{FB} + 2\varphi_F + \frac{qN_A d_{max}}{C_{ox1}}
\]  

(2.2)

Where \( V_{FB} \) is the flat band voltage, \( \varphi_F \) is the Fermi potential; \( q \) is the charge of the electron; \( N_A \) is the density of acceptor atoms and \( C_{ox1} \) is the gate oxide capacitance. Replacing the parameter \( d_{max} \) by the expression (2.1) and introducing a new coefficient \( \gamma \), usually called the body-effect parameter, the threshold voltage of the PD-SOI n-channel MOSFET can be expressed as:

\[
V_{TH} = V_{FB} + 2\varphi_F + \frac{\sqrt{4\varepsilon_{Si} qN_A \varphi_F}}{C_{ox1}} = V_{FB} + 2\varphi_F + \gamma \sqrt{2\varphi_F}
\]  

(2.3)

\[
\gamma = \frac{\sqrt{2\varepsilon_{Si}qN_A}}{C_{ox1}}
\]  

(2.4)

The influence of the body bias \( (V_B) \) on the \( V_{TH} \) in a thin-film SOI n-channel MOSFET is given by:

\[
V_{TH} = V_{FB} + 2\varphi_F + \frac{\sqrt{4\varepsilon_{Si} qN_A \varphi_F}}{C_{ox1}} = V_{FB} + 2\varphi_F + \gamma \sqrt{2\varphi_F} - V_B
\]  

(2.5)

Only the last term depicts the dependence of \( V_{TH} \) on \( (V_B) \). When a negative bias is applied to the body, the \( V_{TH} \) increases as a square-root function of the body bias [2.1].

The \( V_{TH} \) of the FD-MOSFET depends on the thickness of the \( T_{si} \) [2.1]. The \( V_{TH} \) must be constant, when the thickness of the thin film is reduced, the doping level \( N_A \) must be increased, or \( C_{ox1} \) reduced. But an increase of the doping level \( N_A \) induces a reduction of the maximum depth of the depletion region \( d_{max} \), as defined by (2.1). In FD–SOI MOSFETs \( T_{si} \equiv d_{max} \) in this case, the \( V_{TH} \) will be expressed as [2.1].

\[
V_{TH} = V_{FB} + 2\varphi_F + \frac{qN_A T_{si}}{C_{ox1}}
\]  

(2.6)

From (2.6), it can be seen that \( V_{TH} \) decreases in thinner films (i.e. reduced depletion charge), until quantum effects arise and lead to the formation of a 2-D sub-band.
system. Therefore, it may be said that $V_{TH}$ of the FD-SOI MOSFET depends on the $T_{Si}$. Furthermore, if low doping level is used, like the natural doping level of the silicon film, the $V_{TH}$ will be small, but nearly independent of the film thickness. Indeed, in that case, the expression of the $V_{TH}$ will be as expressed as:

$$V_{TH} = V_{FB} + 2\varphi_F + \frac{qN_{TA_{Si}}}{C_{OX1}} = V_{FB} + 2\varphi_F$$  \hfill (2.7)

From (2.7) it is clear that the $V_{TH}$ of the FD-SOI MOSFETs is set by the gate work function.

### 2.4.2 Sub-threshold slope

Sub-threshold slope ($S$) is very crucial issue because the speed of the devices depends on $S$. If the $S$ is sharper then device can be operated faster. It means $S$ indicates how effectively the flow of drain current of a device can be stopped when $V_{GS}$ is decreased below $V_{TH}$. This can be calculated as discussed in [2.21]:

$$S = 2.3 \frac{kT}{q} \left(1 + \frac{C_{It1}}{C_{ox1}} + \alpha_1 \frac{C_{si}}{C_{ox1}} \right)$$  \hfill (2.8)

Where $\alpha_1$ = the interface coupling coefficient, $k=$Boltzmann constant, $T$ is temperature and $q$ is the charge of the electron and $C_{it1}$ accounts for the influence of front interface traps.

$$\alpha_1 = \frac{C_{ox2}+C_{it2}}{C_{si}+C_{ox2}+C_{it2}} < 1$$  \hfill (2.9)

Where $C_{it2}$ accounts for the influence of back interface traps. In the ideal case, where $C_{it1,2} \approx 0$ and the buried oxide is much thicker than both the film and the gate oxide (i.e. $\alpha_1=0$), the swing approaches the theoretical limit $S \approx 60 \text{ mV/decade}$ at 300K. Accumulation at back interface does decouple the front inversion channel from back interface defects but, in turn, makes $\alpha_1$ tends to unity (as in bulk-Si or partially depleted MOSFETs) causing on overall degradation of the swing.

The capacitances of the BOX and Si substrate are connected in series. Therefore, the swing may be depending, essentially for thin buried oxides, on the density of traps and surface charge (accumulation, depletion, or inversion) at the third interface: BOX–Si substrate. The general trend is that the sub-threshold slope improves for thinner silicon films and thicker buried oxides. For the thin-film FD-SOI devices, the
value of S is very close to the ideal case. However, the PD transistors can not exhibit S as good as FD devices. Therefore, this is a drawback of PD-SOI MOSFETs [2.1].

2.4.3 Drain-source current

When the SOI MOSFET works in low moderate inversion regime, the drain-current is dominated by the drift of the minority carriers. In this case, the expression of the low moderate-inversion current in a long channel of SOI MOSFET can be calculated as discussed in [2.1].

\[
I_{DS} = \mu C_{OX1} \frac{W}{L_G} [(V_{GS} - V_{TH})V_{DS} - \frac{1+\alpha}{2} V_{DS}^2]
\]  

(2.10)

Where \( W \) and \( L_G \) are the width and gate length of the transistor. \( V_{TH} \) and \( V_{DS} \) are the, threshold voltage and drain-source bias current, respectively. The coefficient \( \alpha \) is used in (2.10) for FD-SOI and PD can be expressed as:

\[
\alpha(FD) \equiv \frac{C_{G1} C_{OX2}}{C_{OX1} (C_{G1} + C_{OX2})}
\]

(2.11)

\[
\alpha(PD) \equiv \frac{C_{dep}}{C_{OX1}}
\]

(2.12)

The effect of the parameter \( \alpha \) is often neglected in case of FD-SOI MOSFET (\( \alpha \approx 0 \)) and in case of partially depleted, \( 0.3 \leq \alpha \leq 0.5 \) as discussed in [2.1]. In saturation region (\( V_{DS} \geq V_{DS,limit} \)), the drain-to-source current in a SOI-MOSFET can be expressed as:

\[
I_{DS} = \frac{W}{L_G} \mu \frac{C_{OX1}}{2 (1+\alpha)} (V_{GS} - V_{TH})^2
\]

(2.13)

and \( V_{DS, limit} \) can be expressed as:

\[
V_{DS, limit} \approx \frac{V_{GS} - V_{TH}}{1+\alpha}
\]

(2.14)

It is important to note that the FD-SOI MOSFET exhibits a higher drain-to-source current \( I_{DS} \) than the PD transistor for the same device size. The higher \( I_{DS} \) value in FD is due to small value of \( \alpha \) and it results in higher transconductance \( g_m \). The expression of \( g_m \) for FD as discussed in [2.1] can be calculated as:

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W \mu C_{OX1}}{L_G (1+\alpha)} (V_{GS} - V_{TH})
\]

(2.15)

Using (2.13), final expression for \( g_m \) can be expressed as:

\[
g_m = \left( \frac{2W \mu C_{OX1}}{L_G (1+\alpha)} I_{DS} \right)^{1/2}
\]

(2.16)
2.5 How SOI Wafers are Fabricated?

SOI wafer quality is a key element to ensure a success at industrial level. It is necessary a control of the silicon film thickness $T_{si}$, buried oxide thickness BOX and of their surface roughness [2.22]. The challenge of SOI material fabrication lies in the production of a thin film of single-crystal silicon on top of an insulator, usually an oxide sitting on top of a silicon wafer. Ideally both the silicon layer and the oxide layer should be defect free, stress-free and should be uniform in thickness, and should display good interface properties [2.22] [2.23]. There are various technologies available for fabrication of SOI wafers as discussed in [2.22]. Among them, SIMOX is most popular technique and it is used for commercial production of SOI wafers [2.22]. Therefore, in the next section, a detail about this technique is presented.

2.5.1 SIMOX fabrication process

In the last decade, The Separation by IMplantation of OXygen or SIMOX process is considered to be the most promising among the various SOI fabrication technologies. It is synthesized by internal oxidation during the deep implantation of oxygen ions into a Si wafer [2.1].

The buried oxide (BOX) is synthesized by internal oxidation during the deep implantation of high doses of oxygen in to a silicon wafer [2.23]. Formation of a BOX layer by high energy, high dose oxygen ion implantation has the advantage that the ion implantation dose can be made extremely precise and extremely uniform. However, the silicon and oxide layers are highly damaged after the implant, so high temperature annealing sequences are required to restore device quality material [2.24]. This technique provides good quality of wafers thickness uniformity, low defect density, high carrier mobility, the breakdown electrical field in good–quality BOX exceeds 8MV/cm, which is still below the values typical for thermal oxides (in the range of 10 to16 MV/cm) and the BOX interfaces are sharp and uniform. Some basic steps of SIMOX process as discussed in [2.23] are described below:
Step I: Thin and thick Si films are fabricated by adjusting the implant energy.

Step II: Deep implantation of a high dose oxygen into silicon wafer ($\approx 10^{18}$ O$^+$ cm$^{-2}$ at energy $\geq 150$ KeV and temp $650^\circ$C) leads to the synthesis of a BOX of 0.2-0.4$\mu$m thick underneath a thin silicon film.

Step III: Annealing at temperature ($1200^\circ$C-$1300^\circ$C) improves and simplifies the vertical SOI structure: the high quality device-grade region extends over the whole film and the interface become sharp.

Step IV: Interrupted oxide, which can be viewed as SOI region integrated in to a bulk Si wafer.

Figure 2.8: Different steps involved in SIMOX fabrication process of SOI wafers.
2.6 Why FD-SOI?

This section is a high level introduction to FD-SOI technology and its applicability to next technology nodes. This technology solves with less process complexity, scaling, leakage and variability issues to further shrink CMOS device size \[2.15\]. This technology has several advantages compared to the PD and bulk technology as given below:

1. FD-SOI devices are free of kink effect, because the majority carriers can penetrate more easily in to the source; thus preventing the excess carriers accumulations.

2. This type of devices has an enhanced sub-threshold swing, S. For the bulk and PD devices, \(S = 85\) to \(90\) mV/decade, and for the FD SOI, \(S = 65\) to \(70\) mV/decade, which is close to an ideal characteristics of a MOS transistor at room temperature \[2.11\].

3. This type of devices has the higher gain in circuit level, reduced power requirements and higher level of soft-error immunity. In addition, this technology operates faster because of a sharper sub-threshold slope, and a reduced \(V_{TH}\) that allows for faster switching of the MOS transistors. These transistors also have increased drive currents at relatively low voltages \[2.25\].

4. FD-SOI offer a reduced body effect and a nearly ideal \(g_m/I_{DS}\) ratio when biased in the weak or low moderate inversion region, therefore these transistors are fit for front-end analog applications.

5. The excellent electrostatic controlling (stronger gate control) of the FD-SOI transistor, this technology acts as a performance booster and enables lower \(V_{DD}\) (Therefore, lower power consumption) and reaching remarkable performance improvement \[2.26\].

6. An analog/RF performance of FD-SOI is \(\approx 30\%\) to \(40\%\) superior to bulk devices in nm regime. It is because of the superior sub-threshold characteristics \[2.27\].

7. FD-SOI is the major technology that can operate safely in the 0.6V to 0.7V range in nm scale. While there is some reduction in performance, operating power is reduced, giving a very compelling performance of power advantage against other technologies \[2.25\].
2.7 The Industry perspective of FD-SOI

Since the 1980s, SOI has been identified as a possible technology for increasing the performance of CMOS over the bulk [2.5]. A lot of research related to this technology is going on in the industry like STMicroelectronics, IBM, ARM, TSMC, Fjitsu etc [2.14].

In the year 2012, study by International Business Strategies (IBS) has found that those companies using FD-SOI in nm regime give substantial savings in cost-per-die as discussed in [2.2] (see Fig.2.9). For a technology to be utilized in high-volume production, costs must be lower than previous generations of technology and industry already moved to 20nm nodes, thus foundry faces a critical juncture in the shrink from sub-100nm (the precise dimensions vary from foundry to foundry) [2.28].

![Graph showing Die cost vs. various technology choices in nm regime](image.png)

**Figure 2.9:** Plot of Die cost vs. various technology choices in nm regime (from IBS 2012).
As shown in Fig. 2.9, the savings realized by using FD-SOI at the ≈20nm node is significant. Even once FinFETs will mature in year 2016, FD-SOI will still offer comparative savings of ≈50-60% cost, depending on die size. At 20nm, however, the FD-SOI processed wafer cost is less than both bulk CMOS and FinFET processed wafers. Bulk HK/MG CMOS have low parametric yields at 20nm. A major source of yield loss for bulk CMOS is that of dopant fluctuations from transistor implants. These implants are not required for FD-SOI. The time to reach defect density–related yields with allowance impact of parametric yields is estimated to be 12 to 18 months for FD-SOI while 24 to 36 months for FinFETs [2.27] [2.28].

Looking at the near future, competitive and promising FD-SOI structures on thin SOI for the next technology nodes have been reported by a number of major CMOS technology developer, notably IBM, ST, LETI and Hitachi R&D, UC Berkeley, etc.

In this work FD-SOI MOSFET has been designed and performance investigations have been carried out. For analog design, the dc gain and the matching between devices (i.e. current variation between two identical devices) are two critical points. Thus, FD-SOI MOSFET is preferred they do not suffer from kink effect and have a higher intrinsic gain [2.10]. For the RF circuit design the first choice is FD-SOI MOSFETs due to following reasons:

- If the design needs high gain, low drain-source coupling, low high frequency noise (LNA, mixer, and switch) the FD-MOSFET is preferable [2.10] [2.20].
- If the design is sensitive to low frequency noise, typically a VCO, the PD-MOSFET is preferable [2.8]. In case of high breakdown voltage (PA for instance), FD-SOI MOSFET is preferable.

Problem found in this chapter like kink effects and sensitivity of $V_{TH}$ of FD-SOI MOSFETs with process parameter variations, have been authenticated through ATLAS simulator from SILVACO in next chapter.

2.8 Conclusions

In this chapter a review of SOI technology was presented. It has been seen the advantages of SOI-MOSFETs in comparison with bulk are important not only for the digital world but also for analog/RF design. FD-SOI permits also an easier
co-integration of analog/RF and digital circuits (lower cost by reduced area). It has been exposed the comparison between FD and PD MOSFETs and finally FD-MOSFETs found superior. One approach to meet this challenge is to create a reduced power RF system-on-chip that contains digital, analog and RF portions of the design on the same die. In this context, FD-SOI appears as a technology of choice for mixed signal RF CMOS applications. As we have seen, wireless technologies require high performance transistors and low-loss passive devices (inductors and capacitors). FD-SOI allows the use of high-resistivity substrate (>3KΩ.cm), which can result in high Q for the passive elements. Therefore, numerous semiconductor industries plan to develop the FD-SOI device for the mass market. It is because of large volume production is the best way to ensure continuous price reduction and quality improvement. Honeywell, IBM, AMD and many other companies are actively working to further develop and implement this technology.
A Critical Review of Silicon-on-Insulator (SOI) Technology

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41
A Critical Review of Silicon-on-Insulator (SOI) Technology


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A Critical Review of Silicon-on-Insulator (SOI) Technology


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