ABSTRACT

Analog circuit testing is a process of identifying or locating parametric and hard faults of circuit under test (CUT) based on circuit variables called node voltages and currents. Parametric faults or soft faults are due to variation in component values causing system performance degradation and are difficult to locate whereas hard or catastrophic faults are due to open or short circuits causing topological variation and complete change in system performance. Many research proposals aim to provide solutions to analog circuit testing challenges such as tolerance limits of component values, testable group determination, test node selection, minimization of size of fault dictionary and test frequency selection in frequency domain testing.

The objective of this proposed work is to develop a method to locate multiple parametric and hard faults in linear and nonlinear analog circuits based on test vectors. Linear circuit fault diagnosis process starts with the simulation of benchmark circuits under fault free and faulty conditions using Modified Nodal Analysis (MNA), to derive circuit variables. Test vectors corresponding to all the components of CUT are derived with the knowledge of circuit topology and component values. Faults are simulated using fault rubber stamp (FRS) which is based on MNA stamp of components of CUT. To solve tolerance challenge in analog circuit testing, test vectors are generated for lower and upper bound values of components and are treated as fault dictionary. Test vectors corresponding to the circuit variables used for testing alone are stored, to achieve a reasonable amount of memory saving with the time overhead for generation of test vectors. The performance of proposed approach is validated through simulation results of benchmark circuits such as Sallen Key Band Pass Filter, Linear Voltage
Divider (LVD) and performance measures such as computational complexity in terms of time and storage requirement and fault detection efficiency are used. In case of Sallen Key BPF 57% of memory saving is achieved with 78% fault detection efficiency. Fault diagnosis is performed with three test variables measured at input and output nodes. In case of Linear Voltage Divider, 60% of memory saving is achieved with 83% fault detection efficiency. Time required for generation of test vectors is found to be 3.2 seconds and 29.12 seconds for Sallen Key BPF and LVD respectively.

In case of nonlinear analog circuits, testing is done under DC condition as it is simple and testing is performed by linearizing voltage and current relationship of nonlinear components through Taylor series approximation and solving nonlinear circuit equations using Newton Raphson method to obtain circuit variables. Performance of nonlinear circuit testing is evaluated through simulation of benchmark circuits. In case of diode circuit, 85% fault detection efficiency is achieved with 71% memory saving in storing test vectors. Time required for test vectors generation is found to be 1.14 seconds. In case of Common Emitter Amplifier, 60% memory saving is achieved with 74.5% fault detection efficiency. Time required for test vectors generation is found to be 0.79 seconds.

Testing with the test vectors generated for upper and lower bound values of components of CUT require knowledge on component tolerance limits and also that all components except the faulty one should be either in upper or lower bounds. So, testing is also done with multiple test frequencies. In multiple frequency based testing, testing is performed with nominal values of components of CUT and test frequencies are selected within the bandwidth of CUT. 87% fault detection efficiency is achieved in linear circuits with the increased number of test vectors (by four times). Test
vectors of the proposed test method are sensitive to test frequencies. Hence test vectors are generated at all test frequencies. To reduce computational complexity testing is performed with the test variables selected and test vectors corresponding to the test variables are used for testing. In case of nonlinear analog circuits, active components are replaced by its complete small signal equivalent to develop circuit equations. With the proposed method, 81.5% fault detection efficiency is achieved with three test variables and 57% memory saving is achieved. Time required for test vectors generation in fourth order LPF is found to be 29.3 seconds and in CE amplifier is 2.3 seconds. To reduce computational complexity, testing is performed with few measurements made on circuit nodes and test vectors corresponding to those variables are stored and all the calculations involved in detecting faulty components are performed with those circuit variables.

To locate multiple faults, a fault variable corresponding to each component of circuit under test is calculated. The average and relative standard deviation relative to the average value of each fault variable is obtained and an average value of all fault variables corresponding to each components of CUT is estimated and used as threshold. A component of the CUT is said to be faulty if its fault variable is lesser than the threshold. The other challenges in analog circuit testing like test variables selection and testable group determination are also solved based on the values of test vectors without any specialized algorithm.