CHAPTER 3

ANALOG CIRCUIT SIMULATION

3.1 INTRODUCTION

Analog circuit test process involves simulation of CUT under faulty and fault free conditions to derive network or circuit variables such as node voltages and currents. The first step in deriving the circuit variables is to formulate circuit equations. Many computer aided tools have been developed to simulate and to analyse electronic circuits. Vilach and Singhal (1983) presented computer aided analysis methods and explained the mathematical computational methods or techniques required for analysis and design of analog circuits. To analyze the circuit under test, popular methods such as nodal and mesh analysis can be used (Chakrabarti (2007)). But decision between mesh and nodal analysis can be made based on the implementation possibility and presentation of data about the circuit in a machine agreeable form. For the automated analysis of complex circuits, mesh analysis involve construction of tree and identification of associated links to form meshes whereas nodal analysis require only identification of node pairs. The other specialties of nodal analysis are that most of the active components can be
modelled using current sources and modification of circuit description in case of adding as well as removal of components to and from the circuit. Therefore nodal analysis is found to be a best choice for complex circuit automated analysis. But difficulty comes when a voltage source is connected in between two nodes (floating voltage source) and circuit components like operational amplifiers and other active components are used. So, a modified nodal analysis (MNA) is used because the approach is easy to implement as an algorithm and at the same it handles voltage sources and active components connected between nodes effectively. A linear system solver is used to solve the equations obtained and to find the node voltages and currents and in case of nonlinear analog circuits Newton Raphson method is used.

### 3.2 MNA FOR LINEAR CIRCUITS

MNA is an extension of nodal analysis which is used to determine circuit's node voltages and few branch currents. Modified nodal analysis was developed to alleviate the difficulty of representing voltage-defined components in nodal analysis (Ho et al. (1975)).

#### 3.2.1 Nodal Analysis

Nodal analysis starts by selecting a reference node of a circuit with ‘n’ nodes. Remaining ‘n-1’ nodes are assigned with names (node 1, node 2 or node a, node b) and a current through each element and current source is labeled. To formulate circuit equations, Kirchhoff’s current Law (KCL) is applied to each node and solutions are obtained by solving the circuit equations. The difficulty in applying KCL arises when a voltage source is present in between two ungrounded nodes. This type of problem is eliminated by super node analysis but it is difficult to develop an algorithm in automated analysis. Figure 3.1 is an example circuit used to explain the nodal analysis.
The reference node is represented as node 0 and other nodes are named as 1, 2 and 3.

**Figure 3.1  Nodal Analysis Example Circuit**

KCL application on each node (1, 2 and 3 respectively) leads to set of equations as below,

\[
\frac{V_1 - V_2}{R_1} = I_S 1
\]  \hspace{1cm} (3.1)

\[
\frac{V_2 - V_1}{R_1} + \frac{V_2 - V_3}{R_2} + \frac{V_2}{R_3} = 0
\]  \hspace{1cm} (3.2)

\[
\frac{V_3 - V_2}{R_2} + \frac{V_3}{R_4} = 0
\]  \hspace{1cm} (3.3)

The above equations can be solved for the unknowns V1, V2, V3 (node voltages).
3.2.2 Modified Nodal Analysis

Modified nodal analysis follows the same steps as in nodal analysis. But in case of voltage sources connected in between nodes, it assumes a current through each voltage source and KCL is applied. A separate equation must be written for voltage sources. This increases number of equations developed. An example circuit is shown in Figure 3.2 to illustrate the procedure.

\[ \text{application of KCL at node 1 yields,} \]

\[ I_{va} + \frac{V_1 - V_2}{R_1} = 0 \]  \hspace{1cm} (3.4)

\[ \text{applying KCL at node 2,} \]

\[ \frac{V_2 - V_1}{R_1} + \frac{V_2}{R_2} + I_{vb} = 0 \]  \hspace{1cm} (3.5)

\[ \text{KCL at node 3 gives,} \]

\[ -I_{vb} + \frac{V_3}{R_3} = 0 \]  \hspace{1cm} (3.6)
Iva and Ivb are the currents assumed through the voltage sources or the current through the branches between nodes 1 and 0, 2 and 3. Equations for Va and Vb are written as below,

\[ V1 = Va \]  \hspace{1cm} (3.7)  
\[ V2 - V3 = Vb \]  \hspace{1cm} (3.8)

To solve for unknowns, equations from 3.4 to 3.8 can be written in matrix form as below,

\[
\begin{bmatrix}
\frac{1}{R1} & -\frac{1}{R1} & 0 & 1 & 0 \\
\frac{1}{R1} & \frac{1}{R1} + \frac{1}{R2} & 0 & 0 & 1 \\
0 & 0 & \frac{1}{R3} & 0 & -1 \\
1 & 0 & 0 & 0 & 0 \\
0 & 1 & -1 & 0 & 0 \\
\end{bmatrix}
\begin{bmatrix}
V1 \\
V2 \\
V3 \\
Iva \\
Ivb \\
\end{bmatrix}
=
\begin{bmatrix}
0 \\
0 \\
0 \\
Va \\
Vb \\
\end{bmatrix}
\]  \hspace{1cm} (3.9)

and this can be expressed as,

\[ AX = Z \]  \hspace{1cm} (3.10)

where A is called circuit coefficient matrix, X is a matrix with unknowns (node voltages and mesh currents) and Z is the excitation matrix. Equation (3.10) can be solved by,

\[ X = A^{-1}Z \]  \hspace{1cm} (3.11)

a simple matrix linear system solver.

### 3.3 MNA ALGORITHM FOR LINEAR CIRCUITS
To develop an algorithm for modified nodal analysis, it can be observed from equation (3.10) that three matrices (circuit coefficient matrix, excitation matrix and matrix with unknowns) are to be created. These three matrices can be formed as a combination of sub matrices. For example, matrix A can be subdivided as G, B, C and D.

3.3.1 Generation of Matrix A

For a circuit with ‘n’ nodes and ‘m’ independent voltage sources, A matrix is \((m+n) \times (m+n)\) in size and consists of only known quantities and it can be developed as a combination of four matrices as below,

\[
A = \begin{bmatrix} G & B \\ C & D \end{bmatrix}
\]  

(3.12)

G matrix is a \(n\times n\) matrix which is formed by interconnection of conductance of circuit components and it can be observed from equation (3.9) that each element in the diagonal is the sum of the conductance of each element connected to the corresponding node. The off diagonal elements are negative conductance of the element connected to the pair of corresponding node.

B matrix is an \(n \times m\) matrix and consists of only 0, 1 and -1. These values are determined based on the location of voltage sources in the circuit. If the positive terminal of the \(i^{th}\) voltage source is connected to node \(j\), then the element \((i,j)\) in the B matrix is a 1. If the negative terminal is connected to node \(j\), then the element \((i,j)\) in the B matrix is a -1. Otherwise, elements of the B matrix are zero.
C-matrix is the transpose of B-matrix if the circuit contains only independent voltage sources. The D matrix is an m×m matrix that contains only zeros if the circuit has only independent voltage sources. In case of dependent sources, the elements of D matrix are nonzero values.

### 3.3.2 Generation of X Matrix

X matrix is of (m+n) ×1 in size and consists of unknown quantities and it is defined as a combination of two matrices ‘v’ and ‘k’.

\[
X = \begin{bmatrix}
v \\
k
\end{bmatrix}
\]

(3.13)

‘v’ matrix is developed from unknown node voltages and it is n×1 in size. The ‘k’ matrix contains current through voltage sources as unknown quantities and its size is m×1.

### 3.3.3 Generation of Z Matrix

Z matrix is formed by the voltage sources and current sources in the circuit and it has (m+n) ×1 elements. It is developed from two sub matrices as given in equation (3.14).

\[
Z = \begin{bmatrix}
i \\
e
\end{bmatrix}
\]

(3.14)

where ‘i’ is a n×1 matrix contains sum of independent currents to a node and ‘e’ is a m×1 matrix consists of values corresponding to the voltage sources.

### 3.4 MNA STAMPS FOR LINEAR CIRCUIT ELEMENTS
In MNA matrix, entries correspond to the conductance of each element. These entries follow a regular format called stamp and they are based on the nodes to which the elements are connected. MNA stamps for linear and nonlinear circuit elements are explained by Fakhfakh et al. (2012) and MNA stamps for few elements that are used in the research work are highlighted here.

3.4.1 MNA Stamp for Resistor

Figures 3.3 and 3.4 show the MNA stamp for resistors. A resistor connected in between two nodes $N_1$ and $N_2$ leads positive values (conductance) in the main diagonal of circuit coefficient matrix and negative values in off-diagonal entries of circuit coefficient matrix. If a resistor is connected in between a node and ground, it appears only in the main diagonal of circuit coefficient matrix.

$$
\begin{array}{c|cc|}
| & V_1 & V_2 & \text{RHS} \\
\hline
N_1 & \frac{1}{R} & -\frac{1}{R} & \\
N_2 & -\frac{1}{R} & \frac{1}{R} & \\
\end{array}
$$

**Figure 3.3** MNA Stamp of Resistor between Two Nodes

$$
\begin{array}{c|c|}
| & V_1 & \text{RHS} \\
\hline
N_1 & \frac{1}{R} & \\
\end{array}
$$

**Figure 3.4** MNA Stamp of Resistor between a Node and Ground
3.4.2 MNA Stamp for Reactive Elements

The reactive elements such as inductors and capacitors are represented by their complex impedances and the stamp entries are similar to resistors. Figures 3.5 to 3.8 show the MNA stamp for reactive elements.

<table>
<thead>
<tr>
<th></th>
<th>V₁</th>
<th>V₂</th>
<th>RHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N₁</td>
<td>1/sL</td>
<td>-1/sL</td>
<td></td>
</tr>
<tr>
<td>N₂</td>
<td>-1/sL</td>
<td>1/sL</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.5    MNA Stamp of an Inductor between Two Nodes

<table>
<thead>
<tr>
<th></th>
<th>V₁</th>
<th>RHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N₁</td>
<td>1/sL</td>
<td></td>
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</table>

Figure 3.6    MNA Stamp of an Inductor between a Node and Ground

<table>
<thead>
<tr>
<th></th>
<th>V₁</th>
<th>V₂</th>
<th>RHS</th>
</tr>
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<tbody>
<tr>
<td>N₁</td>
<td>sC</td>
<td>-sC</td>
<td></td>
</tr>
<tr>
<td>N₂</td>
<td>-sC</td>
<td>sC</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.7    MNA Stamp of capacitor between Two Nodes

<table>
<thead>
<tr>
<th></th>
<th>V₁</th>
<th>RHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>N₁</td>
<td>sC</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.8    MNA Stamp of capacitor between a Node and Ground
3.4.3 MNA Stamp of an Ideal Current Source

In case of an ideal current source, the right hand side matrix called excitation matrix has its entries corresponding to the current source and current flow direction. The entries in the excitation matrix (RHS) due to a current source connected in between two nodes are shown in Figure 3.9.

![Figure 3.9 MNA Stamp for Ideal Current Source between Two Nodes](image)

From this it can be observed that the entries are positive for current entering a node and negative for current leaving a node. If a current source is connected in between a node and ground, then there is going to be only one entry with positive or negative sign based on the current flow direction.

Figure 3.10 shows the MNA stamp for ideal current source connected between a node and ground.

![Figure 3.10 MNA Stamp for Ideal Current Source](image)
### 3.4.4 MNA Stamp for Ideal Voltage Source

MNA stamp of an ideal independent voltage source connected between two nodes is shown in Figure 3.11. For independent ideal voltage source, a current ($I_v$ leaves node $N_1$ and enters $N_2$) through it is assumed in circuit equations formulation and an additional equation for the voltage source is written as below,

$$V_1 - V_2 = 0$$

(3.15)

where $V_1$ and $V_2$ are the node voltages at the nodes $N_1$ and $N_2$. And the circuit stamp for an ideal voltage source is,

![Figure 3.11 MNA Stamp for Ideal Voltage Source between Two Nodes](image)

**Figure 3.11 MNA Stamp for Ideal Voltage Source between Two Nodes**

MNA stamp for an ideal independent voltage source connected between a node and ground is shown in Figure 3.12. The additional equation for the voltage source is written as below,

$$V_1 = V_s$$

(3.16)
MNA treats ideal operational amplifier (op-amp) similar to ideal voltage source. As in the case of ideal voltage source a current through operational amplifier \(I_{OA}\) is introduced as an unknown variable in the unknown matrix and a separate equation is written for the input voltage. Figure 3.13 shows the stamp for ideal op-amp.

\[
V_1 - V_2 = 0 \tag{3.17}
\]

3.5 MNA FOR NONLINEAR CIRCUITS
In case of circuits with nonlinear components like diodes and transistors, testing is performed under DC conditions as DC testing is simple and DC analysis is prior to an AC small signal analysis to determine linearized small signal models for nonlinear devices. The nonlinear components are modelled using large signal model or DC models to formulate circuit equations. Current through the devices is introduced as a new circuit variable in the unknown matrix (X) and Newton Raphson method is used to solve the equations.

3.5.1 Introduction to Newton Raphson method

Newton Raphson (NR) method is very popular in solving nonlinear equations because of its fast convergence with only one initial guess. A good initial guess cause convergence to the expected result and poor initial guess leads to divergence. It also requires estimating the derivative of the function or equations to be solved. Newton Raphson method uses first order terms of Taylor series of a function \( f(x) \). Taylor series of \( f(x) \) in \((x-x_0)\) is given by

\[
f(x) = f(x_0) + f'(x_0)(x - x_0) + \frac{1}{2} f''(x_0)(x - x_0)^2 + \ldots \ldots
\]

Keeping only first order terms,

\[
f(x) = f(x_0) + f'(x_0)(x - x_0)
\]  

(3.19)

where \( x_0 \) is the initial guess and N-R iteration formula (Vilach and Singhal (1983)) can be obtained as

\[
x_{i+1} = x_i - \frac{f(x_i)}{f'(x_i)}
\]

(3.20)
where \( x_{i+1} \) is the new estimate, \( x_i \) initial guess or value of previous estimate, 
\( f(x_i) \) value of function at \( x_i \) and \( f'(x_i) \) value of derivative of the function at \( x_i \).

### 3.5.2 Newton Raphson Algorithm

Figure 3.14 shows the algorithmic representation of Newton Raphson method to solve. For the function or equation to be solved, derivative is first obtained and an error value is assumed for the desired accuracy. The iterative process starts with an initial guess and continues till the desired accuracy is obtained.

### 3.5.3 Multi-Variable Newton Raphson Algorithm

Newton Raphson for single variable can be generalized to multiple variable cases to solve ‘n’ simultaneous nonlinear equations (Vilach and Singhal (1983)). Consider a system of nonlinear equations \( f_i \) in \( n \) variables \( x_i \),

\[
\begin{align*}
  f_1(x_1, x_2, \ldots, x_n) &= 0 \\
  f_2(x_1, x_2, \ldots, x_n) &= 0 \\
  f_n(x_1, x_2, \ldots, x_n) &= 0
\end{align*}
\]  

(3.21)
Expanding each function in a Taylor series,

\[
f_1(x^{k+1}) = f_1(x^k) + \frac{\partial f_1}{\partial x_1}(x_1^{k+1} - x_1^k) + \frac{\partial f_1}{\partial x_2}(x_2^{k+1} - x_2^k) + \ldots + \frac{\partial f_1}{\partial x_n}(x_n^{k+1} - x_n^k)
\]

\[
f_2(x^{k+1}) = f_2(x^k) + \frac{\partial f_2}{\partial x_1}(x_1^{k+1} - x_1^k) + \frac{\partial f_2}{\partial x_2}(x_2^{k+1} - x_2^k) + \ldots + \frac{\partial f_2}{\partial x_n}(x_n^{k+1} - x_n^k)
\]
\[ f_n(x^{k+1}) = f_n(x^k) + \frac{\partial f_n}{\partial x_1}(x_1^{k+1} - x_1^k) + \frac{\partial f_n}{\partial x_2}(x_2^{k+1} - x_2^k) + \ldots + \frac{\partial f_n}{\partial x_n}(x_n^{k+1} - x_n^k) \]  

(3.22)

where ‘k’ is the iteration count and \( x^{k+1} \) is called new estimate.

The system in linearized form can be written as,

\[ f(x^{k+1}) = f(x^k) + M(x^{k+1} - x^k) \]  

(3.23)

where 

\[ M = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \frac{\partial f_1}{\partial x_2} & \ldots & \frac{\partial f_1}{\partial x_n} \\ \frac{\partial f_2}{\partial x_1} & \frac{\partial f_2}{\partial x_2} & \ldots & \frac{\partial f_2}{\partial x_n} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial x_1} & \frac{\partial f_n}{\partial x_2} & \ldots & \frac{\partial f_n}{\partial x_n} \end{bmatrix} \]  

(3.24)

and is called the Jacobian matrix of the function \( f \).

Equating (3.23) to zero to solve \( f(x) = 0 \),

\[ f(x^k) + M(x^{k+1} - x^k) = 0 \]  

(3.25)

Rewriting Equation (3.25) as,

\[ f(x^k) + Mx^{k+1} - Mx^k = 0 \]  

(3.26)

and simplifying Equation (3.26) as below,

\[ M(x^{k+1} - x^k) = -f(x^k) \]  

(3.27)
\[ x^{k+1} - x^k = -M^{-1} f(x^k) \] (3.28)

\[ x^{k+1} = x^k - M^{-1} f(x^k) \] (3.29)

Equation (3.29) is called Newton Raphson equation. From equation (3.29), it can be understood that the new estimate or solution can be obtained by an iterative process. It has been proved that the Newton Raphson algorithm converges quickly with good initial guess but the need is to estimate the Jacobian matrix.

3.6 LARGE SIGNAL MODELS OF ACTIVE DEVICES

To represent the behavior of active components such as diodes and transistors under DC and AC operating environments, accurate models have been developed as explained by Sedra and Smith (1998). This section explains only the DC models used in the proposed work.

3.6.1 Large Signal Model of PN Diode

Exponential models are used as the most accurate description of diode operation under DC condition and the diode I-V characteristic is represented by the exponential relationship,

\[ I_D = I_S e^{V_D/V_T} \] (3.30)

where \( I_S \) is the reverse saturation current (due to minority charge carriers), \( n \) is a constant that has a value between 1 and 2 (depending on the material and the physical structure of the diode. Diodes made using standard integrated circuit fabrication techniques exhibit \( n=1 \) under normal conditions and diodes
available as discrete two-terminal components exhibit \( n=2 \). \( V_T \) in Equation (3.30) is a constant called thermal voltage and is given by,

\[
V_T = \frac{kT}{q}
\]  
(3.31)

where \( k = \) Boltzmann’s constant = \( 1.38 \times 10^{-23} \text{joules/Kelvin} \)

\( T = \) the absolute temperature in kelvin = \( 273 + \) temperature in °C

\( q = \) the magnitude of electron charge = \( 1.60 \times 10^{-19} \text{coulomb} \)

### 3.6.2 Large Signal Model of BJT

In case of Bipolar Junction Transistors (BJT), Ebers-Moll model is used to describe the behaviour of BJT as it can be used to predict the operation in all of its possible modes (Sedra and Smith (1998)). Figure 3.15 shows the Ebers Moll model of NPN transistor.

![Ebers Moll Model of NPN Transistor](image)

**Figure 3.15  Ebers Moll Model of NPN Transistor**

The collector, emitter and base terminal currents are denoted as \( I_c, I_e \) and \( I_b \). \( \alpha \) is called common base current gain and subscript \( F \) and \( R \) represents forward and reverse active mode respectively. The model equations are given below,
where $I_S$ is called reverse saturation current and it is of the order of $10^{-15}$ to $10^{-12}$ ampere and $V_{BE}$, $V_{BC}$ are the base-emitter and base-collector voltages. $V_T$ is called thermal voltage which is 26mV at room temperature. $\beta$ is called common emitter current gain and subscript $F$ and $R$ represents forward and reverse active mode. Common emitter current gain is related to common base current gain as below,

$$I_e = \left(\frac{I_S}{\alpha_F}\right)(e^{\frac{V_{BE}}{V_T}} - 1) - I_S\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \quad (3.32)$$

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \left(\frac{I_S}{\alpha_R}\right)(e^{\frac{V_{BC}}{V_T}} - 1) \quad (3.33)$$

$$I_B = \left(\frac{I_S}{\beta_F}\right)(e^{\frac{V_{BE}}{V_T}} - 1) + \left(\frac{I_S}{\beta_R}\right)(e^{\frac{V_{BC}}{V_T}} - 1) \quad (3.34)$$

Forward current gain value is within the bound of 20 - 500 and reverse current gain lies within 0-20.

3.7 NONLINEAR ELEMENT STAMPING

In computerized methods of solving nonlinear circuits, nonlinear circuits are linearized and linear equations are solved iteratively till the convergence is met. Each nonlinear element of the nonlinear circuit is characterized by its linearized model called stamp which is be obtained by applying Newton Raphson method to the nonlinear MNA equations.
3.7.1 Diode Stamp

Nonlinear element stamp can be obtained by applying Newton Raphson method directly to the nonlinear equation that characterizes the nonlinear element. In case of diode, the element equation is,

\[ i_d = I_s[e^{\frac{V_D}{kT}} - 1] \]  \hspace{1cm} (3.37)

where \( i_d \) is the diode current, \( I_s \) is called reverse saturation current, \( V_D \) is called diode voltage, \( n \) is a constant that has a value between 1 and 2 (depending on the material and the physical structure of the diode) and \( V_T \) is the thermal voltage.

Application of Newton Raphson method to Equation (3.37) involves expressing (3.37) in a Taylor series,

\[ i_d^{k+1} = i_d^k + \left( \frac{\partial i_d}{\partial V_D} \right)^k (V_D^{k+1} - V_D^k) \]  \hspace{1cm} (3.38)

Rearranging Equation (3.38),

\[ i_d^{k+1} = i_d^k + \left( \frac{\partial i_d}{\partial V_D} \right)^k V_D^{k+1} - \left( \frac{\partial i_d}{\partial V_D} \right)^k V_D^k \]  \hspace{1cm} (3.39)

and expressing Equation (3.39) as,

\[ i_d^{k+1} = G_i V_D^{k+1} + I_o \]  \hspace{1cm} (3.40)

where \( G_i = \left( \frac{\partial i_d}{\partial V_D} \right)^k \)  \hspace{1cm} (3.41)
and \( I_D = i_D^k - (\frac{\partial i_D}{\partial V_D})^k V_D^k \) \hspace{1cm} (3.42)

Equation (3.40) is the linearized form of diode current equation and the linearized model and MNA diode stamp is shown in Figure 3.16 (a, b and c).

(a) Diode \hspace{1cm} (b) Diode Model

<table>
<thead>
<tr>
<th>( V_1 )</th>
<th>( V_2 )</th>
<th>RHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_1 )</td>
<td>( G_0 )</td>
<td>-( G_0 )</td>
</tr>
<tr>
<td>( N_2 )</td>
<td>-( G_0 )</td>
<td>( G_0 )</td>
</tr>
</tbody>
</table>

(c) Diode Stamp

Figure 3.16 (a) Diode, (b) Diode Model, (c) Diode Stamp

3.7.2 BJT Stamp

BJT stamp can be derived from its DC large signal model or the Ebers-Moll model and the linearized model equations. Linearized model equations are obtained by expressing the model equations in Taylor series,

\[
i_{c,1}^{k+1} = I_c^k - g_{ce}^k V_{bc}^{k+1} + g_{ce}^{k+1} V_{ce}^{k+1}
\] \hspace{1cm} (3.43)

\[
i_c^{k+1} = g_{ce}^k V_{bc}^{k+1} - g_{ce}^{k+1} V_{bc}^{k+1} + I_c^k
\] \hspace{1cm} (3.44)

\[
i_b^{k+1} = -(i_{c,1}^{k+1} + i_c^{k+1})
\] \hspace{1cm} (3.45)
where \( I_{e}^{k} = i_{e}^{k} + g_{ee}^{k}V_{be}^{k} - g_{ee}^{k}V_{bc}^{k} \) (3.46)

\[ g_{ee}^{k} = \left( \frac{\partial i_{e}}{\partial V_{be}} \right)^{k} = \frac{I_{s}}{V_{T}} e^{\frac{V_{be}}{V_{T}}} \] (3.47)

\[ g_{ec}^{k} = \left( \frac{\partial i_{e}}{\partial V_{bc}} \right)^{k} = \alpha_{p} \frac{I_{s}}{V_{T}} e^{\frac{V_{bc}}{V_{T}}} \] (3.48)

\[ I_{e}^{k} = i_{e}^{k} - g_{ee}^{k}V_{be}^{k} + g_{ee}^{k}V_{bc}^{k} \] (3.49)

\[ g_{ee}^{k} = \left( \frac{\partial i_{e}}{\partial V_{be}} \right)^{k} = \alpha_{p} \frac{I_{s}}{V_{T}} e^{\frac{V_{bc}}{V_{T}}} \] (3.50)

\[ g_{cc}^{k} = \left( \frac{\partial i_{e}}{\partial V_{bc}} \right)^{k} = -\frac{I_{s}}{V_{T}} e^{\frac{V_{bc}}{V_{T}}} \] (3.51)

Thus the MNA stamp for BJT (NPN) is shown in Figure 3.17 (a, b and c)

(a) BJT -NPN

(b) Linear Model of BJT-NPN
<table>
<thead>
<tr>
<th></th>
<th>e</th>
<th>c</th>
<th>b</th>
<th>RHS</th>
</tr>
</thead>
<tbody>
<tr>
<td>e</td>
<td>$g_{ee}^k$</td>
<td>$-g_{ee}^k$</td>
<td>$g_{cc}^k - g_{ee}^k$</td>
<td>$-I_e^k$</td>
</tr>
<tr>
<td>c</td>
<td>$-g_{ce}^k$</td>
<td>$g_{cc}^k$</td>
<td>$g_{ce}^k - g_{cc}^k$</td>
<td>$-I_c^k$</td>
</tr>
<tr>
<td>b</td>
<td>$g_{ce}^k - g_{ee}^k$</td>
<td>$g_{cc}^k - g_{cc}^k$</td>
<td>$g_{ec}^k + g_{ee}^k - g_{ce}^k - g_{ec}^k$</td>
<td>$I_e^k + I_c^k$</td>
</tr>
</tbody>
</table>

(c) BJT (NPN) stamp

Figure 3.17  (a) BJT –NPN, (b) Linear Model of BJT-NPN, (c) BJT (NPN) stamp

3.7.3 MNA from Element Stamps

In an algorithmic way of formulating circuit equations and solving it for circuit parameters, element stamps are used and are directly entered into the linearized system equation. With Newton Raphson, the linearized system equations are obtained as,

$$M(x^{k+1} - x^k) = -f(x^k) \quad (3.52)$$

Let \( \Delta x^k = x^{k+1} - x^k \) \quad (3.53)

Substituting Equation (3.53) in Equation (3.52), the linearized system to be solved is,

$$M\Delta x^k = -f(x^k) \quad (3.54)$$

rearranging Equation (3.53), the expression for new estimate can be obtained as,
To solve the linearized system, the Jacobian matrix $M$ is to be estimated to find the circuit parameters such as node voltages and branch currents. From the above discussions, it can be understood that Jacobian matrix can be built using element stamps or the element stamps form the Jacobian matrix.

### 3.7.4 MNA Modifications

In case of nonlinear circuits to minimize simulation time new Newton Raphson models for the electronic circuits are developed by Augusto, JS and Almeida (2000). Simulation time is minimized by minimizing iteration dependent blocks. To minimize iteration dependent blocks, nonlinear devices are described by the corresponding node voltages as a function of current and current through the nonlinear devices is introduced as a new unknown variable and nonlinear devices are modelled as current controlled devices. Nonlinear devices are described by their $V$-$I$ relationship as

$$V = f (I)$$  \hspace{1cm} (3.56) \tag{3.56}

The Taylor series approximation (neglecting higher order terms) of (3.56) is,

$$V^{K+1} = V^K + (df(I)/dI)^K (I^{K+1} - I^K)$$  \hspace{1cm} (3.57) \tag{3.57}

where $K$- NR iteration number,

Rearranging (3.57),

$$V^{K+1} - (df(I)/dI)^K I^{K+1} = V^K - (df(I)/dI)^K I^K$$  \hspace{1cm} (3.58) \tag{3.58}
Let \( V^K - (df(I)/dI)I^K = a^K \) \hspace{1cm} (3.59)

Now (3.58) becomes

\[
V^{K+1} - (df(I)/dI)^KI^{K+1} = a^K
\] \hspace{1cm} (3.60)

Now the system equations are written in matrix form as below,

\[
\begin{bmatrix}
G_{11} & \ldots & G_{1n} & B_{11} \\
\vdots & \ddots & \vdots & \vdots \\
G_{n1} & \ldots & G_{nn} & B_{n1} \\
C_{11} & \ldots & C_{1n} & -(df(I)/dI)^K
\end{bmatrix}
\begin{bmatrix}
V_{1}^{K+1} \\
\vdots \\
V_{n}^{K+1} \\
d^{K+1}
\end{bmatrix}
= 
\begin{bmatrix}
. \\
. \\
. \\
.
\end{bmatrix}
\] \hspace{1cm} (3.61)

and from the equation (3.61), it can be observed that the right most element of A matrix alone changes in each iteration.

3.8 FAULT SIMULATION

Fault diagnosis process in analog circuit testing involves faults detection, isolation, identification, prediction, explanation and fault simulation. Fault detection is a process of identifying the abnormal behaviour of the circuit under test. Fault detection is usually performed by comparing the obtained responses of a faulty circuit with the responses of fault free circuit. An analog circuit is said to be faulty if its response lie outside the fault free response.

Fault isolation is the process of mapping of the faulty conditions to the physical part or region of the circuit under test to locate or identify the faulty component by fault identification process. It is possible to predict the behaviour of the circuit and to locate the faulty component by continuously monitoring the circuit under test. This process is termed as fault prediction.
Fault explanation is defined as the process of presenting the results of fault detection and identification in a desired manner.

Fault simulation is a process of simulating a hypothetical fault in a circuit, with the knowledge of fault models and fault identification process. In analog circuit fault diagnosis, a fault is defined as a kind of malfunction in the system that causes an unacceptable system performance. Faults are caused by poor design, manufacturing defects, ageing of components, improper operating conditions and stress beyond the allowable limits. A component of an analog circuit is said to be faulty when its value falls outside its tolerance limits.

Fault simulation is done to simulate the behaviour of an analog circuit for a given set of faults. Fault simulation techniques are developed to analyse system performance under faulty conditions which is required to improve circuit reliability, to analyse fault coverage of a particular testing method, effect of components out of specification, to evaluate the effectiveness of a set of test patterns or waveforms generated automatically or manually.

Fault simulation process is a combination of fault modelling, fault injection and system performance simulation. Fault simulation process begins by defining the type of faults to be tested called fault modelling, introducing them in to the circuit under test and analysing the effect of these faults on circuit performance and recording it for further analysis. Figure 3.18 explains this. Analog faults are modelled as parametric and catastrophic faults. Hard or catastrophic faults are the open and short circuit faults of circuit components.
Parametric faults are variation of circuit component values outside its tolerance limit. Single or multiple faults are simulated to test the performance of a faulty circuit. Multiple faults simulation is useful when the circuit performance depends on ratios of components.

### 3.8.1 Fault Injection

Fault injection procedure aims to introduce the faulty conditions into the circuit under test. Circuit under test is described in the form of net list as explained in Section 3.5 which includes the components name, components nodal connections and the value of components. A fault list based on fault models is prepared and the circuit description file is modified accordingly. With the modified circuit description, the new circuit is simulated to obtain the performance parameters. Figure 3.19 shows the steps involved in fault injection procedure.

![Fault Injection Procedure](image)

**Figure 3.19 Fault Injection Procedure**

Figure 3.20 (a) shows a sample circuit (All Pass Filter) and Figure 3.20 (b) shows the net list form of circuit description of All Pass Filter.
(a) All Pass Filter

<table>
<thead>
<tr>
<th>R</th>
<th>1</th>
<th>2</th>
<th>10000</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2</td>
<td>2</td>
<td>4</td>
<td>10000</td>
</tr>
<tr>
<td>R3</td>
<td>1</td>
<td>3</td>
<td>15900</td>
</tr>
<tr>
<td>C1</td>
<td>3</td>
<td>0</td>
<td>10E-9</td>
</tr>
<tr>
<td>OAm</td>
<td>3</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>

(b) Net list of All Pass Filter

Figure 3.20 (a) All Pass Filter, (b) Net list of All Pass Filter

In net list form of circuit description shown in Figure 3.20 (b), first column corresponds to the name of the circuit components, second and third columns describe the location or nodal position of the components in the circuit and the fourth column gives the value of the components. For a faulty condition, $R_1 = 5000\Omega, R_3 = 25000\Omega$, the circuit description file or net list of All Pass Filter is modified as shown in Figure 3.21.
Simulation of CUT begins for a specific identified stimulus with the net list file. Based on the test stimuli fault simulation process is classified as DC, AC and time domain fault simulation. DC analysis of an analog circuit is required to test and to fix the biasing conditions of an analog circuit so that all the devices and circuit components are operated within their normal operating range. DC analysis is also required to analyse the frequency response characteristics of an analog circuit as it varies around the DC operating points. In analog circuit testing, DC testing is popular especially in case of nonlinear analog circuits because it requires inexpensive test set up and less testing time. Fault simulation under DC conditions is a useful approach to analyse the effectiveness of DC testing of analog circuits for a set of given faulty conditions. DC testing is performed by finding solution for a set of nonlinear equations that describe the circuit behaviour. The set of nonlinear equations are solved iteratively until the convergence criterion is met.

AC analysis also called small signal analysis of an analog circuit is used to understand the behaviour of the circuit at various frequencies. Linear or small signal models of nonlinear components are used to linearize the system behaviour. From AC analysis or frequency response characteristics, the operating frequency range or bandwidth of a circuit, gain at various frequencies, gain roll-off rate and peak gain frequency can be obtained. Time domain behaviour of the circuit can be obtained from transient analysis. Linear
analog circuits are tested under AC conditions and nonlinear analog circuits are tested under DC conditions and AC conditions.

3.8.2 Fault Rubber Stamp

Faults are simulated using Fault Rubber Stamp (FRS) technique. FRS is based on the MNA stamp of the components of CUT. The speciality of FRS technique is that the circuit matrix under faulty condition is unchanged. Instead a new row and a column have been added in the circuit matrix (A) for each faulty element. As each faulty condition introduces an additional row and column into the circuit matrix, the approach requires larger number of equations to be solved.

Modified nodal analysis based simulation of analog circuit involves development of circuit matrix, matrix with unknowns such as node voltages and branch currents and excitation matrix. These matrices are generated using stamps of the components of CUT as explained in section 3.4. The MNA stamp of a component $C_n$ connected in between the nodes $j$ and $j'$ in the circuit matrix is given as,

$$
\begin{pmatrix}
V_j \\
V_{j'}
\end{pmatrix} =
\begin{pmatrix}
+jC_n & -C_n \\
-C_n & +C_n
\end{pmatrix}
$$

(3.62)

where $j$ and $j'$ represent nodes and $V_j$ and $V_{j'}$ are the corresponding node voltages. For a faulty component, the component value changes from its nominal value $C_n$ to $C_n \pm \Delta$. This deviation in component value causes variation in current through that component. This new current value is being added as an unknown branch current and a new variable called fault variable $\phi$ in the unknown matrix (X). To indicate this deviation in current, the faulty component is represented as a parallel combination of its fault free
value \( (C_n) \) and the deviation \( (\Delta) \). This representation of a faulty component is shown in Figure 3.22.

\[
\begin{bmatrix}
  V_j & V_j' & i_f \\
  j & +C_n & -C_n \\
  j' & -C_n & +C_n \\
  f & 1 & -1 \\
\end{bmatrix} = \begin{bmatrix} 1 \\ -1 \\ \ldots \\ \ldots \\ \ldots \end{bmatrix}
\]

(3.63)

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. \( i_f \) is current flowing through the faulty component. The faulty system with fault rubber stamp in matrix form is given as,

\[
\begin{bmatrix}
  A & c \\
  r & \Delta \\
\end{bmatrix} \begin{bmatrix}
  X_f \\
  \phi \\
\end{bmatrix} = \begin{bmatrix}
  Z \\
  0 \\
\end{bmatrix}
\]

(3.64)

where \( c \) and \( r \) are the additional column and row introduced corresponding to the faulty component. The additional column \( C \) is with values 1 and \(-1\) corresponding to the location of the faulty component and all other values are zero. The additional row \( r \) is the faulty component equation with its node voltages. The value of \( \Delta \) depends on the faulty component.
From Equation (3.64), it can be observed that a new variable called fault variable \( \phi \) is added as a new unknown variable. It can also be noted that this faulty variable \( \phi \) corresponds to the unknown branch current through the faulty component. As seen in equation (3.64), the circuit matrix \( A \) is retained in forming the faulty system equation without any modification in the values of it.

### 3.8.3 Fault Simulation Algorithm

Fault simulation procedure is shown in Figure 3.23 for both catastrophic and parametric faults begin by defining the number of faults. For each faulty component, the desired value is entered and this faulty condition is injected into the circuit matrix using fault rubber stamp as explained in Section 3.8.2. The faulty system equations are obtained as explained in Equation (3.64). This procedure is being continued for all the components considered to be faulty.

### 3.9 SUMMARY

Analog circuit simulation under fault free and faulty conditions based on modified nodal analysis and MNA stamps is explained in this chapter. The popular methods for electronic circuit analysis and choice of methods in developing computer algorithms for complex circuits are addressed. Importance of modified nodal analysis in automated analysis of electronic circuits is explained with circuit examples. MNA stamps of electronic components and their significance in developing system equations
Figure 3.23  Fault Simulation Algorithm

are explained with the aid of literature. Fault simulation process and fault simulation method based on fault rubber stamp has also been explained.