CHAPTER 2

LITERATURE SURVEY

2.1 INTRODUCTION

Analog circuits are electronic circuits that operate on continuous time and continuous magnitude signals called analog signals. Analog circuit testing and diagnosis are important objectives in design and maintenance of analog circuits. In fault diagnosis of analog circuits, testing is first performed to identify whether the circuit under test is faulty or not and diagnosis is performed to locate exact faulty components that cause the circuit to work out of its bounds. Many research works aim to develop methods or procedures to find the faulty component of a circuit. The requirements of fault diagnosis methods are the ability or applicability of the methods to identify faulty components both in linear and nonlinear analog circuits and suitable for locating both parametric and catastrophic faults. The test and diagnosis procedure is based on either simulation before testing or simulation after testing. Both SBT and SAT approaches require simulation tools to perform simulation of analog circuit under test under faulty and fault free conditions to obtain the circuit variables that describe the functionality of CUT. Efficient faults simulation is also another important topic in analog circuit fault diagnosis. Fault diagnosis is usually performed under AC or DC conditions and in time domain (Ahmed and Cheung 1994). Other important aspects of analog circuit fault diagnosis are test point selection, testable group selection and test frequencies selection in case of multiple frequency testing. This
chapter explains and highlights existing fault diagnosis methodologies with their limitations and special features.

2.2 CIRCUIT SIMULATION

Analog circuit simulation is a technique to verify the design of electronic and electrical circuits and systems before manufacturing. Circuit simulation combines mathematical modelling of electronic circuit elements or components, formulation of circuit equations that describe circuit behaviour and methods to find solution of circuit equations (Najm 2010). The basic elements of a circuit are resistors, capacitors, inductors and controlled sources such as voltage controlled voltage sources, voltage controlled current sources, current controlled current sources and current controlled voltage sources. Based on the nature of excitation, the simulation and analysis methods are classified as AC, DC and time domain analysis (Raghuram 1989).

2.2.1 Electronic Device Models

Electronic device modelling is a technique that creates models that describe the device behaviour in terms of voltage and current relationship. In practice, a common starting point for circuit simulation is to restrict the formulation to two-terminal elements. Hence multi terminal devices such as transistors are modelled as sub circuits with two terminal elements (Najm 2010). In general, electronic device models are classified as large signal and small signal models to explain the device characteristics under DC and AC conditions respectively. The popular device models for active components such as diodes and transistors are presented by Neamen (2006). The accurate model that explains forward characteristic of diode is exponential model. But the nonlinear nature of this model makes it the most difficult to use and require iterative procedures or techniques to solve the circuit equations. To
speed up the analysis process simpler models like Piecewise-Linear model and Constant-Voltage-Drop models were developed (Sedra and Smith 1998). The current and voltage relationship in a bipolar junction is described by Ebers-Moll model. It is a composite model that can be used to predict the operation of the device in all of its possible modes (Sedra and Smith 1998; Boylestad 2012). These models with complete mathematical equations are described in chapter 3.

### 2.2.2 Network Equations Formulation

A circuit or network is a system consisting of set of elements connected to nodes. In circuit simulation, set of equations that express the circuit characteristics or functionality are to be derived to understand the behaviour of it. In computer based simulation, the equations are to be formulated automatically in a simple way. Techniques have been developed for automatic formulation of circuit equations to formulate circuit equations from the circuit description input file which introduces contribution of each element (Litovski and Zwolinski 1997). The methodologies available for circuit analysis are mesh and nodal analysis. In mesh analysis, Kirchhoff’s Voltage Law (KVL) is used in developing network equations and in nodal analysis; Kirchhoff’s Current Law (KVL) is used in formulating network equations. The nodal analysis is found to be a best method for automatic formulation circuit equations in computer simulation. This is because, the circuit equation formulation procedure is simple and for circuits with resistors and independent current sources the nodal admittance matrix is diagonally dominant which results in good accuracy in solution. And also active devices tend to behave as current sources; nodal analysis is popular in simulation based circuit analysis (Litovski and Zwolinski 1997). The modified form of nodal analysis is introduced in computer based simulation methods though it leads to larger matrices (Vlach 2014), to overcome the limitation of nodal
analysis in handling voltage sources in between two nodes and independent current sources (Thulasiraman 2005; Rajan 2005). The modified nodal analysis is well suited for symbolic and numeric analysis of complex circuits using modern matrix-based simulation tools. The simplicity of incorporating into the matrix equations all types of passive and active circuit elements is demonstrated and examples were illustrated by Wedepohl and Jackson (2002). The matrix representation of linear equations in circuit analysis and matrix based system equation formulation procedure for computer based simulation is explained by Gottling (1994). Each element or components of an electronic circuit in modified nodal based automatic formulation of circuit equations is characterized by distinct patterns called stamps. Detailed explanation about Modified nodal analysis based computer simulation using MNA stamps is presented in chapter 3.

2.2.3 Network Equations Solution

Analog circuit simulation with device models describing device characteristics and equations formulation using circuit analysis methods finds the solution of circuit equations by solving it developing suitable approaches or algorithms. The main aspects in selecting or developing algorithms for solving the system of equations are the speed and accuracy. This is achieved by decreasing the amount of computation (Litovski and Zwolinski 1997). Solutions techniques to solve linear and nonlinear system equations are presented and explained by Najm (2010). Two popular methods called direct and indirect methods are explained by Najm (2010) to solve linear circuit equations. The direct methods are based on Gaussian Elimination and its variants such as LU decomposition and solve the systems in a fixed number of steps. Indirect methods are iterative techniques that approach solution by gradually improving accuracy. These methods are based on Gauss- Jacobi, Gauss Seidal and Conjugate Gradient. In case of circuits with nonlinear
elements, network equations are formulated as system of nonlinear equations. The practical approach in solving nonlinear equations is to linearize them and solving these linear equations. Newton Raphson and simply Newton’s method is the heart of practical nonlinear solvers and it is the basis for modern techniques (Najm 2010). Newton Raphson is an iterative technique that solves the nonlinear system of equations by linearizing through Taylor series approximation. The detailed step by step procedure with algorithmic representation of Newton Raphson approach is explained in Chapter 3.

2.3 ANALOG CIRCUIT TESTING AND FAULT DIAGNOSIS

Fault diagnosis of analog circuits is performed in three stages to solve three important problems such as fault detection to identify the CUT is faulty or not, fault location to identify the faulty components and parameter evaluation to find how much is the deviation from the nominal value (Starzyk, Janusz et al. 2000). There are two important fault diagnosis techniques called simulation before testing and simulation after testing among which fault dictionary approach of simulation before testing is popular. In fault dictionary approaches, efficient fault simulation, proper choice of stimulus (Schreiber 1979), selection of test measurement and fault isolation determines efficiency of the proposed methods (Rao and Sundari 2014).

2.3.1 Fault Simulation in Linear and Nonlinear Analog Circuits

The complex nature of analog circuits and difficulty in fault modelling, analog circuit fault simulation is not successful as its digital counterpart. A novel approach to this problem is proposed by Nagi et al. (1993) by mapping the good and faulty circuits to the discrete Z-domain. An efficient fault simulation is then performed on this discretized circuit for the given input test wave form. A hierarchical fault modelling approach for both
parametric and catastrophic faults is proposed by Nagi and Abraham (1996) which includes both ac and dc faults in passive as well as active components. The fault models are based on functional error characterization. Efficient fault simulation method based on fault rubber stamp is proposed by Augusto, JS and Almeida (2000). Fault rubber stamp methodology is based on MNA stamps and the approach is tested in ac circuits by Veiga et al. (2005). But fault rubber stamp methods introduce one additional equation for each faulty condition which leads to larger number of circuit equations to be solved. The proposed approach uses modified nodal analysis for circuit simulation and therefore fault simulation based on fault rubber stamps is found to be good choice for implementation of different faulty conditions and simulation of faulty circuits.

Yang, C et al. (2013) proposed a complex-circle based fault model. This approach has been improved by optimal test frequency selection (Yang, C et al. 2014) and fault location (Tian et al. 2014). A two dimensional fault model based on collaborative analysis of supply current and voltage is proposed by Hu et al. (2015). This model is a family of circle loci on the complex plane, and it simplifies greatly the algorithms for test point selection and potential fault simulations, which are primary difficulties in fault diagnosis of analog circuits. Furthermore, in order to reduce the difficulty of fault location, an improved fault model in three- dimensional (3D) complex space is proposed, which achieves a far better fault detection ratio against measurement error and parametric tolerance. Analog circuit fault simulation using Pspice engine is proposed by Wang et al. (2015). The method triggers faults by two approaches called substitution method and equivalent circuit method. The simulation framework automatizes the process of fault simulation acquisition by fault model libraries. But this approach requires creation of fault model libraries and it is found to be suitable for catastrophic faults.
Efficient fault simulation using piecewise linear modelling of nonlinear devices in nonlinear circuits is reported by Lin and Elcherif (1985). The linearized circuit equations are formed by conventional linear circuit analysis. Prasad (1990) modelled the circuits with nonlinear devices as a linear multiport terminated by nonlinear elements and the equations of the faulty circuit are written by applying the modification formula to a matrix depending only on linear elements. But the solutions to the nonlinear reduced circuit equations are not discussed.

Augusto, JS and Almeida (2000) discussed an efficient fault simulation method based on fault rubber stamp. The circuit equations are solved using Newton Raphson approach. The electrical characteristic of nonlinear devices is linearized through Taylor series approximation and in each iteration the linear circuit equations must be solved. As this process increases simulation time, the authors developed new Newton Raphson model for electronic active or nonlinear components. Nonlinear devices are modelled as current controlled devices and current through the device is introduced as a new circuit variable and iterative dependent blocks are moved to the lower right most columns of circuit matrix. This reduces the simulation time because only the lower right most columns are to be computed in each iteration. The proposed work uses these electronic models to simulate faults in nonlinear analog circuit. This procedure has been explained in Chapter 3.

Efficient fault simulation in nonlinear analog circuits is addressed by Shi et al. (2006) and two methods called one step relaxation and adaptive simulation continuation are proposed. One step relaxation approach obtains approximate solution for a faulty circuit by one step Newton Raphson with faulty free solution as initial guess and adaptive simulation continuation method uses the solution obtained from first faulty circuit as initial guess for the second faulty circuit. An efficient method for simulation of multiple
catastrophic faults in linear AC circuits is reported by Tadeusiewicz and Hałgas (2010). The faulty elements are either open circuits or short circuits. The method exploits the well-known Householder formula in matrix theory to find the node voltages deviations due to the perturbations of some circuit elements.

### 2.3.2 Test Point Selection Approaches

Test point selection or test node selection is the process of identifying measurement nodes for testing and fault diagnosis. The objective of test point selection approaches is to identify few measurement nodes to detect all potentially faulty components uniquely so that the test cost, test time and size of fault dictionary are reduced. An efficient way of determining the test nodes based on inclusion and exclusion methods have been proposed by Prasad and Babu (2000). A test node is selected using fault wise integer coded table of the test circuit without affecting diagnosing capabilities. An efficient method to select an optimum set of test points for dictionary techniques in analog fault diagnosis is proposed by Starzyk, Janusz et al. (2004) and is based constructing the two-dimensional integer-coded dictionary whose entries are measurements associated with faults and test points. Optimum test points are selected by selecting the columns that isolate the rows of the dictionary. Then, the likelihood for a column to be chosen based on the size of its ambiguity set is evaluated using the minimum entropy index of test points. Finally, the test point with the minimum entropy index is selected to construct the optimum set of test points. In order to select the optimum test points of analog circuits, a method based on fuzzy theory and ant colony algorithm is proposed by Chao-jie et al. (2008). The traditional ant colony algorithm model was updated for test point selection of analog circuits. An accurate fault-pair Boolean table technique for the test point selection problem is explained by Yang, C et al. (2010a) which is based on integer coded table technique.
Jiang, R et al. (2010) introduces heuristic technique based on discrete particle swarm optimization (DPSO) and multidimensional fitness function (MDFDPSO). To radically reduce the search space Cui and Wang (2010) proposed support vector machine based approach. The problem of near optimum test points set selection for analog fault dictionary is considered by Yang, C et al. (2010b). This problem is formulated as a depth-first graph search problem and the test point selection progress is transformed to a graph node expanding progress. The proposed graph search method guarantee a maximum information increase of desired test points set by adding a test point to the set each time, to achieve global minimum test points. Pułka (2011) proposed two heuristic approaches based on optimization techniques based on expert system. This approach finds the set test points based on identification of state of unique fault detectability. A novel test-point selection approach based on slope model that describes voltage relationship between two nodes is proposed by Yang, C et al. (2011). A procedure for selecting appropriate test points, employing some evolutionary techniques, is developed by Tadeusiewicz et al. (2012). The approach is suitable for linear and nonlinear analog circuits.

A sensitivity vector based test point selection method is proposed by Li, Y et al. (2013) and is used to build diagnosis equations. The condition number of diagnosis equations is used in finding test nodes and work proved that the condition number of a matrix is bigger than the maximum row norm ratio. To minimize the computational cost, the approach minimizes the maximum row norm ratio in node selection procedure. Gao, Y, Yang, C, et al. (2014) reported a heuristic graph search method to facilitate the test point selection process. First, the information theoretic concept of entropy is used to evaluate the optimality of test point. The entropy is calculated by using the ambiguous sets and faulty voltage distribution, determined by component tolerance. Second, the selected optimal test point is used to expand current
A new test point selection method is proposed by Zhao and He (2015) and is based on an accurate way for determining the fault ambiguity gap to calculate the isolation probability of the faults. The proposed fault-pair isolation table derived from the mean and standard deviation values of node voltage exactly represent the fault-pair isolation capability of the test points. The special test points that can uniquely isolate some particular fault pairs are selected first to save the total cost of the computation time and to find the final solution directly. More number of optimum test points is selected from the normalized fault-pair isolation probability values in the table are used to select the right test point that has the largest fault-pair isolation capability among all the candidate test points.

2.3.3 Testable Components Selection Methods

A procedure for the determination of an optimum set of testable components in fault diagnosis of analog linear circuits is presented by Fedi et al. (1999), and is based on the testability evaluation of the circuit and on the determination of the canonical ambiguity groups. A numerically efficient approach to identify complex ambiguity groups for the purpose of analog fault diagnosis in low-testability circuits is proposed by Starzyk, Janusz et al. (2000). The approach uses a numerically efficient QR factorization technique to identify ambiguity group. An efficient approach for ambiguity group determination in low-testability analog linear circuits is presented by Manetti and Piccirilli (2003). It is based on the use of the singular-value decomposition of the testability matrix of the circuit under test, and permits to determine canonical ambiguity groups.
A symbolic procedure for ambiguity-group determination, based on the a priori identifiability concept, is proposed by Cannas et al. (2010a). To select potential canonical ambiguity groups, the method performs the analysis of the occurrence of circuit parameters in the coefficients of the input/output relationship. A procedure for ambiguity group determination both in linear and nonlinear circuits is proposed by Cannas et al. (2010b) and it is based on the a priori identifiability concept which greatly reduces the computational complexity of the evaluation of canonical ambiguity groups. The identifiability of the circuit under test is investigated analyzing the coefficients of the Input-Output relationship. A new method of low-testability fault diagnosis for analog circuits is proposed by Han, H and Wang (2012). The transfer relation between test nodes and inputs of a circuit is computed based on the topological structure and the information of finite test points of the circuit. The diagnosability of each component in the circuit is analyzed qualitatively to classify diagnosable component groups of the test circuit, effectively avoiding any invalid diagnosis of inseparable components. Fault classification is carried out by Support Vector Machine that adopts chaos particle swarm optimization to effectively improve the accuracy of fault diagnosis.

Rao and Sundari (2014) proposed a method to find testable groups by ambiguity group identification. Ambiguity groups of CUT are determined by measuring voltage gain for nominal and faulty conditions. A fault dictionary is built with the voltage gain measurements and set of faults which have same measurements are separated and are set to form ambiguity sets.
2.4 FAULT DIAGNOSIS METHODS FOR LINEAR AND NONLINEAR ANALOG CIRCUITS

Fault diagnosis methods in linear and nonlinear analog circuits are used to identify faulty components of CUT. Diagnosis methods are developed to detect both parametric variations and topological variations. The important feature to be considered in fault diagnosis is the tolerance limits of components of circuit under test which limit the practical possibility of proposed methodologies. This section shows some of the methodologies developed to diagnose linear and nonlinear analog circuits.

2.4.1 Parametric Fault Diagnosis

In linear analog circuits, the voltage equation between two nodes is linear and can be expressed by a point-slope-form equation. The point in point-slope-form equation is determined by the nominal voltage values on the two selected nodes, and the slope is used as the fault model. The parameter tolerances taken into account and it influence the fault diagnosis by shifting both the point and the nominal slope value (Yang, C et al. 2011) and the approach is suitable for linear and nonlinear analog circuits. A method to identify single faulty components, based on test vectors, which are derived from the knowledge of circuit components location and values, is proposed by Augusto, JAS and Almeida (2008). This approach is suitable for single parametric faults identification in linear analog circuits. The proposed approach in this research is based on this test vector approach but to locate multiple faults both in linear and nonlinear analog circuits and to improve the practical possibility of the approach, test vectors are generated for upper and lower bound tolerance limits of components of CUT. Multi-fault diagnosis for analog circuits based on support vector machine (SVM) usually used a single feature vector to train all binary SVM classifier. Each binary SVM classifier
has different classification accuracy for different feature vectors. An optimal or near-optimal feature vector selection problem has been discussed by Long, et al. (2012a) which is based on Mahalanobis distance for diagnostics of analog circuits using the least squares SVM (LS-SVM). A method enabling us to detect and identify the hard faults, taking into account the deviations of the circuit parameters within their tolerance ranges, is developed by Tadeusiewicz et al. (2012). This method exploits an appropriate fault dictionary. The fault dictionary is used only for preliminary identification of the faults, because it is based on the analysis of the circuits with nominal parameters. A verification procedure based on the linear programming approach is proposed that leads to the results considering the component variations within their tolerance ranges. Continuation method based multiple soft fault diagnosis of nonlinear circuits is proposed by Tadeusiewicz and Hałgas (2012) and an efficient procedure for tracing a homotopy path is developed to locate faults. A mathematical model based normalisation algorithm to reduce the dimension of the fault samples and to improve the accuracy and efficiency of fault diagnosis is proposed by Huang and Yao (2015). Regarding to the complexity and diversity of analog circuit fault, a principal component analysis, particle swarm optimization and support vector machine analog circuit fault diagnosis method is presented by Sun et al. (2013). It uses principal component analysis and data normalisation as pre-processing, then reduced dimension faulty feature is put into support vector machine for diagnosis and particle swarm optimization is used to optimize the penalty and kernel parameters of SVM that improve the recognition rate of fault diagnosis.

An intelligent fault diagnosis system based on artificial neural network is developed by Zhou et al. (2013). The system is based on learning vector quantization (LVQ) which requires no normalization and other pre-processing of training samples thereby reducing training time of neural networks. A new fault modelling method based on the location information of
components and the fault free components, applicable to both hard and soft faults detection is developed by Yang, C et al. (2013). The tolerance influences the fault diagnosis by shifting the fault free output voltage and distorting it. Minimal distance approach is used to find the faulty component. A method of testing for parametric faults in analog circuits based on a polynomial representation of fault-free function of the circuit is presented by Kumar and Singh (2013). The response of the circuit under test (CUT) is estimated as a polynomial in the root mean square (RMS) magnitude of the applied input voltage at a relevant frequency or DC. The test then classifies the CUT as fault-free or faulty based upon a comparison of the estimated polynomial coefficients with those of the fault-free circuit. Unexpected circuit failures in such systems during field operation can have severe implications. To address unexpected circuit failures in analog circuits, Sarathi Vasan et al. (2013), developed a method for detecting faulty circuit condition, isolating fault locations, and predicting the remaining useful performance of analog circuits. Through the successive refinement of the circuit's response to a sweep signal, features are extracted for fault diagnosis. The fault diagnostics problem is posed and solved as a pattern recognition problem using kernel methods. From the extracted features, a fault indicator (FI) is developed for failure prognosis. Furthermore, an empirical model is developed based on the degradation trend exhibited by the FI. A particle filtering approach is used for model adaptation and RUP estimation. A distance algorithm based fault diagnosis using fault dictionary method is presented by Zhang et al. (2014). The approach uses distance algorithm which is based on Euclidean distance to calculate the similarity between circuit under test and every state of fault dictionary.

A method based on principal component analysis of pre-treatment and particle swarm hybrid neural network is proposed by Huang and Han (2014). Multiple soft fault diagnosis of nonlinear analog circuits
comprising bipolar transistors characterized by the Ebers-Moll model is proposed by Tadeusiewicz and Hałgas (2014). The proposed diagnostic method exploits a strongly nonlinear set of algebraic type equations, which may possess multiple solutions, and is capable of finding different sets of the parameters values which meet the diagnostic test. The equations are written on the basis of node analysis and include DC voltages measured at accessible nodes, as well as some measured currents. The unknown variables are node voltages and the parameters which are considered as potentially faulty. To solve the set of equations the block relaxation method is used with different assignments of the variables to the blocks and corrected using Newton-Raphson algorithm. A DC analysis approach for analog fault dictionary development and testing has been proposed by Hochwald and Bastian (1979).

An analog circuit soft fault diagnosis method using Rényi’s entropy is proposed by Xie et al. (2015). This method uses Lagrange multiplier with Renyi’s entropy to estimate probability density function of the output of the circuit under test. The divergence between the Rényi’s entropy corresponding to the fault and fault free circuits is adopted to detect single and multiple parametric faults. To improve the diagnosis accuracy of analog circuit, a second map support vector data description (SM-SVDD) method is discussed by Jiang et al. (2015). The approach uses an anomalous and close surface instead of a hype sphere to describe the target data. The fault classifier is constructed by a SM SVDD algorithm to realize analog circuit fault diagnosis.

2.4.2 Hard Fault Diagnosis

Hard faults are open and short circuit faults. These faults cause a complete variation in circuit performance and are easy to detect (Milor and Visvanathan (1989). Hence most of the research proposals are for parametric
faults detection and some approaches are applicable for both hard and soft faults (Han, B et al. 2013). Approaches specific to hard fault diagnosis are highlighted here. Kalman filter based method for diagnosing both parametric and catastrophic faults in analog circuits is presented by Li, X et al. (2013). Kalman improve the efficiency of diagnosing a fault through an iterative structure, and the Shannon entropy to mitigate the influence of component tolerance.

A novel method to estimate the influence of hard-fault in linear-analogue circuit system based on the measurement of voltage phasor with assistant branch is introduced by Gao, X et al. (2013) ; Gao, X et al. (2014). A new fault diagnosis method of analog circuits is proposed by He, H et al. (2014). The method is based on Volterra series and SVM. A new fault diagnosis strategy based on the voltage phasor modelling is also established, and the tolerance influence on the corresponding voltage measurement is also discussed. Besides, it can be also applied to ambiguous groups and the sensitive test-frequencies determination in the process of fault diagnosis. Simulation-before-test approach based hard fault detection is used by Tadeusiewicz, Kuczyński, et al. (2015). To build a fault dictionary, a diagnostic test is arranged based on DC analysis. The proposed approach traces large number of nonlinear multivalued input–output characteristics at different values of circuit parameter within their tolerance ranges. Multiple parametric fault diagnosis using the simulation after test approach as well as detection and location of single catastrophic faults, using the simulation before test approach is proposed by Tadeusiewicz, Hałgas, et al. (2015) and the approach is based on homotopy.
2.5 MULTIFREQUENCY TESTING

Multifrequency testing is an analog circuit test and fault diagnosis procedure in which CUT is simulated with multiple frequencies and corresponding nodal variables are measured to acquire more information about the faulty conditions as well as to locate faulty components. This technique is popular when the CUT has few accessible nodes or measurements for testing or when testing is performed with few measurements (DeCarlo and Rapisarda 1988). But this increases computational time and test cost because for a faulty condition, measurements have to be taken for all the test frequencies. Hence to reduce simulation cost, number of test frequencies and the desired test frequencies are to be finalized before testing.

2.5.1 Test frequency Selection

A new procedure for the selection of test frequencies in parametric fault diagnosis of analog circuits is presented by Grasso et al. (2007) and is based on the evaluation of algebraic indices, as the condition number and the norm of the inverse, of a sensitivity matrix of the circuit under test. This matrix is obtained starting from the testability analysis of the circuit. A test index that permits the selection of the set of frequencies that better leads to locating parametric faults in analog circuits is defined.

The fault diagnosis problem for a linear system whose transfer function matrix is measured at a discrete set of frequencies is formalized by Sen and Saeks (1979). A measure of solvability for the resultant equations and a measure of testability for the unit under test is developed. These, in turn, are used as the basis of algorithms for selecting test points and test frequencies. A maximum sensitivity based test frequency selection approach is introduced by Zheng and Wu (2012). An efficient approach for selecting test frequencies in
analog circuits testing is proposed by Wang et al. (2015). Sensitivity analysis is used to generate test frequencies in multifrequency testing.

The approach selects the frequency band in which the fault has maximum sensitivity using particle swarm optimization. The approach selects minimal test frequency set by multi objective optimization. Rao and Sundari (2014), presented a method to select optimal test frequencies with the condition that the test frequency set should consist at least one frequency below the lowest non-zero break frequency and one between the successive break points. Several test frequencies are selected near break points corresponding to complex critical frequencies.

### 2.5.2 Multifrequency Fault Diagnosis

Long et al. (2012b) projected two kinds of feature vectors from frequency response data of a filter system to train least squares SVM (LS-SVM) to diagnose faults. Neural network based fault diagnosis in analog circuit using Polynomial Curve Fitting is proposed by Kumar and Singh (2013) and it covers faults as small as 10% or less. A polynomial of suitable degree is fitted to the output frequency response of an analog circuit. The coefficients of the polynomial attain different values under faulty and non-faulty conditions. Using these features of polynomial coefficients, a BPNN is used to detect the parametric faults. A complex field modelling method is presented by Yang, C et al. (2013). This fault modelling method is applicable to both hard and soft faults. It is also applicable to either linear or nonlinear analog circuits. The parameter tolerance is taken into consideration. A frequency selection method is proposed to maximize the difference between the faults fault signature. Hence, the aliasing problem arise from tolerance can be mitigated. The minimization of number of test frequencies necessary to detect all possible faults in a multi-frequency test approach for linear analog
circuits can be modelled as a set covering problem. An interval graph formulation is used and a polynomial algorithm using the interval graph structure is suggested by Bentobache et al. (2013). A multifrequency test approach based on pole sensitivity approach is proposed by Rao S.P (2013). An analog fault diagnosis approach using a systematic step-by-step test is developed by Peng et al. (2013) for fault detection and location in analog circuits with component tolerance and limited accessible nodes. First, by considering soft faults and component tolerance, statistics-based fault detection criteria are established to determine whether a circuit is faulty. For a faulty circuit, fuzzy fault verification is performed using accessible node voltages. An approximation technique is used to identify the most likely faulty elements with a limited number of circuit gain measurements at selected frequencies. A synthetic decision is made to locate faults according to the results of fault verification and estimation. An efficient approach for diagnosing faults in analog circuits based on the advantages of both multifrequency test and NNs is projected by Wang et al. (2015). Multifrequency test vectors are generated by sensitivity analysis. Fault features of the test point in CUT are extracted and fused. NNs are used to classify the features in a variety of state for the detection and location of faulty components in CUT.

2.6 COMPARISON OF EXISTING METHODS

Table 2.1 shows the merits and demerits of existing fault diagnosis methodologies.

Table 2.1 Comparison of Existing Fault Diagnosis Methods

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<th>Research Paper</th>
<th>Method Used</th>
<th>Merits</th>
<th>Demerits</th>
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<tbody>
<tr>
<td>Yang, C, Tian, S, Long, B and Chen, F 2011, 'Methods of handling Slope based fault modeling</td>
<td>Suitable for linear and</td>
<td>Only single soft fault is</td>
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<tr>
<td>Zhou, SG, Li, GJ, Luo, ZF and Zheng, Y 2013, 'Analog Circuit Fault Diagnosis Based on LVQ Neural Network', in Applied Mechanics and Materials, vol. 380, pp. 828-832</td>
<td>Linear Vector Quantization Neural Network</td>
<td>No need of normalization and preprocessing of training samples. Hence lesser training time</td>
<td>Hard faults are not detected</td>
</tr>
<tr>
<td>Zhang, YJ, Hou, JJ and Huang, L 2014, 'Fault Diagnosis of Analog Circuits with Tolerance'</td>
<td>SBT approach based on Distance algorithm and</td>
<td>Component tolerances taken into account</td>
<td>Higher Computational Time in building fault</td>
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<tr>
<td>Author(s)</td>
<td>Title</td>
<td>Methodology</td>
<td>Results</td>
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<tr>
<td>Huang, G and Han, BR</td>
<td>'Analog Circuit Fault Diagnosis Based on Principal Component Analysis of Pretreatment and Particle Swarm Hybrid Neural Network', in Applied Mechanics and Materials, vol. 494, pp. 809-812</td>
<td>PCA and Particle Swarm Hybrid Neural Network</td>
<td>Complexity of calculation is reduced by PCA, Hard faults are not detected</td>
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<tr>
<td>Tadeusiewicz, M and Hałgas, S</td>
<td>'Multiple soft fault diagnosis of BJT circuits', Metrology and Measurement Systems, vol. 21, no. 4, pp. 663-674.</td>
<td>Block relaxation and Newton Raphson Methods</td>
<td>Multiple soft faults are detected</td>
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<td></td>
<td></td>
<td></td>
<td>➜ Hard Faults are not detected ➜ Applicable to non linear circuits</td>
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<tr>
<td>Xie, X, Li, X, Bi, D, Zhou, Q, Xie, S and Xie, Y</td>
<td>'Analog Circuits Soft Fault Diagnosis Using Rényi’s Entropy', Journal of Electronic Testing, vol. 31, no. 2, pp. 217-224</td>
<td>Lagrange Multiplier with Rényi’s entropy</td>
<td>Single and Multiple soft faults are detected, Hard faults are not detected</td>
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<tr>
<td>Jiang, Y, Wang, Y and Second Map</td>
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<td>Second Map</td>
<td>Better diagnosis</td>
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<tr>
<th>Support Vector Data Description method</th>
<th>accuracy</th>
<th>not detected</th>
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<th>SAT approach</th>
<th>Faults detection of circuits with micrometer and sub-micrometer transistors</th>
<th>Hard faults are not detected</th>
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<td>Multiple soft faults are detected</td>
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<th>Fault Dictionary method</th>
<th>Circuits with multiple DC solutions are considered</th>
<th>Soft Faults are not detected</th>
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<td>Higher computational time in building fault dictionary</td>
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From Table 2.1, it can be observed that the approaches are useful in detecting either soft faults or hard faults. It can also be observed that the approaches are best suited either for linear or nonlinear analog circuits. Fault Dictionary based fault localization approaches use conventional method of developing fault...
dictionary which requires higher computational time. It can also be observed that the approaches propose solution to tolerance and faults detection and the other research challenges such as test node selection, testable group components identification are not addressed. That is, all these approaches require special approaches to resolve these challenges.

The proposed approach in this research work is suitable for linear and nonlinear analog circuits as well as parametric and catastrophic faults detection. Since test vectors are treated as fault dictionary, computational time required is greatly reduced than the conventional methods of fault dictionary. The proposed approach does not require special approaches to identify test nodes for testing and testable group determination as in the case of conventional approaches.

2.7 SUMMARY

Analog circuit testing and fault diagnosis methodologies proposed in the literature are projected in this chapter. The steps involved in analog circuit fault diagnosis are circuit simulation, fault simulation, test measurements evaluation and faulty identification. Circuit simulation tools developed or used for simulation of circuit under test must have capability to simulate faults efficiently. Efficient circuit simulation methods and choice of selection of those methods are listed in this chapter. Methodologies proposed for faults simulation are also reported. Other issues in analog circuit test and fault diagnosis procedure like test node selection, ambiguity group identification and test frequency selection in case of multi-frequency testing approaches are presented and contribution from various researchers in this domain and proposed methodologies has also been explained.