CHAPTER 1
INTRODUCTION

1.1 HISTORY AND TRENDS OF MOS TRANSISTOR

Nowadays, the growth of Electronic devices is increased dramatically with improvement in the performance of the devices. The development of the modern electronic devices began since 1925 where the first solid-state transistor was built up, which is metal-oxide-semiconductor field-effect-transistor (MOSFET). MOSFET is widely used for analog and digital circuits for example inverters, multiplexer, logic gates etc. Then, the analog and digital circuits are combined to form integrated circuits (ICs) that have been widely used either in low-power devices or high-power devices for example smart phones, laptops, sensors and etc which is commonly used for human application.

In day to day life, portable devices are needed because it is easy to use, and more effective than wired devices. An example of a portable device that can be seen commonly is the portable charger. It make easy to charge smart phone during travelling and reduce the electricity cost. The performances of these devices are very good and meet the requirements of today.

In this era of technological advancement, the development of electronic devices technology is very important and causing the difference of human lifestyle. The evolution or change in lifestyle causes people to acquire modern and superior performance of a device in term of speed, quality, low price product and low power consumption. Therefore, the electronic industries need to cover these challenge to meet the people requirements and by improving their product or produce the new superior products so that they can compete their
product in the market. Improving of a product can be done by adding the features of electronic devices so that it has more functionality such as smart watches, portable battery.


**Figure 1.1** The trend of increasing the number of microprocessor transistor through the year 1971 to 2011 according to the Moore’s Law as guidance

Recently, the INTEL Corporation has produced the latest processor which is 4th generation Core i7 processor. It consists of 1.4 billion of transistor in a single chip. The amazing performance and stunning visual are their advantages to compete the product in the market. The increasing number of transistor will show the performance and effectiveness of a device. By referring to the Figure 1.1 there is a trend of increasing the number of transistors per chip would quadruple every three years. This trend is called Moore’s Law developed
by the co-founder of Intel, Gordon Moore. Moore’s Law is used as the guidance to scale down the transistors. Until today, it remained relevant and became a benchmark for the future growth of semiconductor device.

Revolutions of electronic devices have entered into the nanometer scale regime known as nano electronic devices. The manufacture of extremely small size of transistor has become the focus of the researches to continue Moore’s Law. International Technology Roadmap Semiconductor (ITRS) 2000 as shown in Figure 1.2 has looks 10-15 years in the future, it becomes evident that most of the known technological capabilities will be approaching or will have reached their limits. Therefore, we can conclude that miniaturization of transistors will cause the limitations of a transistor and affects the performance of the devices. Now it becomes a challenge for reducing short channel effects. So, it becomes necessary to investigate “next transistor” to continue providing the computer, communication, consumer, and other electronics industries with more efficient building blocks.

Source: (http://semi-md.com/blog/2014/05/12/scouting-report-for-materials-at-end-of-the-road-2013-itrs/)

**Figure 1.2 ITRS 2000 table for the next generation of transistor**
Therefore, the innovation of transistor is the only method to overcome the scaling issues of a transistor. The innovation of transistors can be done by investigating new materials and development of new structures. By using new material such as GaAs, high k-dielectric, strained silicon may enhance the performance of devices by providing better gate control and improving short channel effects (SCEs). In addition to this, new structure of transistors such as GAA (Gate-all-around) transistor, FinFET, Triple Gate Transistor, SiNW tri-gate also improve the performance of device by faster the speed (increase mobility) and low power consumption. With the aid of TCAD tools, the researchers can explore the next transistor concept instead of the real fabrication process to test the feasibility features of transistors. Therefore, it shortens the product development time.

1.2 SCALING ISSUES

Scaling is the process of reducing or shrinking the dimension of the device while attempting to maintain the constant electrical characteristics. Scaling makes transistors smaller and more circuits can be fabricated within a small area of the silicon wafer and therefore resulting in cost effective. There are various approaches used for reducing the dimension of the MOS devices.

![Figure 1.3 The increasing number of transistors per chip with device technology](image-url)
The miniaturization of the conventional MOSFET has been accomplished with technology innovations and leads the device dimensions well into the nanometer era as shown in Figure 1.3. (Dennard et al 1974) introduced the constant electric field scaling approach. The electric field is kept constant and the scaled device is obtained by applying a dimensionless scale-factor $\alpha$ depending on the device variable, the parameter could be divided or multiplied by scaling factor $\alpha$.

The second approach used for reducing the dimension of the device is Constant voltage scaling. The applied bias $V_{DD}$ is kept constant and the scaled device is obtained by applying a dimensionless scale-factor $\alpha$. All the dimensions including the vertical to the device surface are scaled.

**Table 1.1 Technology scaling rules**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Constant Field Scaling</th>
<th>Constant Voltage Scaling</th>
<th>Constant Electrostatic Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Gate width</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Gate oxide</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Junction depth</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Doping density</td>
<td>$\alpha$</td>
<td>$\alpha^2$</td>
<td>$\alpha^2/\lambda$</td>
</tr>
<tr>
<td>Drain voltage</td>
<td>$1/\alpha$</td>
<td>$1$</td>
<td>$1/\lambda$</td>
</tr>
<tr>
<td>Drain current</td>
<td>$1/\alpha$</td>
<td>$\alpha$</td>
<td>$\alpha/\lambda^2$</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>$1/\alpha$</td>
<td>$1$</td>
<td>$1/\lambda$</td>
</tr>
<tr>
<td>Propagation delay time</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$1/\alpha$</td>
<td>$1$</td>
<td>$1/\lambda$</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Line current density</td>
<td>$\alpha$</td>
<td>$\alpha^3$</td>
<td>$\alpha^3/\lambda^2$</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>$\alpha^2$</td>
<td>$\alpha^2$</td>
<td>$\alpha^2$</td>
</tr>
<tr>
<td>Chip size</td>
<td>$1$</td>
<td>$1$</td>
<td>$1$</td>
</tr>
<tr>
<td>Power density</td>
<td>$1$</td>
<td>$\alpha^3$</td>
<td>$\alpha^3/\lambda^3$</td>
</tr>
</tbody>
</table>
The third approach is constant electrostatic scaling, where the scaled device is obtained by applying a dimensionless scale-factor $\alpha$. Here the potential of the device is scaled by the factor $\lambda = \alpha^{0.5}$. These generalized rules are shown in Table 1.1

### 1.2.1 Short Channel Effects

As device dimensions scale down to nanometer regime, the undesirable effects called “short-channel effects” start plaguing MOSFETs. That is the closeness between the source region and the drain region reduces the ability of the gate electrode, to control the potential distribution and the flow of current in the channel region. In other words, the Channel length $L$ is comparable to the depletion widths associated with the drain and source. The potential distribution in the channel depends on both the vertical electric field and lateral electric field. In general, the vertical electric field is greater than the lateral electric field at the channel region. This condition is no longer valid in the short channel devices and the drain potential has more influence on channel region than the gate potential. The two dimensional effects (vertical and lateral electric fields) results in an intolerable degradation of the subthreshold behavior, dependence of the threshold voltage on channel length and biasing voltages, and failure of current saturation.

The request for increasing performance and high packing density pushes the scaling process everyday closer to the physical limits of the silicon based MOS technology. However, the classical MOSFET is approaching its minimum channel length due to the limits imposed by short channel effects (SCEs), ultra-thin gate oxide tunneling, and higher channel doping. To further maintain the improvement in performance by scaling the device dimension, various technologies, such as mobility enhancement, metal gate with high dielectrics, optimal doping profile design, vertical channel transistor, etc., have been proposed. The vertical channel transistors with multiple surrounding gates
are found to possess inherently good suppression of short channel effects, high transconductance ($g_m$) and ideal Subthreshold Slope (SS). Also, they provide more effective suppression of OFF current ($I_{OFF}$) and enhanced ON current ($I_{ON}$). Figure 1.4 plots the evolution of transistor architecture from planar MOSFETs to ultrathin-body (UTB), Silicon-On-Insulator (SOI), Double-Gate (DG), Omega-Gate and Nanowire fin-type FETs (FinFETs).

Figure 1.4  **Evolution of transistor architecture from planar MOSFETs to UltraThin Body (UTB) structures**

Recent researches have reported a number of examples for nanowire fabrication and integration. In addition, the use of different shapes, lateral dimensions and materials like Si, Ge, GaAs are demonstrated. Among the various options, Silicon is still reported as the leading investigation material for semiconductor research.

Figure 1.5 shows the typical transfer characteristics of short and long channel devices (Muller 2003). It is clearly depicted that the OFF current shoots drastically in a short channel device. Also, various other problems like lowering of threshold voltage, large threshold variations with the applied drain bias,
reduced slope of transfer characteristics in the subthreshold region, etc., are all observed in short channel devices.

![Figure 1.5 Comparison of Transfer characteristics of a shortchannel (LG=32nm) MOSFET with a long channel (LG=250nm) MOSFET](image)

These unwanted phenomena are collectively termed as short channel effects and are need to be addressed to improve the performance of a MOSFET device.

1.2.2 Sub-threshold Swing (SS)

Sub-threshold swing (SS) is defined as the variation in the gate voltage required to have a variation in current. For a MOSFET, the following equation represents the sub-threshold swing (Taur 1998).

\[
SS = \left( \frac{kT}{q} \right) \times \ln(10) \times \left( 1 + \left( \frac{C_D}{C_{OX}} \right) \right)
\]  

(1.1)
where, \( T \) is the temperature in degree kelvin, \( q \) is the charge of the electron in coloumb, \( C_D \) is the depletion capacitance and \( Cox \) is the gate oxide capacitance in farads. Even if the second term is neglected \((Cox >> C_D)\), \( SS \) is limited by the first term to 60 mV/Decade. Higher \( SS \) allows the device to have a very few order of changes in drain current from the OFF state to the threshold voltage, which in turn results in a higher OFF current for a given threshold voltage.

1.2.3 **Drain Induced Barrier Lowering (DIBL)**

![DIBL diagram of MOS transistor](image)

**Figure 1.6 DIBL diagram of MOS transistor**

When a high drain voltage is applied to a short channel device, the barrier height of the device is very much lowered, such that it results in decrease of the threshold voltage. The point of maximum barrier is also shifted towards the source end of the device. This effect is called as Drain Induced Barrier Lowering (DIBL). This short channel effect is the main reason behind the increase of subthreshold current due to drain voltage in a short channel device.

The channel region is electrostatically shielded from the drain voltage in a long channel MOSFET. But in a short channel device, the potential barrier (Figure 1.6) of the source and drain side is controlled by both the gate-to-source voltage and the drain-to-source voltage. As the drain-to-source voltage increases, potential barrier from the source to the channel junction will be lowered by the depletion region under the drain. This reduction of barrier potential leads to
increase in the injection of electrons from source to drain region, even if the gate voltage has not reached the threshold voltage. The leakage current is called as the subthreshold leakage current of a MOSFET. Simultaneously, the device reaches the punch-through condition where the gate totally loses the control of the channel and high drain current passes through the device, independent of the gate voltage.

1.2.4 Channel Length Modulation

![Diagram of MOSFET with channel length modulations](image)

**Figure 1.7** Channel length modulations - as the drain voltage applied is above $V_{GS}-V_T$, the drain side of the channel is pinched-off

When the drain voltage is greater than the gate overdrive, a pinch off will occur at the drain end corresponding to a length of $L_G$ as shown in Figure 1.7. A variation in the drain current occurs, due to the effect of channel length modulation, and is given by:

$$I_D = I_{Dsat}/\left(1 - \Delta L_G / L_G\right)$$  \hspace{1cm} (1.2)

The variation of channel length has very less significance in a long channel device. But in a short channel device $L_G$ becomes much more significant and will always be a function of $V_{DS}$. This non saturation behavior of the device reduces the threshold voltage and hence the ON/OFF current ratio.
Here $V_{TH}$ is a strong function of $L_G$ and decreases significantly at less channel lengths. This is often termed in literature as Threshold Voltage roll off with $L_G$.

### 1.2.5 Gate Oxide Leakage

SiO$_2$ is a good insulator to be used in the MOSFET devices. But, when the thickness of the gate oxide is reduced less than 2nm, probability of device tunneling increases and results in an increased oxide leakage current. Using a high-k dielectric can provide a solution to this problem to an extent, reducing the direct tunneling leakage.

### 1.2.6 Velocity Saturation

At high electric fields, the velocity of carriers will become constant due to mobility saturation. A constant field scaling (i.e., scaling all parameters equally) can be employed to maintain the same electric fields in the scaled down transistor. However, the scaling trend followed by the semiconductor industry is not a constant field one. For example, oxide thickness is scaled more and supply voltages are scaled less. This results in an increased electric field in the Nanoscale MOSFETs. The velocity gets saturated as the field is increased. This would have been an issue of low significance if the saturation that occurs at drain voltages is greater than the gate overdrive. But, in a Nanoscale transistor, velocity saturation occurs at lower drain voltages itself, leading to a reduced ON current.

### 1.2.7 Gate Induced Drain Leakage (GIDL)

Scaling of a MOSFET devices results in an increased electric field in the oxide as well as in the gate-drain overlap region. With a high drain bias and a low gate bias applied to the device terminals, the electric field in the gate/drain overlap region is found to be very high. This results in the depletion of carriers in the drain overlap region as shown as Figure 1.8 shows the band diagram in the
vertical direction in the gate/drain overlap region. A significant band overlap between the valance and conduction bands of the drain in the overlap region is observed.

![Figure 1.8 Schematic showing the GIDL effect](image)

**Figure 1.8 Schematic showing the GIDL effect**

### 1.2.8 Hot Carrier Effects

The hot carrier degradation of an n-channel MOSFET is shown in Figure 1.9. A drift in the performance of device over a period of time is caused due to these hot carrier effects. There are three distinct possibilities of hot carrier injections occurring in a MOSFET.

- Carriers generated by impact ionization can result in a high substrate current
- Carriers having higher energy than the silicon/gate dielectric conduction band offset can lead to a conduction current at the gate.
- The silicon-gate dielectric interface can be damaged by high energy electrons resulting in degradation of device parameters like threshold voltage and drain current.

![Figure 1.9 The mechanism of hot carrier degradation in an n-channel MOSFET](image)

### 1.3 RECENT DEVICE STRUCTURES

In continuous efforts to improve the drive current and to achieve better control over the short channel effects, the planar single gate devices have evolved into advanced three dimensional device structures such as SOI Technology, Multi-gate MOSFETs, High Electron Mobility Transistors (HEMT) and Tunnel Field Effect Transistors (TFET). Different devices have been studied extensively as the ultimate solution for extremely scaled devices.

#### 1.3.1 SOI Technology

In a conventional MOSFET, the active elements of the device are located in a thin surface layer and are isolated from the silicon body by the p-n
junction depletion layer as shown in Figure 1.10 (a). The leakage current of this p-n junction exponentially increases with temperature, leading to a number of reliability issues. At high temperatures, excessive leakage current and high power dissipation reduce the performance of the devices considerably. Parasitic n-p-n and p-n-p transistors formed in neighboring insulating tubs that cause latch-up failures have been studied by (Toyabe & Asai 1979).

As the result of down-scaling process, the conventional bulk MOSFET transistor is reaching its limits in terms of device miniaturization and fabrication, Silicon-On-Insulator (SOI) technology has become a very attractive alternative to replace the bulk CMOS technology. It employs a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick layer of silicon oxide (hundreds of nanometers) as illustrated in Figure 1.10 (b). Latch up failures are avoided by dielectric isolation of components and reduction of various parasitic circuit capacitances. The manufacturing compatibility with the existing bulk silicon CMOS technology also represents a very important benefit of the SOI technology.

SOI MOSFETs are bound to operate either in Fully Depleted (FD) or Partially Depleted (PD) regimes depending on the thickness of the silicon layer. In Figure 1.11 (a), PD transistors are built on relatively thick silicon layers with
the depletion depths of the fully powered MOS channel shallower than the thickness of the silicon layer. When the channel depletion region extends through the entire thickness of the silicon layer, the transistor operates in a FD mode as shown in Figure 1.11 (b).

Figure 1.11 Cross Sectional View of (a) Partially Depleted and (b) Fully Depleted SOI CMOS Devices

The advantages of Fully Depleted SOI MOSFETs devices over Partially Depleted devices are listed below:
- Free from kink effect
- Enhanced subthreshold swing.
- Highest gain in terms of circuit speed, less power consumption and very high level of immunity to soft-errors.

1.3.2 Multi Gate MOSFETs

In classical bulk MOS devices, the gate controls the channel over one surface. But in multi-gate MOS devices, the gate controls the channel from many surfaces, which leads to high improvement over SCEs and device performance. The multi gate device structures include Double Gate (DG) MOSFETs, Triple Gate MOSFETs, Surrounding Gate (SG) MOSFETs, and Dual Material Surrounding Gate (DMSG) MOSFETs.
The first article on the Double Gate device structure was published by (Sekigawa and Hayashi 1984). They showed that significant reduction of short channel effects can be achieved by sandwiching a fully depleted SOI structure between two gate electrodes that were connected with each other. And also, the impact of the drain electric field on the channel was considerably reduced in this device structure.

In general, Double Gate (DG) MOSFETs (Figure 1.12) have two gates that control the charge in the thin silicon body layer and allow current flow for both the channels. DG MOS structure gives better control of the channel by using two gate electrodes, leading to mobility enhancement and very good immunity to short channel effects. Linking of the gate electrodes in a DG device leads to volume inversion in the silicon film and hence, the sub-threshold slope of DG MOSFET is ideal for very low doping applications. Another advantage of DG MOSFET is that the threshold voltage of the device is controlled by metal gate work function. The presence of back gate ensures high gate capacitance of the channel and better control over the channel potential, thus the leakage current $I_{OFF}$ is highly reduced. However, the manufacturing challenges like
maintaining a uniform Silicon channel thickness make the realization of a DG SOI MOSFET a difficult process.

The MIGFET (Multiple Independent Gate FET) is a double gate device in which the two gate electrodes are not connected to each other. Hence, they can be biased with two different gate potentials. The most important feature of a MIGFET is that the threshold voltage of one of the gates can be modulated by the bias applied to another gate, similar to the body effect in Fully Depleted SOI MOSFETs. These kinds of devices find their applications in the field of signal modulation.

Figure 1.13  Schematic diagram of Triple Gate MOSFET

Triple Gate MOSFETs (Figure 1.13), also called as the Tri Gate MOSFETs, and are considered as important candidates for prospective in VLSI, particularly for low power and high performance at 45nm CMOS technology. It is a non planar narrow transistor where the gates are wrapped around the silicon body. The two lateral channels as well as the top horizontal channel are controlled by the gates. The device represents a thin film consisting of narrow silicon island with gates on its three sides. The triple gate transistor is ideal for
using in Fully Depleted transistor applications. The electric field from the lateral sides of the gate exerts excellent control on the bottom side of the channel. Due to its SOI technology, the structure is compatible with conventional silicon integrated circuit processing. The drain current characteristics are improved and short channel effects are highly reduced in TG devices when compared to their DG counterparts.

Figure 1.14 (a) Schematic diagram and (b) Cross section view of surrounding gate MOSFET

The Surrounding Gate MOSFETs or Gate All Around (GAA) devices are considered as one of the most promising devices to reduce SCEs. GAA MOSFETs are similar in concept to triple gate MOSFETs except for the fact that the gate material surrounds channel region on all sides. The schematic diagram and cross section view of surrounding gate MOSFET is shown in Figure 1.14. Surrounding Gate MOSFET presents higher packing density, steep subthreshold
characteristics and higher current drive. In this device structure, the gate surrounds the silicon pillar completely and hence, the potential of the channel region is greatly controlled by the gate and short-channel effects can be greatly suppressed.

1.3.3 High Electron Mobility Transistors

Figure 1.15 Schematic diagram of high-electron mobility transistor

In a High-Electron-Mobility Transistor (HEMT), also called as Heterostructure FET (HFET), a junction between two materials with different band gaps is employed as the channel, instead of a doped region. When two different materials such as AlGaAs/GaAs are joined together or grown one over the other, while maintaining the same crystal structure, a hetero-structure is formed. The schematic diagram of HEMT is shown in Figure 1.15. The device operation is based on the high mobility electrons generated using highly-doped wide-band gap n-type donor AlGaAs layer and a non-doped narrow-band gap GaAs channel layer. The free electrons form a two-dimensional electron gas (2-DEG) due to the presence of a notch at the interface on the GaAs side. The transport properties of HEMT device are considerably superior to those of free electrons in a conventional Metal–Semiconductor Field Effect Transistor
(MESFET). HEMT device offers high electron mobility, small source resistance, high transconductance, high output resistance, reduced short channel effects and operate at higher frequencies than ordinary transistors. They find their applications in high frequency products such as cell phones, satellite television receivers, voltage converters and radar equipments.

1.3.4 Tunnel Field Effect Transistor

Figure 1.16 Schematic cross-section of n-channel TFET with indication of the tunneling junction

Tunnel Field Effect Transistor (TFET), shown in Figure 1.16, is a gated p-i-n diode that works in the reverse bias condition. In a normal MOSFET, the injection of carriers depends on the thermal injection. But in a TFET, the output current is determined by the Band-To-Band Tunneling (BTBT) of charge carriers between the source and channel in the device. Due to their lower leakage current and reduced SCEs, TFET devices are very much suitable for low power applications. As the BTBT region of the device in the source side is about 10nm, the device can be comfortably scaled down up to 20nm. The other significant advantages of TFET includes reduced subthreshold swing (<60mV/dec), higher speed of operation and reduced threshold voltage roll off. Also there is no punch-through effect in TFET due to its reverse biased p-i-n structure.

1.4 FUTURE PROSPECT: NANOWIRE TRANSISTORS

The Nanowire Transistor is one candidate which has the potential to overcome SCEs in SOI MOSFETs and has gained significant attention from
both device and circuit developers in recent years. The multi gate Nanowire Transistors show excellent current drive, provide an effective suppression of SCEs due to their improved gate strength, and also are compatible with conventional CMOS processes.

1.4.1 Overview

The discovery of carbon nanotubes (CNTs) by (Iijima 1991) have led to a great interest in the synthesis and characterization of other one dimensional (1D) structures like nanowires, nanorods and nanobelts. Nanowires of various inorganic materials have been synthesized and characterized in last few years. A nanowire is an object with a 1D aspect in which the width does not exceed a few tens of nanometers and the ratio of length to width is greater than 10. They represent the smallest dimension for efficient transport of electrons and excitons. Hence, they find their applications in nanoelectronics and nano-optoelectronics as interconnects.

1.4.2 Various Types and Advantages of Nanowires

**Table 1.2 Different types of nanowires**

<table>
<thead>
<tr>
<th>Types of Nanowires</th>
<th>Specific Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elemental</td>
<td>Ge, B, In, Sn, Pb, Sb, Bi, Se, Te, Au, Ag, Fe, Co, Ni and Cu</td>
</tr>
<tr>
<td>Metal Oxide</td>
<td>MgO, Al₂O₃, Ga₂O₃, In₂O₃, SnO₂, SiO₂, GeO₂, TiO₂, MnO₂, Mn₃O₄, CuₓO and ZnO</td>
</tr>
<tr>
<td>Metal Nitride</td>
<td>GaN, InN, Si₃N₄ and Si₂N₂O</td>
</tr>
<tr>
<td>Metal Carbide</td>
<td>BC and SiC</td>
</tr>
<tr>
<td>Metal Chalcogenide</td>
<td>CdS, CdSe, CdTe, PbS, PbSe, Bismuth, Chalcogenides, CuS, CuSe, ZnS and ZnSe</td>
</tr>
</tbody>
</table>

Nanowires can be prepared from metals, semiconductors, organic molecules, etc. and are used in various fields like mechanical, electronic, optical and medical applications. Henceforth, depending on the materials used for
synthesis, nanowires are classified as metallic nanowires, semiconductor nanowires and molecular nanowires. Table 1.2 summarizes the different types of nanowires together with their specific examples. Although a number of semiconductor nanowires are available, the silicon nanowires have become the prominent nanowires. This is because of their easy availability, the Si/SiO₂ interface is chemically stable, and silicon nanowires are utilized in a number of device demonstrations that have well known silicon technology based counterparts.

1.4.3 Electrical Properties of Nanowires

The impact of device dimensions on electrical conductivity of nanostructures is pretty complex to understand, as they are based on distinct mechanisms. These mechanisms can be broadly grouped into four different categories: surface scattering, quantized conduction, Coulomb charging, tunneling. In addition, the electrical conductivity of the nanostructures and nanomaterials are affected by increased perfection such as reduced impurity, structural defects and dislocations.

When the size of a material is less than the de Broglie wavelength, electric dipoles are formed due to the spatial confinement of electrons and holes. Also, discrete electronic energy levels are formed in all materials. In close resemblance to a particle moving inside a box, decreasing the dimensions of a device results in the increase of energy separation between the adjacent levels. In addition, the electron Density of States (DOS) depends on the dimensionality of nanostructures. Whereas for bulk systems a square-root dependence of energy prevails, a staircase behavior is a characteristic for 2D quantum well structures, spikes are found in 1D Quantum Wires (QWs), and discrete features appear in Zero Dimensional (0D) quantum dots.
The other mechanism that occurs in quantum wires is ballistic condition, when the length of the device is smaller than the electron mean free path. Here, each transverse waveguide mode or conducting channel contributes $G_0 = 2e^2/h = 12.9$ kW to the total conductance. Another important aspect of ballistic transport is that no energy is dissipated in the conduction, and there exists no elastic scattering. The later requires the absence of impurity and defects. When elastic scattering occurs, the transmission coefficients, and thus the electrical conductance will be decreased, which is then no longer precisely quantized. Finally, the tunneling conduction is a phenomenon that affects the electrical conductivity of the nanowires.

1.4.4 Nanowire Field Effect Transistors

Nanowire MOSFETs are considered to be excellent candidates for maintaining the relentless progress in scaling for semiconductor devices. Several things have contributed to the boom of research on nanowire transistors. First, they can be produced in high yield with reproducible electronic properties as per the requirements for Ultra Large Scale Integration (ULSI) applications. Second, “bottom-up” synthesized nanowire materials offer well controlled size in comparison with the “top-down” nanofabricated device structures; that is at or beyond the limits of lithography. Also, the crystalline structure, smooth surfaces and ability to produce radial and axial heterostructures can reduce scattering drastically. This results in higher carrier mobility in comparison with other nanodevices of similar size. Finally, the diameter (body thickness) of nanowires can be controlled down to well below 10nm. Therefore, even as the gate length is aggressively scaled, electrical integrity of nanowire based electronics can be sustained. This is a feature that could not be easily achieved in planar MOSFETs.

Silicon Nanowire FETs, unlike planar MOSFETs, have metal source and drain contacts. That is, the source and drain contacts are made from metals
instead of degenerately doped semiconductors. Due to this factor, positive Schottky barriers are formed at the metal/semiconductor interface due to the combination of metal work function and Fermi level pinning by surface states. As a result, the device performance is affected by physical contact properties to a large degree. Hence, application of annealing can lead to the formation of essentially ohmic contacts leading to increase in ON current and apparent carrier mobility.

Figure 1.17 Schematic diagram of Surrounding Gate Silicon Nanowire Transistor

Surrounding Gate Silicon Nanowire Transistors have attracted significant interest because of their excellent electrostatic integrity even at the nanoscale. Various types of nanowire transistors are being explored for future transistors replacing planar MOSFETs in logic and Dynamic Random Access Memory (DRAM) applications, and their fabrication is being studied. The schematic diagram of a Surrounding Gate (SG) Silicon Nanowire Transistor is shown in Figure 1.17.

1.4.5 Advantages of Nanowire Transistors over planar MOSFETs

Nanowire MOSFETs have several advantages as the candidates of main stream CMOS devices for the future. The ability to suppress short channel effects and hence the suppression of the OFF leakage current are expected to be very good, because of the surrounding gate configuration. Also, they are expected to have high ON current due to the following reasons.
• The nature of quasi 1D conduction of thin nanowires with small freedom of the carrier scattering angle; hence high conduction is possible.
• The use of multi-quantum channels for the conduction; the band structure of silicon nanowires is quite different from that of the bulk and many conduction sub-bands appear near the lowest sub-band. These sub-bands contribute to the conduction with increase in gate voltage.
• Multilayer nanowires can be implemented easily by utilization of Si/Ge multilayers.

1.5 CARRIER TRANSPORT

The carrier transport can be classified into three regimes: diffusive transport, quasi-ballistic transport, and ballistic transport. Nanowire Transistors can have gate length (Lg) is smaller than 0.1 µm. So, the carriers must traverse within Ballistic or Quasi Ballistic or Near Ballistic regimes.

1.5.1 Ballistic Transport

Injection of electron from source to drain without scattering to get ideal current is shown in Figure 1.18. Ballistic transport is the transport of electrons in a medium having negligible electrical resistivity caused by scattering. Without scattering, electrons simply obey Newton's second law of motion at non-relativistic speeds.

Figure 1.18 Ballistic transport
Ballistic transport is observed when the mean free path of the electron is (much) longer than the dimension of the medium through which the electron travels. The electron alters its motion only upon collision with the walls. Ballistic transport can be observed in a metal nanowire: this is simply because the wire is of the size of a nanometer (meters) and the mean free path can be longer than that in a metal.

1.5.2 Quasi Ballistic Transport

The presence of a small number of scattering basically characteristic the device operation in quasi ballistic transport and distinguishes it from that in ballistic transport which is shown in Figure 1.19. In simple, electron transport with scattering effects included is called as quasi ballistic transport.

However, carrier scattering is vital of quasi ballistic transport, and its effects must be measured if realistic devices properties are concerned. Introduction of scattering effects into ballistic modeling of a MOSFET can be described through KT-layer.

![Quasi ballistic transport](image)

**Figure 1.19 Quasi ballistic transport**

The carrier scattering within the region of the critical length neighboring source which is responsible for carrier backscattering is shown in Figure 1.20.
The elastic scattering and optical phonon emission is the dominant route of energy relaxation in the device. In an actual system with a large channel length, the presence of energy relaxation due to optical phonon scattering clearly changes the aspect of transport.

The elastic scattering plays an important role in a small system with a very short channel length, exemplified in nanoscale conductors. If energy relaxation is suppressed by some way or another, and yet the elastic scattering is emphasized in the system.

### 1.5.3 Elastic Scattering

Elastic scattering occurs when two or more particles collide without any loss of energy. This means that while the directions of the particles may change, the total kinetic energy of the system, or movement energy, is always conserved. The term elastic scattering is typically used in particle physics, which is the study of microscopic particles, but an elastic collision can also take place between macroscopic objects. An inelastic collision occurs when energy is lost during the collision.
1.5.4 Optical Phonon Emission

Transport of electrons in the conduction band of silicon is considered within the effective-mass approximation. There exist six minima in the conduction band, which can be grouped into three doubly degenerate valleys. Each valley will be labelled with an index $\nu = 1, 2, 3$. The case of both acoustic intra-valley and optical inter-valley scattering mechanisms will be presented.

In the case of acoustic intra-valley, phonon scattering is treated in the elastic approximation. It is important to recall that in the presented derivation of the phonon scattering self-energy functions a bulk model has been assumed for the phonon system as shown in Figure 1.21.

Electrons and holes are accelerated by the electric fields, but lose momentum as a result of various scattering processes. These scattering mechanisms include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections.

1.6 SCATTERING

Scattering is the general physical process where some forms of radiation, such as light, sound or moving particles, are forced to deviate from a
straight trajectory by one or more paths due to localized non uniformities in the medium through which they pass. Scattering may also refer to particle-particle collision between molecules, atoms, electron, photons and other particles.

A detailed chart of most of the imperfections that cause the carrier to scatter in a semiconductor is given in Figure 1.22 as

![Figure 1.22 Scattering mechanisms in a typical semiconductor](image)

Since the effects of all of these microscopic phenomena are lumped into the macroscopic mobilities introduced by the transport equations, these mobilities are therefore functions of the local electric field, lattice temperature, doping concentration, and so on. Mobility modeling is normally divided into: (i) low field behavior, (ii) high field behavior, (iii) bulk semiconductor regions and (iv) inversion layers. The high electric field behavior shows that the carrier mobility declines with electric field because the carriers that gain energy can take part in a wider range of scattering processes. The mean drift velocity no longer increases linearly with increasing electric field, but rises more slowly.

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### 1.6.1 Impurity Scattering

By impurities we mean foreign atoms in the solid which are efficient scattering centers especially when they have a net charge. Ionized donors and acceptors in a semiconductor are a common example of such impurities. The amount of scattering due to electrostatic forces between the carrier and the ionized impurity depends on the interaction time and the number of impurities. Larger impurity concentrations result in a lower mobility. The dependence on the interaction time helps to explain the temperature dependence.

The interaction time is directly linked to the relative velocity of the carrier and the impurity which is related to the thermal velocity of the carriers. This thermal velocity increases with the ambient temperature so that the interaction time increases, the amount of scattering decreases, resulting in a mobility increase with temperature. To first order the mobility due to impurity scattering is proportional to $T^{3/2}/N_I$, where $N_I$ is the density of charged impurities.

### 1.6.2 Surface-Roughness

The deviation in the direction of the normal vector of the real surface from its ideal form called as Surface Roughness variation which is shown in Figure 1.23. If these deviations are large, the surface is rough, if they are small, the surface is smooth. The electron mobility degrades monotonically with increasing surface roughness.
1.6.3 Surface-Roughness Scattering

Surface-Roughness scattering due to the asperity of the interface between the silicon substrate and the gate insulator (usually SiO$_2$) has been an important scattering mechanism in bulk MOSFETs, particularly in strong inversion, because the charge conduction in MOSFETs occurs in the vicinity of this imperfect interface.

As device scaling causes higher confining of fields at the interface, this process is expected to dominate device performance, even preventing the occurrence of ballistic transport. With respect to the physical modelling of the surface scattering, (Andrew’s 2010) approach has been regarded as the most comprehensive model available for both Monte Carlo simulations and mobility calculations.

Surface Roughness scattering (SRS) reduces the electron density of states in the channel, which increases the silicon nanowire transistor (SiNWT)
threshold voltage, and the SRS in SiNWTs becomes more effective when more propagating modes are occupied, which implies that SRS is more important in planar metal-oxide-semiconductor field-effect-transistors with many transverse modes occupied than in small-diameter SNWTs with few modes conducting. The SiNWT is attracting broad attention as a promising structure for future electronics. Therefore, understanding carrier transport in Si nanowire becomes increasingly important.

1.7 DEVICE MODELING

The characteristics of semiconductor materials and devices require a suitable means of describing their physical and electrical properties. Although experimental data can provide considerable information on the behavior of semiconductors under specific conditions, it is important to obtain information on processes that influence the experimental characteristics but cannot be directly observed. In addition to providing a general explanation of how this phenomenon occurs, it also explains a method to predict the device behavior. In order to achieve this level of understanding, it is necessary to produce some form of analogy which can describe the behavior of the device within the accuracy required for specified operating conditions. This process of interpretation by obtaining a suitable analogy of the proposed device is called modeling, and the description obtained is the model itself.

Semiconductor device models can be used to describe the terminal electrical properties of a device and the carrier transport processes which take place within the device. It is convenient to divide these models into two categories. These are physical device models and equivalent circuit models. Physical device models can be used to predict both terminal characteristics and transport phenomena. Equivalent circuit models are restricted to the electrical description of the device characteristics, although it is possible in many cases to relate the equivalent circuit model elements to the device physics.
Physical device models are based on a description of carrier transport physics. They can be used to characterize the DC, transient and AC operation of devices, in addition to providing a detailed insight into the physics of the device operation. An important advantage of this type of model is that it can be used to predict the characteristics of new devices, based on a suitable description of the carrier transport mechanisms. The principal limitation of the physical device models is that, currently, comprehensive models are usually implemented using large scale computer simulations that are dependent on substantial computer resources.

Equivalent circuit models are based on the electrical characteristics of the device. They are based on the association of electrical circuit elements with the device structure. The element values are obtained by attempting to fit the model’s terminal characteristics with measured data or by identifying the element’s electrical behavior with the physical characteristics of specific aspects of the device structure. These models are frequently used in electronic circuit design applications to compare devices of similar principles. They are very easy to implement and can be evaluated in a short period of time. Furthermore, the results can be immediately identified with electrical performance of the device. Regardless of these advantages, this modeling method does have its limitations. At higher frequencies, the models become too complex and it is difficult to equate the model elements with device parameters. Also, since the element values are dependent on bias, signal level and frequency, the models become increasingly nonlinear with signal level and frequency. Hence, due to these limitations, equivalent circuit models are of limited use predicting the characteristics of new devices without the support of experimental results.

It is important at this stage to distinguish between the terms ‘analysis’ and ‘simulation’. The analysis of a semiconductor device is normally taken to imply the task of characterizing the device that is carried out using some form of
mathematical representation that may be considered as a series of simplified stages which allows the required parameters to be extracted with a reasonable level of accuracy and in a relatively straightforward manner. Analysis usually involves the derivation and use of closed-form expressions which describe the device characteristics in an accurate manner. The simulation of a device is usually taken to be the process of representing the characteristics of the device by examining the operation of an analogous system. Hence, by providing a description of the device and its operating conditions, a simulation can predict how the actual device would behave. A severe interpretation of the term ‘simulation’ implies that the required information can be obtained without practical experimentation.

For the device model to be used in a circuit simulator, the following requirements should be satisfied:

- Over all regions of operation, the model should be so accurate to simulate actual device behavior.
- In transient analysis, calculations of drain current is carried out a countless number of time, hence, it is mandatory that the model should be both computationally efficient and accurate.
- The mathematical equations representing the device model must be continuous, with continuous first derivatives, so that any non convergence problems in the simulator can be avoided.

The combined requirement of computational efficiency and available memory restrict the device model for circuit simulators into the following three categories.

- Analytical Modelling
- Table Lookup Model
- Empirical Model
1.7.1 Analytical Modeling

There are basically two types of analytical models where model equations are directly derived from device physics. The charge sheet models proposed by (Brews 1978) are based on surface potential analysis, and are inherently continuous in all regions of operation of the device. The drive current can be accurately determined using these models, but the complexity of derived equations and the need for many number of iterations just to compute the surface potential for a given bias condition are the major disadvantages. (Kuo & Sum 1998) proposed another model which insisted on applying various approximations to the semiconductor equations based on decisions as to which physical phenomena dominate.

Thus, different analytically modeled equations are required to describe the different regions of operation of a device. These models are used to understand the first order device behavior in a fairly accurate manner and higher order effects can also be studied, by introducing physical and empirical parameters in the process. These models, usually referred as semi-empirical analytical models and are used to describe the relationship between the physical process, geometry structure and electrical behavior of a device. However, technology dependence and considerable time required to develop a model are the drawbacks of analytical modeling.

1.7.2 Table Lookup Model

A Table lookup model stores the device output current for different bias points and device geometries in a tabular form, and it has been discussed in detail by (Shima et al 1983 and Bischoff & Krusius 1985). The data base is collected from experimental devices or generated from device level simulators. These stored values are later used to compute the currents and conductance required by the simulator and this has been explained by (Bischoff & Krusius...
1985 and Barby et al 1988). These models are technology independent, need a very less storage area and have high model evaluation speed. However, these models provide very less physical insight into the device behavior.

1.7.3 Empirical Model

Empirical models do not account for the device physics but are modeled based on the curve fitting type device characteristics. These models have been discussed in detail by (Vogel 1985). The major advantages of these models are that they need very little memory for storage and the time required for developing the model is shorter in comparison with other modeling approaches. The drawback of this model is that, it depends on technology to produce accurate results. Pure empirical models are seldom used in circuit simulators, although empirical parameters are often included in physical models and simulators to describe the 2D or 3D behavior of the device under consideration.

1.8 SCOPE OF THE THESIS

Continuous shrinking of channel length in Silicon CMOS devices to increase performance has led to the development of non-planar devices. Nanowire based Field Effect Transistors are an attractive candidate in this area due to their better electrostatic gate control. Recently many research groups have demonstrated fabrication of nanowire transistors of diameters even down to 3nm. To understand the working of such small devices it is important to have proper theoretical models that encapsulate the device characteristics.

Modeling and numerical simulation play an important role to predict the behavior of novel device architectures. Therefore, in order to fully assess the ultimate performance of Silicon Nanowire Transistors, proper modeling is essential in understanding their electrical characteristics. This dissertation gives us the exploration and analytical modeling of three different Scattering
mechanisms and its combined effect in Near ballistic Silicon Nanowire MOSFET. Analytical modeling provides insight into the operation of modern semiconductor devices and circuits, and simulation dramatically reduces the fabrication costs and time to-market.

Thus, the work in this thesis focuses on deriving the analytical models for Discrete Random dopant Scattering (DRS) or Impurity scattering influenced Near Ballistic Silicon Nanowire MOSFET (SiNW MOSFET), Surface Roughness Scattering (SRS) influenced Near Ballistic SiNW MOSFET, Scattered Near Ballistic SiNW MOSFET which includes both SRS and DRS and Temperature influenced Scattered Near Ballistic SiNW MOSFET. The scope of the work is to analyze the Current-Voltage and analog characteristics for various scattering mechanism in Silicon Nanowire MOSFET. Throughout the thesis, the proposed models are simulated using MATLAB and validated using the device simulator Sentaurus TCAD.

1.9 **ORGANIZATION OF THE THESIS**

In this work, Near Ballistic Silicon Nanowire Transistor with various scattering effects are investigated in detail, both in analytically modeled results and simulation. The first chapter of this thesis introduces the conventional MOSFET operation, the important features of Silicon Nanowire Transistors and various scattering mechanisms in Silicon Nanowire Transistor. Chapter 2 discusses the literature review and the methodology used in modeling Gate All Around (GAA) Silicon Nanowire (SiNW) MOSFET. An overview of the device simulator Sentaurus TCAD, which is used to validate the simulations results, is also given in this chapter. Chapter 3 deals with the structure and operation of the Gate All Around (GAA) Silicon Nanowire Transistor. An analytical model for Near Ballistic SiNW MOSFET is developed by including the impact of Impurity-limited mobility or Discrete Random dopant Scattering (DRS) using Natori’s quasi-ballistic transport model for Si NW MOSFETs, which is derived
by directly solving the BTE. The performance of Current-Voltage and analog characteristics of above model is analysed. Chapter 4 presents the analytical model for Near Ballistic SiNW MOSFET which includes the impact of Surface Roughness Scattering (SRS) using Natori’s quasi-ballistic transport model for Si NW MOSFETs is obtained. The performance of Current-Voltage and analog characteristics of above model is analysed. Chapter 5 presents the analytical model for Scattered Near Ballistic SiNW MOSFET which includes the effect of both SRS and DRS is developed using Natori’s quasi-ballistic transport model. The performance of Current-Voltage and analog characteristics of above model is analysed. In chapter 6, presents the analytical model for Temperature influenced Scattered Near Ballistic SiNW MOSFET which includes both SRS and DRS at different temperature is developed using Natori’s quasi-ballistic transport model. The performance of Current-Voltage and analog characteristics of above model is analysed. Chapter 7 concludes the works proposed in this thesis and provides the suggestions for future works.