ABSTRACT

Silicon CMOS has been the technology of choice of the microelectronics industry for the past four decades. In this regard, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have become the fundamental building blocks of Very Large Scale Integrated circuits (VLSI) due to their excellent properties. The demand for higher integration density, low power consumption, high speed and low cost requires aggressive scaling of the MOSFETs. While scaling down the device, as the channel length of a MOSFET is reduced, departures from long channel behaviour are expected to occur. These deviations are called as “Short-Channel Effects” (SCEs), which are the results of a two-dimensional potential distribution and high electric fields in the channel region. Hence, in these conditions, Silicon Nanowire Transistors have garnered a huge attention in the modern semiconductor industry as the alternate option for the conventional MOSFETs due to their highly improved electrical and optical properties. Devices based on silicon nanowires are bound to have high electrostatic control over the channel and reduced short channel effects.

The classical single gate devices are approaching their minimum channel length due to the limit imposed by gate oxide tunnelling. For extending the scalability of CMOS technology, several non classical MOSFETs have been proposed that are being the subject of intense research. The use of several gates has shown good electrostatic control of the channel and, therefore, the possibility of higher reduction in channel length compared to traditional bulk MOSFETs. Structures such as FINFETs, Double Gate (DG), Tri Gate (TG), Surrounding Gate (SG) and Omega Gate devices are preferred to planar structures as they have a steep sub threshold voltage and reduced leakage currents for very short channel lengths. Short channel effects like Drain Induced Barrier Lowering
(DIBL), threshold voltage roll-off, and off-state leakage current are greatly reduced in these devices.

Surrounding Gate structures are one of the most promising structures beyond bulk CMOS. Theoretically, they provide better gate electrostatic control capability than planar and double gate devices. The nanowire approach to nanoscale MOSFET fabrication offers the possibility for ultimate scaling of the transistors using Gate All Around (GAA) device structure. Since the addition of more gates (two or more) improves MOSFET’s performance, as well reduces short channel effects.

Carrier transport regime is classified as diffusive transport, quasi-ballistic transport, and ballistic transport. Roughly speaking, when the gate length (Lg), longer than 0.1 µm, the carriers traverse within the diffusive transport regime. When the Lg is shorter than 10 nm, the carriers traverse within the ballistic transport regime. In the intermediate Lg, the carriers traverse within the quasi or near ballistic transport regime. Carrier scattering is an important phenomenon of near ballistic transport. Scattering mechanisms are broadly classified as Defect scattering, Carrier-Carrier scattering and Lattice scattering. This dissertation gives us the exploration and analytical modeling of three different Scattering mechanisms and its combined effect in Near ballistic Silicon Nanowire MOSFET.

In this thesis, an analytical model of a Discrete Random Dopants (or) Impurity Scattering influenced Near Ballistic Silicon Nanowire MOSFET has been developed. This model is used to formulate an analytical expression of Drain current using Landauer formalism. Landauer formalism incorporates impurity limited mobility which is derived using “knitting” algorithm. Transmission parameters have been evaluated by directly solving Boltzmann transport equation (BTE). Finally the drain current for Near ballistic Silicon Nanowire MOSFET considering Impurity Scattering mechanism is evaluated.
Analog parameters like Transconductance \( (g_m) \), Transconductance generation factor \( (g_m I_{DS}) \) and Early Voltage \( (V_a) \) are also analysed from derived Drain current.

Another scattering mechanism called Surface Roughness Scattering is considered in the device structure. An analytical model of a Surface Roughness Scattering influenced Near Ballistic Silicon Nanowire MOSFET has been developed. This model is used to formulate an analytical expression of Drain current using Landauer formalism. Landauer formalism incorporates Surface Roughness limited mobility and Transmission parameter. Finally the drain current for Surface Roughness Scattered Near ballistic Silicon Nanowire MOSFET is evaluated. Analog parameters like Transconductance \( (g_m) \), Transconductance generation factor \( (g_m I_{DS}) \) and Early Voltage \( (V_a) \) are also analysed from derived Drain current.

The third device that has been considered combines the above mentioned Impurity and Surface Roughness scattering in the same device structure. This model is used to formulate an analytical expression of Drain current using Landauer formalism. Landauer formalism incorporates combined scattering using Mathiessen’s rule and Transmission parameter. Finally the drain current for Combined Scattered Silicon Nanowire MOSFET is evaluated. Analog parameters like Transconductance \( (g_m) \), Transconductance generation factor \( (g_m I_{DS}) \) and Early Voltage \( (V_a) \) are also analysed from derived Drain current.

Finally, the temperature influenced Scattered SiNW MOSFET is considered. This model is used to formulate an analytical expression of Drain current for Combined scattering with temperature effect using Arora’s formula. Landauer formalism incorporates combined scattering using Mathiessen’s rule and Transmission parameter. Finally the drain current for Combined Scattered Silicon Nanowire MOSFET is evaluated at various temperatures. This work
discusses the detailed behavior of analog parameters like transconductance \((g_m)\) and early voltage \((V_a)\).

Throughout the thesis, the proposed analytical device models are simulated using MATLAB and validated using the device simulator Sentaurus TCAD. In essence, the work proposed in this thesis addressed Scattering issues related to Surrounding Gate Nanowire Transistors and will facilitate further research in them.