CHAPTER 3

IMPACT OF SEU IN VOLTAGE AND CURRENT BEHAVIOUR IN CNTFET SRAM CELL

3.1 INTRODUCTION

Single Event Upset concepts, critical charge characterization, modelling of current pulse for CNTFET SRAM is explained in this chapter. The purpose of this chapter is to analyse the details of the way SEU makes changes in CNTFET SRAM qualities and its comparison with reference to CMOS 6T SRAM.

This chapter is intended to analyse the impact of Single Event Upset in voltage and current characteristics in CNTFET SRAM cell during all three modes of operation. It has been concluded that even a small amount of radiations can cause flipping in the SRAM nodes and the need for the special circuitry to detect and correct the errors in CNTFET SRAM,

Due to their low power consumption and low off current values, CNTFETs are found to be suitable device for memory structures. At nanoscales level due to scaling of VDD SRAM operation is affected. The problem can be best corrected with usage of CNTS instead of CMOS. SEUs are modelled as current pulses which have been discussed in previous chapter having varying amplitude based on the amount of charge.
Charge required to upset the device is known as critical charge. When the device goes on decreasing the charge required to cause the flip also decreases. The study of the changing characteristics by SEU had become essential thing like power, area and speed.

Previously the SEU analyses were done at the space level. Then in later stages it is found that at ground level the impact of SEU s can be observed. This is due to the alpha particles. These alpha particles occur due to the radioactive decay of Uranium and Thorium present in the packaging materials. Solder bumps containing lead isotopes acts as source for alpha emitters. When these materials are nearby to substrate they bring about serious effects in the characteristics. The main aim of this chapter is to know about how the single Event upset is bringing change in the characteristics of CNTFET SRAM under various considerations. This chapter is organized as follows. The first part deals with the previous works, whereas subsequent parts deal with the read write operations of CMOS SRAM, CNTFET SRAM, radiation effects in CMOS SRAM, CNTFET SRAM, changes in voltage and current behaviour and the discussion of results.

3.2 PREVIOUS WORK

In previous works comparison of leakage currents between CMOS SRAM and CNTFET SRAM, preferences for choosing the CNTFET over CMOS SRAM, effect of Single Event Upset are discussed. From the literature CNTFET seems to be a promising technology when we come to nanoscales. The study of single event upset in CMOS SRAM at the circuit level and at the fabrication level and the measure to correct the errors at different level is explained.
The proposed work gives a brief analysis of how these effects bring about changes in the CNTFET SRAM voltage and current characteristics when subjected to ionizing radiation.

### 3.3 CRITICAL CHARGE CHARACTERIZATION

Critical Charge \(Q_{\text{crit}}\) is defined as the amount of charge required to change the state of the circuit. The ion strike is specified by two phases one is fast drift current and the other is slow diffusion current. Reverse biased junctions are more prone to ion strikes. OFF-NMOS and OFF-PMOS are more sensitive to strikes, since more electron mobility is observed (Naseer et al. 2007) there are different modelling techniques available for single event transient. Some of the models will be discussed below.

According to (Roche et al) \(Q_{\text{crit}}\) can be found using the Equation (3.1).

\[
Q_{\text{crit}} = C_N VDD + I_{DP} T_F 
\]  

\((3.1)\)

\(C_N\) is the node capacitance \(VDD\) is the supply voltage, \(I_{DP}\) is the maximum drain conduction current of the PMOS. \(T_F\) is the flipping time of the cell. Since the additive term is neglected, \(Q_{\text{crit}}\) found by this method seems to be underestimated one. Another current model proposed by (Freeman 1996) is also used to find the \(Q_{\text{crit}}\) for CMOS SRAM cell. His model projected \(Q_{\text{crit}}\) in terms of total charge deposited by the ion and timing parameter \(\tau\) given by equation 3.2 (Freeman 1996).

\[
I(t) = \left( \frac{2}{\sqrt{\pi}} \right) \cdot \left( \frac{Q_{\text{crit}}}{\tau} \right) \cdot \left( \sqrt{\frac{t}{\tau}} \right) \cdot \exp \left( -\frac{t}{\tau} \right) 
\]  

\((3.2)\)
The next model given by Equation (3.3) is the diffusion model which is found to be more suitable for neutron strikes (Naseer et al. 2007). The \( t_{\text{max}} \) is the instant of time where maximum \( I_{\text{max}} \) is reached.

\[
I(t) = I_{\text{max}} \left( e^{\left(\frac{t_{\text{max}}}{t}\right)}\right)^{\frac{3}{2}} \left(\exp\left(-3\frac{t_{\text{max}}}{2t}\right)\right) \tag{3.3}
\]

The most commonly used model is the double exponential pulse given by equation 3.4. This model is used for the experimental analysis of our research work. This model is having two timing parameters \( \tau_r \) and \( \tau_f \). Former represents the rising time and the latter represents falling timing constants. \( I_{\text{max}} \)

\[
I(t) = \frac{Q_c}{\tau_f - \tau_r} \left[ \exp\left(-\frac{t}{\tau_f}\right) - \exp\left(-\frac{t}{\tau_r}\right) \right] \tag{3.4}
\]

From the work of (Naseer, R. Boulghassoul, 2007) the double exponential models are best suited for current profiles for LETs less than 1 MeV-Cm\(^2\)/mg.

\( Q_{\text{crit}} \) value computed from 3D device simulation currents are 3 times smaller than the available current models (Naseer et al. 2007), this modelling seems to be underestimating the real SER risk. In our work we have considered double exponential pulse. Different kinds of modelling curves for Single Event Upset are given in the Figure 3.1.
To model the SEU in SRAM cell a current pulse is injected in sensitive node of SRAM and the values at the output nodes are studied. The variation in the value of $Q_c$ highly depends on the amplitude, current pulse rise time and fall time. The analysis of photocurrent pulses from (LET) heavy ions can be described by an exponential pulse. The threshold to produce the soft error is close to $0.25 \text{MeV-cm}^2/\text{mg}$ (Naseer et al. 2007).

### 3.4 CNTFET SRAM CELL

In this section some of the design factors involved in the design of CNTFET SRAM are discussed.
Figure 3.2  CNTFET SRAM

Figure 3.2 gives the structure of CNTFET SRAM. The following are some of the considerations considered for the CNTFET SRAM construction for the simulation. In this figure MN0, MN1 acts as driver transistors, MP0, MP1 acts as load transistors and TG0 and TG1 acts as access transistor. WL is the word line and BL, BL_B.

- Supply voltage VDD=0.9V
- Chirality of tube (n, m)=(13,0) and (19,0) (Zigzag)
- CNT PITCH =20nm
- Physical Channel length (Lg) =32nm, 22nm, 10nm.
- Mean free path Intrinsic CNT=200nm
- Mean free path doped
- CNT(Lss, Ldd)=32nm
The conventional CNTFET model is used. MOSFET-like CNTFET operation is considered and SB-CNTFET effects is not considered. The choice of MOSFET-like CNTFET model is due to the fact that it is faster and suppresses the ambipolar conduction.

The working principle of CNTFET SRAM is same as that of the CMOS SRAM. The characteristics have been detailed in the next section. Here CNTFET based considerations are discussed. The concept of chirality factor is explained below. The angle of the atomic arrangement along the tube has to be adjusted to make CNTFET to work as a semiconductor or a conductor device. This angle is referred as chiral vector and is represented by an integer pair (n, m). The circumference of carbon nano tube can be expressed in terms of chiral factor which connects the two sites of dimensional graphene sheet as shown is given in the equation 3.5 (Avouris et al. 2003).

\[ C = na_1 + ma_2 \] (3.5)

C = circumference of Carbon nano Tube,

(n, m)-chiral factor

a1, a2- vector co-efficient

The chiral angle can be calculated from the formula given in the Equation (3.6) (https://sites.google.com/site/cntcomposites/structure-ofcnts)

\[ \cos \theta = \frac{\frac{n+m}{2}}{\sqrt{n^2 + m^2 + mn}} \] (3.6)

The differences in the chiral angle and diameter changes the properties of carbon nano tube. This affects the Threshold values also. As the chiral factor is increasing the threshold value will be decreasing. This analysis of changing the diameter values, threshold values and chiral values were done for Single Event Upset affected CNTFET SRAM.
3.4.1 Read and write operations in CMOS SRAM and CNTFET SRAM cell

![6T CMOS SRAM cell diagram]

Figure 3.3 6T CMOS SRAM cell

The read and write operations is similar in CMOS shown in figure 3.3 and CNTFET SRAM cell. In the following paragraph read and write operation with respect to CMOS SRAM is explained which is extended for CNTFET SRAM as well. M1, M3 used as driver transistors, M2, M4 used as load transistors, M5, M6 used as access transistors. BL, NBL taken as bit lines and WL as word line.

To explore and understand the working of memory cell, let us consider the read and write operation in sequence. We derived transistor sizing constraints by understanding read and write operation.

Assume that a bit ‘1’ is stored at ‘Q’. Before read operation both bit lines are precharged to Vdd. The read cycle is initiated by asserting the word line. This enables the pass transistors M5 and M6. When the read operation is done properly the values stored in ‘Q’, ‘Qbar’ are transferred to the BL and NBL lines through M1-M5. This happens by discharging NBL and leaving precharged value on BL. A careful sizing of the transistors is
important because this can inadvertently write ‘1’ into a cell causing malfunctioning of the cell often called read upset.

For large memories bit line capacitance is in the range of pF. After enabling the word line, NBL is pulled to ground by the series combination of two NMOS transistors. For small sized transistors, discharging large bit line capacitance takes the most amount of time. Write operation in CMOS SRAM can be explained with figure 3.4. During WRITE operation the bit line ‘0’ and the NBL line is considered as ‘1’. When the word line enabled the values will be written in the respective nodes.

![Figure 3.4 Write operation in CMOS SRAM](image)

**3.4.2 Static noise margin**

Static Noise Margin (SNM) is the most important parameter for designing memory. The stability of the SRAM circuit depends on the SNM (Static Noise Margin). Good SNM is required for better stability of the cell and it that depends on the value of the pull up ratio, threshold voltage, cell ratio, and also the supply voltage.
About 70% SNM is due to driver transistor (Mukherjee, D et al. 2010). We have analysed SNM with the Read Margin, Write Margin, Hold Margin and also the Threshold voltage because SNM affects both read and write margin and it is related to the threshold voltages of the NMOS and PMOS devices. Suppose if there is a need to increase the SNM of the cell, the threshold voltages of the NMOS and PMOS devices need to be increased. But, there are limits on the threshold voltage. The limitation is because if the devices have too high threshold voltages it is difficult to flip the operation of MOS devices and hard to operate. Increasing the Cell ratio, we achieve increased noise margin and speed, but the size of the cell also increases.

An existing static approach that is a butterfly method for measuring static noise margin is introduced. Butterfly method is a graphical technique of approximating the SNM. It is obtained by drawing the inverter characteristics, mirroring it, superimposing both and finding the maximum possible square between them. Figure 3.5 shows presentation of SNM graphically for a bit-cell holding data. The plot of VTC curve of U1 and U2 gives the “butterfly curve” and is used to determine the SNM. The largest square length that can be embedded inside the lobes of the curve gives the SNM value.

![Figure 3.5 Static Noise Margin](image-url)
In Figure 3.5 Vn represents a noise voltage source. U1 and U2 are the cross coupled inverters. Noise can be introduced by the supply, coupling between bit lines of two cells etc.

3.5 RESULTS AND DISCUSSION

3.5.1 Comparison of SNM between CMOS SRAM and CNTFET SRAM

The comparison of SNM at two different temperatures for CNTFET SRAM and CMOS SRAM is given by (Pushkarna et al. 2010). Table 3.1 gives the comparison of the characteristics of 10nm CMOS SRAM and CNTFET SRAM at 25°C. The SNM calculation is done for CNTFET AND CMOS SRAM cell for 32nm. Figure 3.6 shows the Write SNM curve when the ‘m’ value is equal to 32nm. Table 3.1 and 3.2 compares the measured read and write noise margin.

**Table 3.1 Comparison of CMOS and CNTFET SRAM Characteristics (Pushkarna et al. 2010)**

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>CNTFET SRAM</th>
<th>CMOS SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>32nm</td>
<td>32nm</td>
</tr>
<tr>
<td>SNM (Volts)</td>
<td>0.178</td>
<td>0.117</td>
</tr>
<tr>
<td>Write Margin (V)</td>
<td>0.155</td>
<td>0.2715</td>
</tr>
</tbody>
</table>
Table 3.2  Comparison of SNM for Different ‘m’ values

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>CNTFET SRAM 32nm (n, m)=0, 13</th>
<th>CNTFET SRAM 32nm (n, m)=0, 15</th>
<th>CNTFET SRAM 22nm (n, m)=0, 13</th>
<th>CNTFET SRAM 22nm (n, m)=0, 15</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNMREAD(V)</td>
<td>0.285</td>
<td>0.313</td>
<td>0.278</td>
<td>0.304</td>
</tr>
<tr>
<td>Write Margin(V)</td>
<td>0.261</td>
<td>0.255</td>
<td>0.262</td>
<td>0.257</td>
</tr>
</tbody>
</table>

Values were taken at a temperature of 25°C and chiral value (13,0)

Figure 3.6 WRITE SNM for 22nm CNTFET SRAM.
Figure 3.6 shows the Write SNM curve when the ‘m’ value is equal to 32nm. Table 3.2 shows the variation in noise margin if the chirality factor is varied. Since the chirality factor has the impact in diameter, the variance in the diameter of CNTS from 1.03nm to 1.189nm shows an increase in the READ SNM values but decrease in WRITE SNM values.

3.5.2 Critical charge characterisation

As we are moving towards the reduced size structures the $Q_{\text{crit}}$ value required to cause the flip is also reducing. From the experimental analysis, it has been perceived that the charge required to cause the flip in CNTFET SRAM is very less compared to CMOS SRAM. We have considered rise time as 2.5ps and fall time as 5.5ps.

**Table 3.3 Charge Values and Corresponding Current Values Used In CNTFET SRAM**

<table>
<thead>
<tr>
<th>$Q_c$ value(fC)</th>
<th>I(t) A</th>
<th>$\tau_f$=5.5 ps $\tau_{r=2.5}$ ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.084 $\times 10^{-3}$</td>
<td></td>
</tr>
<tr>
<td>4.2</td>
<td>0.305 $\times 10^{-3}$</td>
<td></td>
</tr>
<tr>
<td>10.2</td>
<td>9.16 $\times 10^{-6}$</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.7 shows the Current pulse used in for flipping of 32nm CNTFET SRAM cell for chiral value (13,0) (14, 0). In this amplitude of 9.169 $\mu$A is shown.
Figure 3.7  Current Pulse Used for the Study of SEU in CNTFET SRAM

Flipping occurs for an exponential pulse if \( Q_{c} = 3Q_{\text{crit}} \).

Table 3.4  Chiral values and corresponding \( Q_{\text{crit}} \)

<table>
<thead>
<tr>
<th>Chiral value (n, m)</th>
<th>( Q_{\text{crit}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(13,0)(14, 0)</td>
<td>9.1699uA</td>
</tr>
<tr>
<td>(0, 15)</td>
<td>9.2uA</td>
</tr>
<tr>
<td>(0, 16)</td>
<td>17.5uA</td>
</tr>
<tr>
<td>(0, 17)</td>
<td>18uA</td>
</tr>
</tbody>
</table>

Chiral values and corresponding \( Q_{\text{crit}} \) values are tabulated in Table 3.4. As the chiral value increase the Diameter value increases and therefore the charge required to flip the cells also increases.
3.5.3 Radiation Effects In 32nm SRAM Cell

3.5.3.1 Voltage Behavior

For this experimentation 32nm SRAM is considered. Berkeley Predictive model files are used for modelling CMOS SRAM. Pulse width can vary between a few (ps) to hundred (ps). The simulations are done for both read as well as write operation.
Flip is caused when the charge values more than the critical charge. The condition for flipping is also observed to be $Q_{\text{crit}} = 3Q_c$. In our circuit charge hitting happens at 15ns. Rise time is considered as 2.5 ps. Critical charge value is dependent on the pulse width. It is observed that the charge value being raised when the pulse width is increased. The output graph
is given in figure 3.8 which shows the occurrence of flipping when the collected charge value is 3 times that of the critical charges.

The $Q_{\text{crit}}$ values were calculated based on the given equation 3.7 (Torrens, G et al. (2009))

$$i(t) = \frac{Q_{\text{coll}}}{\tau_f - \tau_r} \left( e^{-\frac{(t-t_0)}{\tau_f}} - e^{-\frac{(t-t_0)}{\tau_r}} \right)$$  \hspace{1cm} (3.7)

Before reaching $Q_{\text{crit}}$ the cell is in the metastable state, where it is having admissible overlapping. After some time it will regain its original states and this is taken as pass case.

Rise time is considered as 2.5 ps and fall time as 5.5 ps. The same procedure is repeated for $Q='0'$ and $Q_{\text{bar}}='1'$ and for reading operations the ratio of the driver transistor sizes to that of access transistor size is kept higher than 0.5 in order to prevent read and upset problem. Figure 3.9 shows the cell being affected during read operation.

3.5.3.2 Current Behavior

Leakage current is influenced in SRAM by SEU particle hit. This is found to be some five times higher than that of the cell without SEU. The total leakage component can be the summation of individual current leakages given by equation 3.8 (Torrens, G et al. (2009)) .

$$I_{\text{seu}} = i_{\text{VDD}} + i_{\text{gnd}} + i_{T_{g0}} + i_{T_{g1}} + i_c$$  \hspace{1cm} (3.8)

Individual components include access transistor leakages in supply($i_{\text{VDD}}$ ) and ground lines($i_{\text{gnd}}$ ), leakage in bulk or substrate, leakage currents through pass transistors($i_{T_{g0}}, i_{T_{g1}}$) charging and discharging of currents in $Q$ and $Q_{\text{bar}}$ ($i_c$).
Figure 3.10  Current Values measured when $Q_c = Q_{\text{crit}}$ in the 32nm SRAM cell

Figure 3.10 shows the amount of leakage current measured at different nodes in 32nm CMOS SRAM. From this, it is inferred that the current value is in the order of 80\(\mu\text{A}\) peak value for VDD. When the ion hits the NMOS transistor the number of electrons will be induced in the cell. The presence of SEU increases the amount of leakage current across the access transistor and load transistor. The analysis is extended for CNTFET SRAM and the next section describes the leakage analysis with CNTFET SRAM.
3.5.4 SEU in CNTFET SRAM Cell

3.5.5 Voltage behavior

Figure 3.11 SEU modeled in CNTFET SRAM

Figure 3.11 shows the circuit diagram in which SEU is injected CNTFET SRAM. MP0, MP1 load transistors, MN0, MN1 acts as driver transistors, TG0, TG1 acts as access transistors.

The Stanford CNTFET model is used for simulation. The standard model is used for analysis. The following parameters are considered:

- Supply voltage VDD=0.9V
- Chirality of tube (n, m)=(13,0) and (19, 0)(Zigzag)
- CNT PITCH =20nm
- Physical Channel length (Lg) =32nm, 22nm, 10nm
- Mean free path Intrinsic CNT=200nm
- Mean free path doped CNT(Lss, Ldd) = 32nm
- The conventional CNTFET model is used. MOSFET like CNTFET operation is considered and SB-CNTFET effects not considered.

The MOSFET like CNTFET model is used due to the fact that it is faster and suppresses the ambipolar conduction. The $Q_{\text{crit}}$ value required to cause the upset in read operation takes a more value compared to that in write operation. Read operation which is affected by SEU is given in Figure 3.12.

![Figure 3.12 Read operation affected by SEU in CNTFET SRAM](image_url)
3.5.5.1 Current behaviour

The current analysis includes leakage currents in VDD, GND and access transistors. Dependence of each parameter with respect to collected charge is calculated. Then the characteristics were compared with normal SRAM. The characteristics were analysed in hold mode also Figure 3.13 shows the leakage at different nodes.

![Leakage current values at Qc=Qcrit for (0,13)](image)

**Figure 3.13** Current values measured at Qc=Qcrit for 32nm CNTFET SRAM Cell
Figure 3.14 Leakage current values at Qc=Q_{crit} for Chirality (0,19) for 32nm CNTFET SRAM Cell

The variation of leakage current values for varied chirality is shown in figure 3.14 and figure 3.15 for 32nm CNTFET SRAM cell. The calculated value for the 32nm CNTFET SRAM cell at the time of the ion strike for chirality factor (13,0) is represented in Table 3.5 and Table 3.6 for chirality factor (19, 0).

Table 3.5 Leakage Currents observed due to the current pulse in 32nm CNTFET SRAM for chirality factor (13,0)

<table>
<thead>
<tr>
<th>Nodes</th>
<th>Leakage current values at Qc=Q_{crit}</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>8.98\mu A</td>
</tr>
<tr>
<td>GND</td>
<td>8.19\mu A</td>
</tr>
<tr>
<td>TG0</td>
<td>1.29\times10^{-13} A</td>
</tr>
<tr>
<td>TG1</td>
<td>0</td>
</tr>
</tbody>
</table>
Table 3.6 Leakage Currents observed due to the current pulse in 32nm CNTFET SRAM for chirality factor (19, 0)

<table>
<thead>
<tr>
<th>Nodes</th>
<th>Leakage current values at $Q_e=Q_{crit}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>9.12μA</td>
</tr>
<tr>
<td>GND</td>
<td>1.06x10^{-5} A</td>
</tr>
<tr>
<td>TG0</td>
<td>9.93x10^{-12} A</td>
</tr>
<tr>
<td>TG1</td>
<td>0</td>
</tr>
</tbody>
</table>

When subjected to SEU current leakage values of CNTFET are comparatively less than CMOS SRAM. As the channel length decreases the charge value required to bring the flip also decreases and also the leakage values. Leakage current increases by a factor of $10^3$ for VDD and GND for CMOS SRAM. CMOS SRAM access transistors current varies by a value of $10^{10}$. Compared to CNTFET SRAM when SEU hits the off transistor.

Leakage currents are measured by varying the diameter values. The diameter plays a critical role in the characteristics of CNTFET given by the equation 3.9 (Sinha & Chaudhury 2014).

$$D_{CNT} = \frac{a_0}{\pi} \sqrt{n^2 + mn + m^2}$$  \hspace{1cm} (3.9)

The diameter value depends on n, m and varies accordingly where the value of $a_0$ is given as .249 n, m are chiral values. The diameter of CNNTS is varied and the impact of SEU in CNTFET SRAM is studied. In our study, the diameter varies between 1.03nm to 1.343nm and the leakage currents are measured. Figure 3.15 shows the increase of $Q_{crit}$ value when the diameter value is increased.
Figure 3.15 Dependency of Charge Values on Diameter Values

![Graph showing dependency of charge values on diameter values.](image_url)
When comparing the results of CNTFET SRAM with CMOS 6T SRAM, $Q_{crit}$ value is found to be very less for CNTFET SRAM which shows that CNTFET SRAMs are easily susceptible to even small amount of charges. From this, it is inferred that when CNTFET SRAM if used for space applications, even a small amount of radiation can cause soft errors.

The channel width values can be changed by varying the number of tubes in CNTFET. The impact of varying the width brings variation in the charge required to bring the flipping. As the number of tubes is increased the $Q_{crit}$ value also increases.

CNTFET possess gate controlled characteristics. If the gate controlled parameters and the drain controlled parameters are varied, there is
an increase in drain current. The most of the currents showed negative value that is the current direction is on the negative side and then rises. This occurs at the time of SEU hit. Simulations are done for various channel lengths of 32nm, 22nm, 10nm. As the device size is reduced, the amount of leakage current is less compared to the analysis done with 6T SRAM. The chirality factors were varied and the simulations were done for various chirality factors. The analysis done with chirality factor variation accounts for three different analysis which include diameter variation threshold voltage variation and the model of CNTFET. Two sets chirality had been taken (19,0) and (13,0), and relates to the threshold voltage of 0.293V and 0.428 V. Leakage currents were analysed for the rise time of 2.5ps and fall time of 5.5ps. The critical charge value increases as the chiral value increases shown in Figure 3.16a, 3.16b shows that ,as the diameter value gets increased the leakage current value also increases.

Only minute changes are observed when the temperature is varied. It is varied between -10° C to 125°C. For the worst case conditions, small variations in voltage characteristics and major changes in current characteristics are observed. The leakage current for worst case conditions shows similar results of 6.39 μA as that for the normal case condition. The flipping factor is reduced as the temperature is increased. The temperature variation causes leakage factor to be less in CMOS SRAM than in CNTFET SRAM. The temperature rise made the VDD terminal to be affected irrespective of SEU Pulse.
From Table 3.7 when we compare the results of CNTFET SRAM and CMOS, the leakage current values are less in CNTFET SRAM. At the same time when the chirality factor is varied, higher chirality values showed higher leakage. Hence, for a lower threshold value CNTFET shows more leaky values. The channel length variations show the increase in leakage at the time of SEU strike when the channel length is decreased.

As the diameter varies between 1.03nm to 1.343nm the $Q_{\text{crit}}$ value shows the greater dependence on the diameter variations. The increase in diameter increased the resistance towards an ion strike. i. e. the value of $Q_{\text{crit}}$ is increased. So for smaller charges CNTFET SRAM does not show Upsets. As the diameter varies or increases, the leakage currents across the nodes increase. This is due to the dependency of leakage current on band gap and band–band tunnelling and this, in turn, depends on the diameter of CNTs and the Supply voltage(Javey et al. 2004).
Table 3.8  Impact of certain parameters on the current transients – a comparison

<table>
<thead>
<tr>
<th>Factors</th>
<th>CNTFET SRAM</th>
<th>CMOS SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>A Leakage current increase in the ground node by a factor of 2 µA is observed</td>
<td>Leakage current decreases as temperature increases by factor more than 2 µA</td>
</tr>
<tr>
<td>Size variation</td>
<td>Less leaky current value</td>
<td>More leaky current values</td>
</tr>
<tr>
<td>Chirality factor</td>
<td>Current value increases with increase in chiral factor</td>
<td>-</td>
</tr>
<tr>
<td>Critical Charge</td>
<td>For very low charge values flipping occurs</td>
<td>Charge value is Comparatively more than CNTFET SRAM for same channel lengths at nanoscales.</td>
</tr>
<tr>
<td>Diameter</td>
<td>As the diameter value has increased the value of $Q_{\text{crit}}$ increases</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 3.8 summarises the impact of SEU by considering various parameters on CNTFET SRAM and SRAM. As the $Q_{\text{c}}$ values increase the defect also increases to a certain high energy level after which it remains constant.

3.6 CONCLUSION

This chapter shows the effect of SEU in CNTFET SRAM and its comparison with 6T SRAM. The results of the CNTFET SRAM show major variations with respect to current values when compared to normal SRAM. The impact of SEU is more in a CNTFET based SRAM cell as it is being affected by small charge value. But the ion strike induces fewer leaks. The
temperature variations show a greater impact on the VDD and GND lines. An efficient BICS is to be developed to detect these minute variations of current in power and ground lines. BICS can be placed in access transistors for SEU detection due to variation in current across the access transistor.

This chapter gives the general introduction to CNTFET devices, CNTFET SRAM, CNTFET SRAM characteristics and Single Event Upset Characteristics in CNTFET SRAM. The charge characterization is also dealt in a brief manner which will be a prerequisite for the forthcoming chapters. The next chapter elaborates the fault analysis in CNTFET SRAM.