Abstract

Title: Study of InGaAs n-channel MOSFETs for analog/mixed signal application

Over the last four decades, spectacular improvement in the performance of integrated circuits (ICs) has been achieved due to aggressive miniaturization of device dimensions of complementary metal oxide semiconductor field effect transistors (CMOSFETs). Recently, high mobility channel materials such InGaAs and Ge have become attractive to researchers due to their outstanding transport properties particularly at more advanced technology nodes. The present thesis deals with device physics, design, and optimization of InGaAs nMOSFETs, hybrid CMOS device comprising n-InGaAs and p-Ge MOSFETs with channel length ranging 140 - 20 nm for analog/RF and logic circuit applications. First, a detailed investigation of analog performance of InGaAs nMOSFETs has been made together with a comparison with equally-sized Si nMOS devices, in which InGaAs devices have turned out to be superior. Secondly, the effect of dual-material gate has been studied, which has been proved to be an effective technique in reducing the output conductance of the InGaAs nMOS device for sub-100 nm technology nodes. Thirdly, investigations have been conducted to study the influence of mole fraction $x$ of In in In$_x$Ga$_{1-x}$As channel material and thickness of a barrier layer inserted between the channel and gate oxide on the analog/RF performance parameters of the device. Such an optimization of sub-50 nm devices is useful to choose the most preferable nMOS In$_x$Ga$_{1-x}$As devices for further analysis. Fourthly, investigations have been extended from the device level to the circuit level and a comprehensive analysis of CMOS devices comprising optimized In$_x$Ga$_{1-x}$As nMOSFETs and Ge pMOSFETs has been performed to study different logic circuit parameters of the hybrid CMOS inverters and their comparison with equivalent Si counterparts. It has been found that in digital domain the hybrid CMOS, comprising In$_x$Ga$_{1-x}$As nMOS and Ge pMOS outperforms the equivalent Si CMOS in terms of rise time, fall time, noise margins, etc. Finally, in-depth analyses have revealed that hybrid CMOS devices comprising In$_x$Ga$_{1-x}$As nMOSFETs and Si pMOSFETs, exhibit superiority compared to equivalent Si CMOSFETs with respect to various device parameters related to analog/RF performance. The author’s detailed analysis turns out that hybrid CMOSFETs may be useful for future nanoelectronics.

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