CHAPTER - VIII

Conclusion and future direction

8.1 Conclusion

The continuous down-scaling of Si-based complementary metal-oxidesemiconductor (CMOS) devices has enabled higher device packing density and performances. However, the performance enhancement will soon be limited by the fundamental limit imposed by the material properties of Si. Higher mobility material is needed to replace silicon channel material for future logic application. For n-channel metal-oxide-semiconductor field-effect-transistors (n-MOSFETs), III-V compound semiconductor, such as In$_{x}$Ga$_{1-x}$As (also denoted as InGaAs), is the most matured and suitable channel material.

This thesis has explored the performance of various types of InGaAs nMOS in analog and RF domain followed by the optimization of the appropriate device, based on the obtained result. Then, the performance of Ge pMOS has been studied. The performance of the both the devices are being compared with their Si counter parts. InGaAs and Ge devices have been found to outperform their equivalent Si devices in analog and RF domain. Furthermore, a circuit level analysis of hybrid CMOS device in analog as well as in digital domain has been thoroughly investigated and the performance parameters have been compared against the equivalent traditional Si CMOS devices. Hybrid CMOS devices have been found to outperform the equivalent Si CMOSFETs.
Various device parameters pertaining to analog circuit performance for InGaAs n-MOSFETs have been studied. The study shows that the InGaAs-channel devices outperform their Si counterparts in terms of transconductance, transconductance-to-drain-current ratio, voltage gain, and unity-gain cutoff frequency. Further improvements in these parameters are possible if the interface trap charge density is reduced by using efficient passivation techniques.

Furthermore, various device parameters for analog circuit performance pertaining to InGaAs channel DMG (dual material gate) and SMG (single material gate) n-MOSFETs have been studied. It is demonstrated that the DMG device outperforms its SMG counterpart in terms of transconductance, transconductance-to-drain current ratio, voltage gain, and unity-gain cut-off-frequency. Further improvements in these parameters are possible if the interface-trapped-charge density is reduced by using elegant passivation techniques.

A detailed investigation regarding the effect of different barrier layers on the electrical parameters of In$_{0.7}$Ga$_{0.3}$As MOSFETs has been performed. The double barrier device outperforms the single barrier and no barrier device in terms of ON current, transconductance ($g_m$), transconductance to drain current ratio ($g_m/I_{DS}$), device gain ($g_d$), unity gain cut-off frequency ($f_T$).

A detailed investigation on the influence of indium content in InGaAs channel on the analog circuit performance of InGaAs MOSFETs has been made. My findings reveal that various device parameters such as, transconductance, transconductance efficiency, cut-off frequency, max frequency of oscillations, and device gain show 18%, 51.19%, 50% , 26% and 32.3% maximum improvement, respectively, for 75% of In content in InGaAs channel with reference to 53% of In. On the contrary, larger In content increases the output conductance owing to higher value of the dielectric constant. Further improvement in the
analog circuit performance of such devices with higher In content may be possible by improving $g_d$ with the use of suitable SCE reduction techniques.

An investigation of the performance of a hybrid CMOS inverter comprising a Ge-channel p-MOSFET and an InGaAs-channel n-MOSFET at channel lengths of 45 nm, 30 nm and 20 nm. The performance parameters, such as noise margin, rise time, and fall time, for such InGaAs/Ge inverter show significant improvement in comparison with that for its equivalent Si counterpart for $D_{it} \leq 5 \times 10^{12}$ eV$^{-1}$cm$^{-2}$. Furthermore, the frequency of oscillations for a 3-stage hybrid ring oscillator exhibits a significant improvement over the equally sized Si-based ring oscillator. My findings revealed that hybrid inverters exhibit notable performance enhancement over their Si counterparts so long as $D_{it}$ remained below $5 \times 10^{12}$ eV$^{-1}$cm$^{-2}$, which had already been achieved in recent processing technology. Moreover, our device exhibits better performance in terms of leakage current, power delay product, and static power dissipation compared with ITRS specifications at different technology nodes.

A thorough analysis of the analog circuit performance of hybrid asymmetric CMOS inverters comprising Si-channel pMOSFETs and InGaAs/InP-channel nMOSFETs for channel lengths of 50 and 30 nm have been studied. The performance parameters such as gain and GBW (Gain-Bandwidth-product) showed significant improvement for the hybrid inverters as compared with their Si counterpart for sub-50 nm channel lengths. Notably, the HAS3 CMOS device yields highest values of peak GBW, unity current gain frequency and maximum oscillation frequency. My findings unveiled the potential of hybrid CMOS devices for their use in extremely scaled regime.
8.2 Future direction

In this thesis, several impressive results on how the InGaAs channel nMOSFET outperforms the equivalent Si nMOSFET in analog and RF domain has been presented. Several techniques, like dual material gate, buried channel MOSFETs, assymetric S/D, etc have been studied in order to improve different analog parameters and to reduce SCEs. All those techniques have been proved to be effective and act as performance benefitters. For sub-15 nm channel length, the SCEs viz. GIDL, DIBL, threshold voltage roll-off, off-state current etc may become critical issues and hamper the device performance. To control the SCEs at smaller technology nodes, innovative device structures are necessary. FINFET, GAA (Gate-All-Around) MOSFETs, nanowires are some of such possible structures. Analytical modeling and simulation studies on these structures using high-mobility III-V channel materials are still at its infancy. Hence, there is an urgent need to develop appropriate models for MOS devices with various architectures using III-V channel materials with advanced high-k dielectrics in order to evaluate analog, digital and RF performances.