CHAPTER - VII

Performance of CMOS With Si p-MOS and Asymmetric InP/InGaAs n-MOS for Analog Circuit Applications

7.1 Introduction

In recent years, novel material combinations and innovative device architectures for CMOS devices are being extensively investigated for further extending the Moore’s law. Hybrid co-integration of nMOSFET with InGaAs channel and pMOSFET with Ge channel can considerably enhance their performance [7.1-7.2]. Notably, a laterally asymmetric InP/In$_{0.53}$Ga$_{0.47}$As MOSFET with different regrown contacts at the source (InP) and drain (In$_{0.53}$Ga$_{0.47}$As) exhibits more drain current and transconductance as compared with InGaAs MOSFET [7.3]. On the other hand, Ge channel pMOSFET suffers from pronounced short channel effects such as DIBL resulting in a large output conductance, which poses constraint to its use in common source CMOS configuration that needs a load device with a large output resistance. In order to mitigate this shortcoming, a hybrid CMOS circuit comprising an asymmetric InGaAs/InP nMOSFET and a Si pMOSFET is proposed. The latter offers a large output resistance because of the low dielectric constant of Si and thus suits well for an active load. Co-integration of Ge pMOS and In$_x$Ga$_{1-x}$As nMOS transistors with a common Al$_2$O$_3$
gate dielectric has already been demonstrated in [7.4] and is discussed thoroughly in previous chapters. The use of high-k dielectrics, such as HfO$_2$ and Al$_2$O$_3$, has become attractive due to their high value of dielectric constant and acceptable values of conduction and valence band offsets. The author's proposed device is not only commensurate with the composite CMOS device reported earlier but simple, cost-effective and can be fabricated on a common Si platform. There have been some investigations on the analog performance of Si-based CMOS devices at channel lengths below 120 nm [7.5, 7.6]. However, the analog behavior of such hybrid CMOS circuit is still unexplored.

In this chapter, the analog performance of a hybrid CMOS inverter using a Si pMOSFET and an asymmetric InP/In$_{0.75}$Ga$_{0.25}$As nMOSFET at channel lengths of 50 and 30 nm, are analyzed and discussed thoroughly in terms of voltage gain and gain-band-width product, followed by a comparison with its Si counterpart [7.7, 7.8].

7.2 Device Structure

Silicon p-MOSFETs and four different types of n-MOSFETs are used to build different common source CMOS inverters studied in this work: (i) asymmetric In$_{0.75}$Ga$_{0.25}$As nMOS with InP source (AS), (ii) asymmetric In$_{0.75}$Ga$_{0.25}$As nMOS with InP drain (AD), (iii) symmetric In$_{0.75}$Ga$_{0.25}$As nMOS (S), and (iv) Si nMOS. The corresponding CMOS inverters are termed as HAS, HAD, HS and SS, respectively. The structure of the HAS inverter is shown in Fig. 7.1. The nMOS in such a hybrid CMOS consists of an InGaAs channel sitting on an InAlAs buffer layer placed on top of an insulator. Such a structure may be realized using wafer bonding technique, as reported in [7.4]. The lowest value of the parasitic source/drain resistance ($R_{SD}$), as reported in [7.9] is employed. $R_{SD}$ consists of contact n-InP
with doping concentration of $2 \times 10^{19}$ cm$^{-3}$ and thickness of 200 nm, capped by contact 10 nm thick n-InGaAs with doping concentration of $5 \times 10^{19}$ cm$^{-3}$, which is followed by source/drain electrode comprising Ti (20 nm) /Pd (20nm) /Au(80nm) [7.9]. The common gate stack of Al$_2$O$_3$/HfO$_2$ capped with gate metal TaN, is used for both n- and p-MOSFETs. The different device parameters of InGaAs nMOSFET and Si pMOSFET following ITRS specifications [7.10] for channel lengths of 50 nm and 30 nm, respectively, used in this study are listed in Table 7.1.

Fig. 7.1 Schematic structure of a CMOS device comprising of an n-channel InGaAs-InP MOSFET and a p-channel Si MOSFET. Also shown is the CMOS inverter circuit and different capacitances.
The detailed device structures for the individual nMOS and pMOS devices, which are used as building blocks for constructing the CMOS circuit in common source configuration are being discussed below. The fabrication technique adopted in [7.1] is described in the following.

The InGaAs nMOS devices, were fabricated on S.I. InP (100) substrates. First, a 190 nm In$_{0.52}$Al$_{0.48}$As buffer layer ($N_A = 5 \times 10^{16}$ cm$^{-3}$), a 5 nm In$_{0.52}$Al$_{0.48}$As delta doping layer ($N_D = 8 \times 10^{18}$ cm$^{-3}$), a 1 nm In$_{0.52}$Al$_{0.48}$As (N.I.D.) barrier layer, and a 10 nm In$_{0.53}$Ga$_{0.47}$As (N.I.D.) channel were grown by molecular beam epitaxy (MBE). Subsequently, a 5 nm Sn-doped InP layer ($N_D \approx 10^{19}$ cm$^{-3}$) and a 5 nm Sn-doped In$_{0.53}$Ga$_{0.47}$As layer ($N_D = 6 \times 10^{19}$ cm$^{-3}$) were grown by metalorganic vapour phase epitaxy (MOVPE). Hydrogen silsesquioxane (HSQ) resist was first used as an etching mask to define the drain (or the source) pattern and then a second mask was defined for the dummy gate by electron beam exposure with a 100 nm overlap towards the edge of the InP, to avoid mis-alignment and to

<table>
<thead>
<tr>
<th>Device parameters</th>
<th>InGaAs nFET</th>
<th>Si pFET</th>
<th>Si nFET</th>
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</thead>
<tbody>
<tr>
<td>EOT (nm) for $L_g = 50$ nm</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
</tr>
<tr>
<td>EOT (nm) for $L_g = 30$ nm</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Channel thickness (nm)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Source/drain extension (nm)</td>
<td>-</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Source/drain junction depth (nm)</td>
<td>40</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Channel doping concentration (cm$^{-3}$)</td>
<td>-</td>
<td>$1 \times 10^{15}$</td>
<td>$1 \times 10^{15}$</td>
</tr>
<tr>
<td>Interface trapped charge density $D_{it}$ (cm$^{-2}$ eV$^{-1}$) [7.1, 7.11]</td>
<td>$1 \times 10^{12}$</td>
<td>$1 \times 10^{12}$</td>
<td>$1 \times 10^{12}$</td>
</tr>
<tr>
<td>$R_{SD}$ (Ω·μm) [7.9, 7.12]</td>
<td>93</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

The detailed device structures for the individual nMOS and pMOS devices, which are used as building blocks for constructing the CMOS circuit in common source configuration are being discussed below. The fabrication technique adopted in [7.1] is described in the following.
serve as a dummy field-plate over the InP region. Regrowth of the S/D epitaxial layers was realized immediately after Ozone and HCl etching [7.13] using the HSQ dummy gate as a hard mask. The regrown layers consisted of a 40 nm thick Sn-doped In$_{0.55}$Ga$_{0.47}$As ($N_D = 6 \times 10^{19}$ cm$^{-3}$) layer and a 90 nm thick InP support layer. After removal of the dummy gate, Al$_2$O$_3$/HfO$_2$ (0.5/5 nm) was deposited through atomic layer deposition (ALD) at 300/120 °C using TMA/TDMAHf and H$_2$O as precursors. A T-shape gate was then defined by e-beam lithography, followed by thermal evaporation of Ti/Pd/Au. The T-gate also served as a mask during the removal of the high-k oxide and the InP sacrificial layer. Self-aligned Ni/Pd/Au S/D contacts were deposited using thermal evaporation followed by a 250 °C, 1 minute anneal. For the assymetric source/drain side the formation of T-gate is done by selectively etching the InP support layer in HCl:H$_2$O. Source and drain Ti/Pd/Au contacts are deposited in a self-aligned manner by thermal evaporation [7.14].

For Si nMOS and pMOS devices the author has chosen UTB SOI MOSFET [7.15] for the purpose of achieving good control of the channel by the gate, and to improve the electronic characteristics of UTB SOI MOSFET. The channel thickness for both Si pMOSFET and nMOSFET are taken as 10 nm having source/drain junction depth as 40 nm and source/drain extension as 10 nm. The channel doping concentration for both the MOSFETs are kept as $1 \times 10^{15}$ cm$^{-3}$.

7.3 Simulation Set Up and Device Parameters

Device characteristics of asymmetric InP/InGaAs nMOSFET and Si pMOSFET are obtained using the two dimensional numerical device simulator SILVACO ATLAS [7.13]. After that, mixed-mode simulation is performed on SILVACO platform to simulate the
different types of common source CMOS inverters for two different channel lengths viz. 50 nm and 30 nm, respectively and for various $W_p/W_n$ ratios.

Experimental findings reveal that InGaAs/high-$k$ interfaces contain interface-trapped charge density in the range of $1 \times 10^{12} - 2 \times 10^{12} \, \text{eV}^{-1} \text{cm}^2$ [7.1, 7.16, 7.17, 7.18]. The dielectric constant of InGaAs alloy is computed using linear interpolation between the corresponding parameters of the constituents GaAs and InAs [7.19, 7.20]. The compressive strain developed in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel grown on InP substrate and InAlAs buffer is taken into account in the calculation of band gap values as well as for calculating corresponding conduction and valence band offsets [7.21]. Also, the reported values [7.22, 7.23, 7.24] of the dielectric constant and the band gap of the substrate InP and buffer material InAlAs are used.

For circuit simulations, same channel length 30 nm, 50 nm and an EOT of 1.0 nm, 1.1 nm, respectively are used for both the devices. The threshold voltage for the InGaAs and Si devices are set at 0.2 and -0.2V, respectively, by adjusting the work function value of the gate metal. The following models have been invoked during simulation.

The author has employed CVT [7.25] Lombardi mobility model for simulating mobility of inversion charges, Hurkx model [7.26] to account for trap-assisted tunneling, models for Shockley-Read-Hall and Auger generation-recombination models, and nonlocal band-to-band tunneling model. In addition, effects of lattice strain between buffer InAlAs layer and channel, and impact ionization are considered for the InP/InGaAs device. Fermi-Dirac distribution of carriers and quantum mechanical effects are also considered. Furthermore, energy balance transport model, which uses a higher order approximation of Boltzmann transport equation, is activated.
7.4 Model Calibration

The simulated drain current, transconductance $g_m$ vs. gate to source voltage $V_{GS}$, and

![Graph showing model calibration for $I_{DS}$-$V_{GS}$ and $g_m$-$V_{GS}$ with experimental characteristics of InGaAs-InP channel nMOSFET in [7.3].](image)

![Graph showing model calibration for $I_{DS}$-$V_{DS}$ with experimental characteristics of InGaAs-InP channel nMOSFET in [7.3].](image)

output characteristics for the asymmetric InGaAs/InP MOSFET match well with the
experimental characteristics reported in [7.3], as may be seen in Fig. 7.2-7.3. Furthermore, model calibration is also performed with measured characteristics for both ultra-thin-body (UTB) Si channel n- and p- MOSFETs in [7.14]. Figs. 7.4-7.6 are showing

![Diagram of potential energy profile](image1)

**Fig. 7.4** Model calibration for potential profile as a function of channel position with reported results published in [7.14] for Si UTB SOI nMOSFET having channel length 35 nm.

![Diagram of electric field profile](image2)

**Fig. 7.5** Model calibration for electric field as a function of channel position with reported results published in [7.14] for Si UTB SOI nMOSFET having channel length 35 nm.
Fig. 7.6 Model calibration for electron velocity as a function of channel position with reported results published in [7.14] for Si UTB SOI nMOSFET having channel length 35 nm.

Fig. 7.7 Model calibration for potential profile, electric field profile and electron velocity profile respectively along the channel length. Fig. 7.7 shows the comparison of output characteristics between the experimental data and our simulated results. From figures 7.4-7.7 it is clearly

Fig. 7.7 Model calibration for output characteristics with experimental results published in [7.14] for Si UTB SOI nMOSFET having channel length 35 nm.
observed that author's simulated data match well with data reported in [7.3, 7.14]. This agreement ensures the validity of the simulation scheme.

7.5 Results and Discussion

A comparison of the transconductance ($g_m$) and output conductance ($g_d$) of four different nMOSFETs against gate over drive voltage ($V_{GT}$) is shown in Fig. 7.8. (a) and (b), respectively.

![Graph](image)

Fig. 7.8 Comparison of (a) $g_m$ and (b) $g_d$ as a function of $V_{GT}$ for different In$_{0.75}$Ga$_{0.25}$As nMOSFETs and Si nMOSFET at $L=30$ nm and $V_{DS} = 0.5V$. The threshold voltage of all the devices is set at 0.2V.

It is evident in Fig. 7.8(a) that $g_m$ for AS exhibits a peak value whereas from Fig. 7.8 (b) $g_d$ is found to be the lowest for Si nMOSFET as compared with the others. These results are commensurate with the experimental results reported in [7.3]. The dielectric constant of Si and In$_{0.75}$Ga$_{0.25}$As are 11.7 and 14.59, respectively. The lower value of dielectric constant results in lower source-channel and drain-channel junction capacitances which in turn prevent...
from easy sharing of source- and drain depletion charges as compared to other devices. As a consequence, short channel effects such as DIBL are lower in Si devices thereby reducing output conductance $g_d$. The voltage gain of different inverters is determined from the slope of the respective voltage transfer characteristic (VTC) at different $V_{Bias}$. Fig. 7.9 (a) and (b) demonstrates the variation of voltage gain with $V_{Bias}$ for different CMOS inverters at channel length of 50 and 30 nm, respectively. Two different values of $W_p/W_n$, 3 and 8, are used for HAS and HAD inverters whereas a value of 3 for the same is used for both HS and SS inverters in Fig. 7.9 (a) and (b). In figures 7.9-7.13, the value of $W_p/W_n$ is indicated on the right hand side of the inverter acronyms. One can observe in Fig. 6.9 (a) and (b) that HAS and HAD inverters produce larger gain throughout the entire range of $V_{Bias}$ in comparison with the other inverters for both channel lengths. The peak gain of the hybrid CMOS inverter is improved by 37.5% and 92.10% for HAD3 and HAD8, respectively, as compared with

Fig. 7.9. Comparison of voltage gain between different inverters at channel length (a) $L_g = 50$ nm and (b) $L_g = 30$ nm.
their equivalent SS3 CMOS device. The highest gain for HAD is attributed to the lowest value of $g_d$ and moderately high value of $g_m$ for AD nMOSFET, as observed in Fig. 7.8 (a) and (b). Different parasitic capacitances at the output node of CMOS inverters, are extracted by AC simulation at $V_{out} = 0.5$ V for two channel lengths. $C_{Total}$, which is the sum of $C_{g1d1}$, $C_{g2d2}$, $C_{d1}$, and $C_{d2}$, is found to decrease slightly with increasing $V_{Bias}$ for both channel lengths, as shown in Fig. 7.10 (a) and (b). As a higher $V_{Bias}$ drives the device toward the subthreshold region of operation, the gate to drain capacitance reduces due to the appearance of depletion capacitance in series association with the gate oxide capacitance. Consequently $C_{Total}$ is reduced with increasing $V_{Bias}$. $C_{Total}$ for HAD is larger than that for HS due to the presence of field-plate capacitance owing to extended channel length toward InP drain. The gain-bandwidth product (GBW) of the inverter is estimated as $GBW = g_m/C_{Total}$, where $g_m$ is the transconductance of the n-MOSFET [7.27], and plotted in Fig. 7.11 (a) and (b) as a function of $V_{Bias}$ with channel length (a) $L_g = 50$ nm and (b) $L_g = 30$ nm.

![Graphs showing C_Total vs V_Bias for different inverters with channel lengths of 50 nm and 30 nm.](image)

Fig. 7.10. Comparison of $C_{Total}$ between different inverters as a function of $V_{Bias}$ with channel length (a) $L_g = 50$ nm and (b) $L_g = 30$ nm.
of $V_{Bias}$ for different inverters at two different channel lengths. The GBW for HAS inverter exhibits the highest value as compared with the other inverters despite the larger value of $C_{Total}$ in the former case. The GBW of HAS3 is increased by 148.1% and 260.4% relative to SS3 for $L_g = 50$ and 30 nm, respectively. The highest GBW for HAS is ascribed to the largest value of $g_m$ for AS nMOSFET, as observed in Fig. 7.8 (a). Also, all hybrid CMOS inverters exhibit increased GBW as compared with their Si counterpart over the entire range of $V_{Bias}$ due to enhanced value of $g_m$ of InGaAs nMOSFET. The variation of GBW with frequency for different hybrid and Si inverters is demonstrated in Fig. 7.12 (a) and (b) at $L_g = 50$ nm and 30 nm, respectively. The HAS3 device exhibits the highest peak value of GBW owing primarily to largest value of $g_m$ in AS n-FET as shown in Fig. 7.8 (a). It is worth noting that in spite of having same $g_m$, the GBW is much lower in HAS8 & HAD8 devices as compared with those in HAS3 & HAD3 devices, respectively, due to higher value of $C_{Total}$, which is

Fig. 7.11. Variation of gain-band-width product with $V_{Bias}$ for different inverters at channel length (a) $L_g = 50$ nm and (b) $L_g = 30$ nm.
accounted for larger $W_p/W_n$ ratio. GBW for other devices can be interpreted by considering variation of $g_m$ as shown in Fig. 7.8 (a) and $C_{\text{Total}}$ as demonstrated in Fig. 7.10 (a) and (b).

The current gains of different devices as estimated from the simulated $y$-parameters are

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Fig. 7.12. Dependence of GBW with frequency for different inverters at (a) $L_g = 50$ nm and (b) $L_g = 30$ nm.

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Fig. 7.13. Demonstration of current gain with frequency for different inverters at (a) $L_g = 50$ nm and (b) $L_g = 30$ nm. $f_T$ corresponds to the frequency at which the current gain equals to unity or 0 dB. Shown in Fig. 7.13 (a) and (b) at $L_g = 50$ nm and 30 nm, respectively. The current gain vs.
frequency plot is extrapolated till the gain equals 0 dB in order to obtain the value of unity current gain frequency $f_T$. The largest value of $f_T$ is observed for HAS3 device, which is attributed to highest value of $g_m$ of n-FET in such a device, as may be noticed in Fig. 7.8 (a), and $C_{Total}$ value closer to the Si value, as may be seen in Fig. 7.10 (a) and (b). Fig. 7.14 (a) and (b)

![Graph](image)

Fig. 7.14. Dependence of power gain with frequency for different inverters (a) $L_g= 50$ nm and (b) $L_g= 30$ nm. $f_{max}$ corresponds to the frequency at which the power gain becomes unity or 0 dB.

shows the dependence of power gain of different devices with frequency having their input and output ports conjugate-matched for maximum power transfer at $L_g = 50$ nm and 30 nm, respectively. It is evident from the figure that the HAS3 device yields largest value of $f_{max}$ which corresponds to the frequency at which the extrapolated power gain becomes 0 dB. The highest value of $g_m$ for AS device and near Si device value of $C_{Total}$ for HAS3 inverter together produce the largest value of $f_{max}$ in HAS3 device.
7.6 Summary

In summary, the analog circuit performance of hybrid asymmetric CMOS inverters comprising Si-channel pMOSFETs and InGaAs/InP-channel nMOSFETs for channel lengths of 50 and 30 nm have been studied and analysed thoroughly in this chapter. The performance parameters such as gain and gain bandwidth product (GBW) showed significant improvement for the hybrid inverters as compared with their Si counterparts for sub-50 nm channel lengths. Notably, the HAS3 CMOS device yields highest values of peak GBW, unity current gain frequency and maximum oscillation frequency of oscillations. Author's findings unveiled the potential of hybrid CMOS devices for their use in extremely scaled technology nodes.

References


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