CHAPTER – 7
APPLICATION OF 128 POINT FFT PROCESSOR FOR MIMO OFDM SYSTEMS

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CHAPTER – 7
APPLICATION OF 128 POINT FFT PROCESSOR FOR MIMO OFDM SYSTEMS

7.1 INTRODUCTION

In this chapter, a low power 128-point FFT processor is adopted for the applications of MIMO - OFDM using mixed-radix algorithm, Single delay feedback (SDF) architecture and multiple delay commutator architecture (MDC) in terms of less complexity and better usage of memory. A mixed radix multiple delay commutator (MRMDC) FFT processor in tradition will improve the capability of hardware and can be employed to alter the sequence order of inputs [3]. Generally the FFT processor is realized with appropriate consumption of power for various sizes of FFT. In general, the architectures based on mixed radix employ a longer internal word length to obtain a signal to noise ratio (SNR) of higher value; whereas proposed processor maintains internal word length same as that of input data by implementing the block-floating point (BFP) approach to keep the SNR constant. The suggested FFT utilizes various commutators to reduce the number of delay elements and combine with MIMO-OFDM blocks.

The FFT plays an inevitable place in the domain of Digital signal processing. It finds use in wide areas such as Communication, Signal processing, Seismic processing, etc [1]. The FFT is also an important component in OFDM systems. The integration of Multiple-input multiple-output (MIMO) with OFDM is a right approach for improving the performance of communication systems where the concept of frequency-selective fading is employed. In this chapter, a 128-point FFT processor for MIMO-OFDM has been implemented which manipulates within a duration of 40 µs.
7.2 TYPES OF ARCHITECTURES OF FFT

Generally the FFT processors can be decomposed into three types -

I. Pipeline FFT: In this type, parallel processing of different stages is employed to obtain high degree of performance.

II. Column FFT: In this type, every stage in FFT is manipulated with a group of butterfly elements and the next stage is computed by providing the output as a feedback to them.

III. Parallel FFT: The functions of signal-flow graph are transformed to a hardware structure in an isomorphic manner. The implementations of hardware are not flexible with account to latest technology and thus not appropriate for constructing large FFTs.

7.3 DESIGN ISSUES OF FFT PROCESSOR FOR MIMO OFDM

The block diagram of the receiver using the standards of IEEE 802.11 n is shown in Figure 7.1. It includes four FFT processors, four Radio frequency components (RF), four analog-to-digital converters (ADCs), four De-Qam and De-interleaver and a 4 x 4 MIMO equalizer along with various other components. The scheme of modulation can be Quadrature Amplitude modulation (QAM) or Binary Phase shift keying (BPSK) with 1–6 bits based upon the selected data rate. The rate of encoding in this case is 1/2, 2/3, 3/4, or 7/8. The count of data sequences is given by 1, 2, 3, or 4. The period of guard interval may be selected as either 400 ns or 800 ns. The range of frequencies for transmission can be chosen as either 20 or 40 MHz. The length of FFT is taken as either 128 or 64 points and the FFT processor has to manipulate them with 1–4 data sequences within 3.6 or 4 seconds in a simultaneous manner. In the past decade, different types of FFT styles such as single-memory architecture, double memory architecture, pipeline architecture, cached-memory architecture and array
architecture had been suggested. But pipeline FFT architectures are used to process multiple sequences of data in case of MIMO-OFDM systems.

In general, several processors of FFT are combined to process multiple sequences of data in a MIMO OFDM system as shown in Figure 7.1 and they account for a huge rise in complexity of hardware and consumption of power in comparison with a single FFT processor. An efficient FFT processor can contribute an optimum performance and also process with multiple sequences of data for the applications of MIMO-OFDM. In this regard, the pipelined FFT must be the correct solution for applications of high throughput with reasonable cost of hardware.

This pipelined architecture is decomposed into two types – single delay feedback (SDF) and multiple delay commutator (MDC). In general, MDC can contribute better performance while SDF needs less hardware and memory. The higher radix algorithm is employed to reduce the count of multiplications in order to reduce the power dissipation. The Radix-4 FFT in two steps is employed to decrease the count of multiplications. Since 128-point FFT is not a multiple of ‘4’, the mixed-radix FFT integrating two different architectures is very much required. The Mixed-radix multiple delay feedback (MRMDF) style is obtained by combining MDC and SDF styles and this architecture contributes higher throughput with low cost. The objective of this chapter is to implement a 128-point FFT processor based on MRMDF architecture and Mixed Radix 4/2 algorithm which can process with 1–4 sequences of data simultaneously for applications of MIMO OFDM thus reducing the complexity of hardware in comparison with the conventional approach.
Fig. 7.1 Block Diagram of Receiver using standards of IEEE 802.11n

7.4 THE FFT ARCHITECTURE FOR MIMO OFDM

The FFT architecture integrating the styles of MDC and SDF includes four modules - 1, 2, 3, 4, conjugate blocks, multiplexers and a division block. The important features of the suggested FFT architecture are as follows. Initially, the operation of a 128 point FFT processor to process with 1–4 sequences of data will be discussed in this design. Next, the design architecture can give several rates of
throughput with standards of IEEE 802.11 n by using delay commutator architecture. The third feature is – less amount of storage is required by adopting the delay feedback architecture to rearrange the input and the intermediate results of each module. The constant multipliers and the scheduling method can be used to decrease the complexity of hardware. Hence this FFT processor possesses less complexity of hardware in comparison with the conventional approach of using multiple processors of FFT. Further a FFT algorithm of higher radix can be adopted to reduce the dissipation of power irrespective of the functions of 128-point FFT.

The sequences of input data and output data follow a particular order in the suggested FFT architecture. Since the order of input sequences of data and order of sequences of data from ADC are the same, no additional memory is needed to rearrange these sequences of input data before loading into the processor. Generally, the order of sequences of output data radically varies from that of input data in a pipelined architecture. Normally output sequence order is based on the algorithm of FFT, available number of data paths and type of architecture used. In this architecture, the order of output sequences is same as that of order of input sequences.

The function of 128 or 64-point FFT is monitored by the control signal mode. If the function of 64-point FFT is to be done, then the computed data from Module 1 will enter Module 3 directly bypassing module 2 as shown in Figure 7.2. The role of Module 1 is to rearrange sequences of the input data from the four data paths into a particular order to implement the FFT operation in an efficient way. The role of Module 2 is to adopt a Radix-2 FFT which corresponds to the initial stage of Signal Flow Graph as shown in Figure 7.3. The functions of Module 3 and Module 4 are meant for adopting Radix-4 FFT and they correspond to the second and third stages of the Signal Flow Graph as illustrated in Figure 7.3. The architectures SDF and MDC
are employed in Module 3 and Module 4 respectively to implement the Radix-4 FFT to reduce the requirements of memory and verify the FFT operation.

![Diagram](image)

**Fig. 7.2 128-point FFT Architecture for MIMO-OFDM**

The 128-point and 64-point FFT are followed for bandwidth of 40 and 20 MHz respectively with respect to standards of IEEE 802.11n [1]. In general, the 1–4 sequences of data have to be included in this case based upon the count of antennas employed. The FFT processor requires eight modes of operation as per the standards of IEEE 802.11. The clock rates 40 and 20 MHz are invariably required for the functioning of 128-point and 64-point FFT respectively. The throughput rates of our architecture depend on the count of sequences of data and are given by-

\[
\text{Throughput Rate (effective)} = 4 \times R \times \text{Operation Ratio} \quad (7.1)
\]

The operation ratio is given by the count of sequences of data decomposed by a factor of ‘4’. If the number of sequences of data is less than four, the number of functional operations will be less than four. Hence the throughput will be less than number of sequences of data and only three functional operations are needed for each
Therefore the operation ratio is equivalent to the effective throughput rate and its value is \( \frac{3}{4} \).

![Fig. 7.3 Signal Flow graph for 128-point FFT](image)

### 7.5 RESULTS AND DISCUSSION

Initially coding for 128 or 64-point FFT algorithm is obtained by using MATLAB. Once FFT algorithm is validated, the processor architecture is modeled and verified using Verilog and XL simulator respectively. The word length of this FFT processor is a factor decided by the customers. This word length is found to be 12 bits and satisfies the standards of IEEE 802.11 n based upon the simulation results. As per the specifications listed in Table 7.1, the clock rates (R), 40 and 20 MHz are used for implementing 128-point and 64-point FFT respectively. Further the sequences of input data are in the determined order before loading into the FFT processor, as shown in Figure 7.2. The manipulation of 128-point FFT and 64 point FFT with four data sequences requires 3.2 seconds (128 cycles) at the clock rate of 40 MHz and 20 MHz respectively.
Table 7.1 Performance of Operation Modes in 128-point FFT

<table>
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<tr>
<th>Mode of Operation</th>
<th>Operation clock rate (R)</th>
<th>Effective throughput</th>
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<tbody>
<tr>
<td>No. Of FFT point</td>
<td>No. of input sequence</td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>4</td>
<td>40 MHz</td>
</tr>
<tr>
<td>128</td>
<td>3</td>
<td>40 MHz</td>
</tr>
<tr>
<td>128</td>
<td>2</td>
<td>40 MHz</td>
</tr>
<tr>
<td>128</td>
<td>1</td>
<td>40 MHz</td>
</tr>
</tbody>
</table>

7.6 SUMMARY

In this chapter, a 128 point FFT processor using Mixed Radix suitable for a MIMO OFDM system has been discussed. This architecture can contribute various rates of throughput to process with 1–4 sequences of data in an efficient manner based upon data reordering and grouping. Moreover, the cost towards multiplier and memory storage can be decreased appropriately by implementing the scheduling of data and delay feedback architecture. Further, the FFT algorithm of higher radix is employed to decrease the count of complex multiplications in an effective manner. This FFT processor can satisfy the standards of IEEE 802.11 at a frequency of 40 MHz.