CHAPTER 4

ANALYSIS AND EXPERIMENTAL VALIDATION OF PROPOSED EXTENDED SWITCHED INDUCTOR QUASI Z SOURCE INVERTER

4.1 INTRODUCTION

This chapter briefly evaluates the performance of selected modified and extended boost quasi Z source inverters (qZSI) topologies through simulation. These topologies possess various advantages like reduced component ratings, reduced source stress, and reduced component count. All the control schemes applied for ZSI can also be adopted for qZSI.

A new family of switched inductor/capacitor qZSI topologies is proposed and extensive open loop simulations are carried out under various switching schemes. Experimental validation of proposed extended switched inductor quasi Z source inverter suited for photovoltaic system is also discussed in this chapter.

4.2 EXISTING QUASI Z SOURCE INVERTERS

To analyze the family of quasi Z source inverters, the basic topologies of voltage and current fed ZSI are seen first as a reference, which is described below.

Voltage and current fed Z source inverters are most common topologies for PV systems. The voltage fed ZSI has some significant drawbacks such as the input current is discontinuous in boost mode and the
capacitors must sustain a high voltage, whereas in current fed ZSI, inductors must sustain high currents. Also, control complexity is an issue, when ZSI is used in a back to back configuration due to the coupling of the inverter switching functions. A three phase voltage fed ZSI with discontinuous input current and current fed ZSI with continuous input current are shown in Fig 4.1 and Figure 4.2 respectively.

![Figure 4.1 Voltage fed ZSI with discontinuous input current](image1)

![Figure 4.2 Current fed ZSI with continuous input current](image2)
Four basic topologies of quasi Z source inverters [Joel Anderson et al. (2008)] are discussed in section 4.2.1 and 4.2.2, a preliminary study needed for the analysis of improved qZSI topologies are discussed in the later sections of this chapter.

4.2.1 Voltage Fed qZSI with Continuous and Discontinuous Input Current

Voltage fed qZSI topologies with continuous and discontinuous input current shown in Figures 4.3 and 4.4 respectively, are similar with the voltage fed ZSI, and can be made bidirectional by replacing the diode, D₁, with a bidirectional conducting, unidirectional blocking switch. The qZSI, shown in Figure 4.3, when compared to the ZSI shown in Figure 4.1, has lower dc voltage on capacitor C₂ as well as continuous input current, while the qZSI shown in Figure 4.4, has lower dc voltage on capacitors C₁ and C₂, however, the input current is discontinuous.

Figure 4.3 Voltage fed qZSI with continuous input current
4.2.2 Current Fed qZSI with Continuous and Discontinuous Input Current

Current fed qZSI topologies shown in Figures 4.5 and 4.6 are similar to current fed ZSI shown in Figure 4.2, and bidirectional with the diode, $D_1$. Current fed qZSIs shown in Figures 4.5 and 4.6 have lower current in inductors $L_1$ and $L_2$. 
4.2.3 Simulation Results and Discussions

Simulations are carried out for above discussed topologies for the given input dc voltage of 70 V with $L_1 = L_2 = 2 \text{ mH}$ and $C_1 = C_2 = 20 \mu\text{F}$ and filter values of $L_f = 10 \text{ mH}$ and $C_f = 2000 \mu\text{F}$ with a resistive load of $10 \Omega$ yields output a.c voltage (peak value) for various switching schemes with switching frequency, $f_s = 20 \text{ kHz}$ and modulation index of value 1.0 are tabulated in Table 4.1.

Table 4.1 Output ac voltages and THD’s of qZSI topologies under simple boost switching scheme

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Inverter Topologies</th>
<th>$V_{\text{out}}$ (in volts)</th>
<th>$V_{\text{THD}}$ (in %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Voltage fed ZSI with discontinuous input current</td>
<td>115.80</td>
<td>1.81</td>
</tr>
<tr>
<td>2</td>
<td>Voltage fed qZSI with continuous input current</td>
<td>115.80</td>
<td>1.81</td>
</tr>
<tr>
<td>3</td>
<td>Voltage fed qZSI with discontinuous input current</td>
<td>115.80</td>
<td>1.81</td>
</tr>
<tr>
<td>4</td>
<td>Current fed ZSI with continuous input current</td>
<td>45.16</td>
<td>1.90</td>
</tr>
<tr>
<td>5</td>
<td>Current fed qZSI with continuous input current</td>
<td>42.77</td>
<td>0.81</td>
</tr>
<tr>
<td>6</td>
<td>Current fed qZSI with discontinuous input current</td>
<td>43.21</td>
<td>0.77</td>
</tr>
</tbody>
</table>
Analysis can also be made by finding the voltage stress across the capacitors for the given input conditions. For voltage fed ZSI, the voltage stress across $C_1$ and $C_2$ is 34.62 V and for voltage fed qZSI with continuous and discontinuous input current, $C_1$ and $C_2$ values are 38 V and 35.38 V respectively. However, output phase voltage of voltage fed ZSI/qZSI topologies has the same value of 115.80 V with a THD value of 1.81 %.

In the case of current fed ZSI, voltage stress across $C_1$ and $C_2$ is 11.36 V, if $L_1 & L_2 = 2 \, \text{mH}$. On the other hand, the voltage stress across $C_1$ and $C_2$ will be different with the values of 40.65 V and 18.97 V, if $L_1$ and $L_2$ is changed to 1 mH. The current fed qZSI with continuous input current have the voltage stress across the capacitors $C_1$ and $C_2$ of value, 27.88 V and 0 V, if $L_1 & L_2 = 2 \, \text{mH}$. On the other hand, the voltage stress across $C_1$ and $C_2$ will be different with the values of 83.35 V and 0 V, if the front end inductor value changed to 1 mH. The current fed qZSI with discontinuous input current have voltage stress across its single capacitor C to have the value of 162.8 V. However in all the cases the output phase voltage of current fed ZSI/qZSI topologies has the values ranging from 43 - 45 V.

Voltage stress across Z network capacitors of voltage fed ZSI/qZSI topologies have the uniform value, since the number of capacitors are the same, placed at different locations based upon the type of topology, whereas it is different in the case of current fed ZSI/qZSI topologies due to passive component count and location.

It can be also stated that voltage fed qZSI have better performance than the current fed qZSI in terms of voltage boosting ability.
Figure 4.7 and Figure 4.8 shows the output phase voltage waveforms of voltage and current fed qZSI respectively. The other topologies of qZSI discussed in this section have similar output a.c phase voltage (peak value) waveforms as that of Figure 4.7 and Figure 4.8, so they are not given.

Figure 4.7  Simulated output voltage waveform of voltage fed qZSI

Figure 4.8  Simulated output voltage waveform of current fed qZSI
From the simulation results, it is also observed that the other switching schemes under discussion viz., simple PWM and space vector PWM also exhibit the same characteristics for the basic qZSI topologies, as given in Table 4.2. Voltage stress analysis across the capacitors of Z network of the topologies discussed under these switching schemes have the same characteristics as that of the earlier, so it is avoided.

Table 4.2  Output ac voltages and THD’s of qZSI topologies under simple PWM and space vector switching scheme

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Inverter Topologies</th>
<th>$V_{out}$ (in volts)</th>
<th>$V_{THD}$ (in %)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Voltage fed ZSI with discontinuous input current</td>
<td>116.50</td>
<td>2.13</td>
</tr>
<tr>
<td>2</td>
<td>Voltage fed qZSI with continuous input current</td>
<td>116.50</td>
<td>2.13</td>
</tr>
<tr>
<td>3</td>
<td>Voltage fed qZSI with discontinuous input current</td>
<td>116.50</td>
<td>2.13</td>
</tr>
<tr>
<td>4</td>
<td>Current fed ZSI with continuous input current</td>
<td>45.33</td>
<td>2.26</td>
</tr>
<tr>
<td>5</td>
<td>Current fed qZSI with continuous input current</td>
<td>42.83</td>
<td>0.98</td>
</tr>
<tr>
<td>6</td>
<td>Current fed qZSI with discontinuous input current</td>
<td>43.29</td>
<td>0.77</td>
</tr>
</tbody>
</table>

4.3  EXISTING EXTENDED BOOST QUASI Z SOURCE INVERTERS

Four qZSI boost inverter topologies namely diode and capacitor assisted qZSI with continuous and discontinuous current [Chandana Jayampathi Gajanayake et.al (2010)] are analyzed in this section with their extensions. Also its combination, hybrid topology is also analyzed.

4.3.1  Diode Assisted Extended Boost qZSI Topologies

Two diode assisted qZSI boost inverter topologies, namely, the continuous current and discontinuous current diode assisted extended boost
qZSI topologies are analyzed under this category. Figure 4.9(a) shows the continuous current topology and it can be extended to have a high boost by cascading more stages, as shown in Figure 4.9(b). This extended topology comprises an additional inductor, a capacitor and two diodes to the first extension. The operating principle of this additional impedance network is similar to that found in the cascaded boost converters. The added impedance network provides the boosting function without disturbing the operation of the inverter. Figure 4.10 shows the discontinuous current topology.

(a)

(b)

Figure 4.9  Diode assisted extended boost continuous current qZSI
(a) First Extension (b) Second Extension
Figure 4.10 Diode assisted extended boost discontinuous current qZSI
(a) First Extension (b) Second Extension
4.3.2 Capacitor Assisted Extended Boost qZSI Topologies

In capacitor assisted extended boost qZSI topology, the diode $D_3$ is replaced with a capacitor and four topological variations are derived as continuous and discontinuous input current forms, as shown in Figure 4.11 (a) – (d).

![Figure 4.11](image-url)
Figure 4.11 Capacitor assisted extended-boost qZSI topologies
(a) Continuous current first extension. (b) Discontinuous current first extension. (c) Continuous current second extension (d) Discontinuous current second extension
4.3.3 Hybrid Extended Boost qZSI Topologies

Both diode assisted and capacitor assisted techniques are combined to have four topologies of hybrid extended boost topologies, as shown in Figure 4.12 and 4.13.

Figure 4.12 Hybrid extended boost continuous current qZSIs
(a) First extension (b) Second extension
Figure 4.13 Hybrid extended boost discontinuous current qZSIs
(a) First extension (b) Second extension

4.3.4 Simulation Results and Discussions

Extensive simulations are carried out for the open loop configuration of the above topologies discussed in sections 4.3.1, 4.3.2 and 4.3.3 in MATLAB/SIMULINK environment and the results are obtained. For
all the topologies, an input dc voltage of 70V and Z source network parameters, L=2mH, C=20μF (all dc side inductors and capacitors) are selected as input parameters. A resistive load of 10Ω is connected and the output phase voltage (peak value) are obtained for the various switching schemes of switching frequency, $f_s = 20$ kHz and modulation index of value 1.0, are obtained as given in Tables 4.3 and 4.4, where the voltage boosting capability and THD of each topology are compared.

From simulation results, it is observed that all the switching schemes produce sinusoidal output waveforms with very similar peak voltages, so the results pertained to simple boost switching scheme is alone mentioned. Also varying the dc side capacitor in the front end of the inverter further boosts the voltage in these topologies and the parasitic resistance of the inductors leads to conduction losses and voltage drop, if high values of inductors are used.

**Table 4.3  Output a.c voltages and THD’s of extended boost qZSI topologies in continuous current mode under simple boost switching scheme**

<table>
<thead>
<tr>
<th></th>
<th>Continuous Current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1&lt;sup&gt;st&lt;/sup&gt; Extension</td>
</tr>
<tr>
<td></td>
<td>$V_{out}$ volts</td>
</tr>
<tr>
<td>Diode assisted</td>
<td>114.8</td>
</tr>
<tr>
<td>Capacitor assisted</td>
<td>88.4</td>
</tr>
<tr>
<td>Hybrid</td>
<td>112.8</td>
</tr>
</tbody>
</table>
Table 4.4  Output a.c voltages and THD’s of extended boost qZSI topologies in discontinuous current mode under simple boost switching scheme

<table>
<thead>
<tr>
<th></th>
<th>Discontinuous current</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1st Extension</td>
<td>2nd Extension</td>
<td></td>
</tr>
<tr>
<td>V_out volts</td>
<td>V_THD %</td>
<td>V_out volts</td>
<td>V_THD %</td>
</tr>
<tr>
<td>Diode assisted</td>
<td>107.8</td>
<td>1.61</td>
<td>141.3</td>
</tr>
<tr>
<td>Capacitor assisted</td>
<td>79.41</td>
<td>1.79</td>
<td>104.68</td>
</tr>
<tr>
<td>Hybrid</td>
<td>98.8</td>
<td>1.64</td>
<td>127.4</td>
</tr>
</tbody>
</table>

4.4 MODIFIED TOPOLOGIES OF SWITCHED INDUCTOR Z SOURCE INVERTER

4.4.1 Switched Inductor Z Source Inverter

Switched Inductor Z Source Inverter (SLZSI) [Miao Zhu et.al (2010)] shown in Figure 4.14 has a structure with an addition of six diodes and two inductors, compared to the classical Z source inverter.

Figure 4.14 Switched inductor Z source inverter
SLZSI consists of four inductors, two capacitors and six diodes. Both the top and bottom switched inductor (SL) cells are used to store and transfer energy from capacitors to dc bus under the switching action of the main circuit to increase the voltage boost inversion ability.

4.4.2 Switched Inductor quasi Z Source Inverter

Figure 4.15 shows that the Switched Inductor quasi Z Source Inverter (SLqZSI) topology [Minh-Khai Nguyen et.al (2011)] that provides inrush current suppression, unlike the SLZSI topology, because no current flows to the main circuit at start up; however, the inductors and capacitors in SLqZSI still resonate. This inverter adds only three diodes and one inductor. This inverter has similar states and control strategy as that of SLZSI.

![Figure 4.15 Switched inductor quasi Z source inverter](image)

Figure 4.15 Switched inductor quasi Z source inverter
4.4.3 Embedded Switched Inductor quasi Z Source Inverter

Figure 4.16 shows the Embedded Switched Inductor quasi Z Source Inverter (ESLqZSI) with two isolated dc sources [Minh-Khai Nguyen et.al (2011)]. Embedding the dc sources (either one or two sources operating at an instant) in SLqZSI can connect the sources directly to the inductors of impedance network; therefore the dc input current flows smoothly.

The topologies discussed in the sections 4.2, 4.3 and 4.4 motivate the author to propose a new family of switched capacitor/inductor qZSI topologies having the features of better voltage boosting ability, smooth output waveform quality and expendability in its structure, to be discussed in section 4.5, 4.6. Open loop simulations and experimental verification of proposed extended switched inductor quasi Z source inverter are to be discussed in section 4.7 and 4.8 respectively.
4.5 PROPOSED SWITCHED CAPACITOR Z SOURCE INVERTER TOPOLOGIES

Switched Capacitor quasi Z Source Inverter (SCqZSI) can be realized by replacing the inductor cell of SLqZSI with a capacitor cell as shown in Figure 4.17. With small modifications in the positions of the passive components, this proposed topology has voltage boosting capability. Also the capacitors can minimize the ripple current within the inverter.

![Figure 4.17 Proposed switched capacitor quasi Z source inverter](image)

SCqZSI can be modified to operate with two dc sources by embedding the dc sources within the network. The principle of embedding the dc sources remains the same as in the previous cases but the output characteristics differ for the proposed Embedded SC quasi Z Source Inverter (ESCqZSI) shown in Figure 4.18 and the circuit has an additional advantage of supplying with a smooth dc source, reduced ripple current compared to the SLqZSI.

Extension made to SCqZSI lead to the development of Extended Switched Capacitor quasi Z Source Inverter (XSCqZSI) which can be realized with the addition of two capacitor cells as shown in the Figure 4.19. There is
an inclusion of an inductor in addition to the two capacitors found in the previous topology. The inductor regulates the current as well as filters the dc supply entering into the inverter. The function of the capacitor remains the same as in the previous case.

Figure 4.18 Proposed embedded switched capacitor quasi Z Source inverter

Figure 4.19 Proposed extended switched capacitor quasi Z source inverter
4.6 PROPOSED EXTENDED SWITCHED INDUCTOR TOPOLOGIES

4.6.1 Extended Switched Inductor Z Source Inverter

The Extended Switched Inductor Z Source Inverter (XSLZSI) topology shown in Figure 4.20, introduces more inductors in parallel during shoot-through charging and more inductors in series during non-shoot-through discharging. These generalized orientations can indeed be guaranteed by the diode layout found within each switched-L cell. The cascading procedure also reduces the voltage stress across the capacitors during startup conditions.

Figure 4. 20 Proposed extended switched inductor Z source inverter
4.6.2 Extended Switched Inductor quasi Z Source Inverter

Extended Switched Inductor quasi Z Source Inverter (XSLqZSI) shown in Figure 4.21 has two inductor cells added as shown with capacitors to carry the excess voltage and also feed the inverter with a ripple free current, whose details are briefed in section 4.8.

![Figure 4.21 Proposed extended switched inductor quasi Z source inverter](image)

4.7 SIMULATION RESULTS & DISCUSSIONS OF PROPOSED qZSI TOPOLOGIES

Simulations are carried out for the proposed topologies with the given input voltage of 70V and a resistive load of 10Ω. The performances of the proposed topologies are analyzed for the above input and load conditions by having same inductance and two different values of capacitances at the dc side of the inverter with same switching frequency, $f_s = 20\text{khz}$ and modulation index of value 1 under various switching schemes are tabulated in Tables 4.5 and 4.6.

i) Case: A: \[ L_1=L_2=2\text{mH}; C_1=C_2=20\mu\text{F} \]

ii) Case: B: \[ L_1=L_2=2\text{mH}; C_1=C_2=50\mu\text{F} \]
Table 4.5  Output a.c voltages and THD’s of proposed qZSI topologies for Case A under different switching schemes

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Inverter Type</th>
<th>Simple Boost</th>
<th>Simple PWM</th>
<th>SVPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{out} (volts)</td>
<td>V\textsubscript{THD} (in %)</td>
<td>V\textsubscript{out} (volts)</td>
</tr>
<tr>
<td>1</td>
<td>SLZSI</td>
<td>112.0</td>
<td>1.53</td>
<td>112.8</td>
</tr>
<tr>
<td>2</td>
<td>SLqZSI</td>
<td>112.4</td>
<td>1.66</td>
<td>113.0</td>
</tr>
<tr>
<td>3</td>
<td>ESLqZSI</td>
<td>113.4</td>
<td>1.68</td>
<td>113.9</td>
</tr>
<tr>
<td>4</td>
<td>SCqZSI</td>
<td>88.23</td>
<td>1.41</td>
<td>88.67</td>
</tr>
<tr>
<td>5</td>
<td>ESCqZSI</td>
<td>87.56</td>
<td>1.37</td>
<td>88.09</td>
</tr>
<tr>
<td>6</td>
<td>XSCqZSI</td>
<td>95.97</td>
<td>1.43</td>
<td>96.36</td>
</tr>
<tr>
<td>7</td>
<td>XSLZSI</td>
<td>99.08</td>
<td>1.37</td>
<td>99.68</td>
</tr>
<tr>
<td>8</td>
<td>XSLqZSI</td>
<td>125.1</td>
<td>1.84</td>
<td>125.6</td>
</tr>
</tbody>
</table>

Table 4.6  Output a.c voltages and THD’s of proposed qZSI topologies for Case B under different switching schemes

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Inverter Type</th>
<th>Simple Boost</th>
<th>Simple PWM</th>
<th>SVPWM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>V\textsubscript{out} (volts)</td>
<td>V\textsubscript{THD} (in %)</td>
<td>V\textsubscript{out} (volts)</td>
</tr>
<tr>
<td>1</td>
<td>SLZSI</td>
<td>99.05</td>
<td>1.39</td>
<td>99.73</td>
</tr>
<tr>
<td>2</td>
<td>SLqZSI</td>
<td>109.4</td>
<td>1.57</td>
<td>109.9</td>
</tr>
<tr>
<td>3</td>
<td>ESLqZSI</td>
<td>110.3</td>
<td>1.58</td>
<td>110.7</td>
</tr>
<tr>
<td>4</td>
<td>SCqZSI</td>
<td>79.65</td>
<td>1.49</td>
<td>80.05</td>
</tr>
<tr>
<td>5</td>
<td>ESCqZSI</td>
<td>79.07</td>
<td>1.49</td>
<td>79.56</td>
</tr>
<tr>
<td>6</td>
<td>XSCqZSI</td>
<td>87.67</td>
<td>1.42</td>
<td>88.37</td>
</tr>
<tr>
<td>7</td>
<td>XSLZSI</td>
<td>96.56</td>
<td>1.34</td>
<td>97.18</td>
</tr>
<tr>
<td>8</td>
<td>XSLqZSI</td>
<td>118.7</td>
<td>1.88</td>
<td>119.5</td>
</tr>
</tbody>
</table>
Tables 4.5 and 4.6 show the output phase voltage (peak value) and $V_{THD}$ values for various topologies (Fast Fourier Transform (FFT) analysis) obtained through simulation in steady state condition.

Voltage boost inversion ability (i.e) ratio of output a.c voltage to input d.c voltage is mainly decided by values of $L$ & $C$ used in the Z network. Also voltage stress across the capacitors used in the Z network to be considered.

Voltage boost inversion ability of the switched inductor topologies are high by a factor of 1.6, and switched capacitor topologies have the value ranging from 1.26 to 1.37 and extended SLZSI/SLqZSI topologies by the value of 1.42 and 1.79 respectively. Comparing the $V_{out}$ values for the proposed topologies, from Sl. No. 4 to 8 given in the Table 4.6 and 4.7, the variation in output voltage is 5 – 11 % depending upon the switching scheme. The proposed switched capacitor topologies also provide better voltage output. However, due to frequent failure of capacitors due to high voltage stress across the capacitors which is dealt in the following paragraph, next best topology (i.e) extended switched inductor Z source inverter is chosen for hardware fabrication.

Considering the case A (Table 4.5), switched inductor topologies namely SLZSI, SLqZSI, ESLqZSI have nearly the same voltage boosting characteristics. Finding the voltage stress across Z network capacitors for these topologies, SLZSI have a value of 68.32 V in both the capacitors $C_1$ and $C_2$, nearly the same value as that of the input dc voltage. Voltage stress across Z network capacitors for SLqZSI have the values of 7.492 V and 8.265 V in the capacitors, $C_1$ and $C_2$ respectively, whereas ESLqZSI have the values of 26.74 V and 27.51 V in the capacitors, $C_1$ and $C_2$ respectively. It can be inferred that the voltage stress across the capacitors is very low in SLqZSI, so this topology is a better choice of the three.
Both SCqZSI and ESCqZSI have voltage stress across the capacitors with a value of 206.8 V in its switched capacitor cell and 40.91 V in the remaining capacitor. In the case of XSCqZSI, voltage stress across the capacitors is 203.7 V in all the four capacitors of the switched capacitor cell and 11.85 V in the remaining 2 external capacitors. Here the voltage stress across the capacitors is very high, w.r.t to the input dc voltage. The proposed switched capacitor Z source inverter topologies are used for both boost and buck operations. Therefore, these inverters are reasonably competitive for buck-boost applications with good performances confirmed by simulation.

Voltage stress analysis across the capacitors of XSLZSI have the voltage of values 67.54 V and 65.12 V, whereas XSLqZSI have very minimum voltage stress of value 22.34 V in the capacitor C₁ and 7.155 V and 0.8373 V in its first and extended switched inductor cells respectively. Of the above eight inverter topologies, extended switched inductor quasi Z Source inverter(XSLqZSI) topology have high voltage boosting ability with reduced voltage stress across the capacitors, so it is the best choice for hardware fabrication.

The topology with extended boosting capability has higher THD values than the previous cases. This is obvious because of the increase in the number of passive components that has a direct effect on THD values of the extended boost topologies. A tradeoff between the boosting capability and THD has to be made to have reliable output characteristics.

From Tables 4.5 and 4.6, it is also found that extended switched inductor quasi Z source inverter have better voltage boost compared to other proposed topologies,. Hence experimental verification of the above topology is carried out.
4.8 EXPERIMENTAL VERIFICATION OF PROPOSED EXTENDED SWITCHED INDUCTOR QUASI Z SOURCE INVERTER

The topology arrangement of the proposed extended SLqZSI is shown in Figure 4.21 which consists of five inductors \((L_1, L_2, L_3, L_4\) and \(L_5\)), three capacitors \((C_1, C_2\) and \(C_3\)) and seven diodes \((D, D_1, D_2, D_3, D_4, D_5\) and \(D_6\)). The combination of \(L_2–L_3–D_1–D_2–D_3\) acts as a basic switched-inductor cell and \(L_4–L_5–D_4–D_5–D_6\) will be the extended switched-inductor cell.

The cascading of cells are designed on the bases of \(N\) cells in cascaded structure using \(n = N + 1\) inductors. Beginning with the extended SL cell structure, the generalized concept is to introduce more inductors in series during non shoot-through charging and less inductors in parallel during shoot-through discharging. These can indeed be guaranteed by the diode layout found within each switched-L cell. The cascading of cells also reduces the voltage stress across the capacitors during start conditions. Besides providing high gain, this extended SLqZSI might still have some convincing advantages over those existing Z source inverters, when they are commanded to produce the output voltage from the same given input voltage. It is also obvious that multi-cell switched-L network results in a reduction of the capacitive voltage stress.

The operating states of the proposed extended SLqZSI’s impedance network are classified into the non shoot-through state and the shoot-through state, respectively shown in the Figure 4.22.
Figure 4.22 Operating states of proposed extended SLqZSI:
(a) non shoot-through and (b) shoot-through state

During the non shoot-through state, $D$, $D_1$ and $D_5$ are ON, while $(D_2, D_3)$ and $(D_4, D_6)$ are OFF in the cells 1 and 2 respectively. $(L_2, L_3)$ and $(L_4, L_5)$ are connected in series. The capacitors $C_1$, $C_2$ and $C_3$ are charged, while the inductors $(L_1 – L_5)$ transfer energy from the dc voltage source to the main circuit shown in Figure 4.22 (a).

The corresponding voltages across $L_2 – L_5$ in this state are $V_{L2-non}$ to $V_{L5-non}$, respectively as

\[ V_{L1} = V_{C1} - V_{dc} \]  \hspace{1cm} (4.1)

\[ V_{L2} = V_{L2-non} = V_{C2} - V_{L3-non} \]  \hspace{1cm} (4.2)
\[ V_{L3} = V_{L3\text{-non}} = V_{C2} - V_{L2\text{-non}} \quad (4.3) \]
\[ V_{L4} = V_{L4\text{-non}} = V_{C3} - V_{L5\text{-non}} \quad (4.4) \]
\[ V_{L5} = V_{L5\text{-non}} = V_{C3} - V_{L4\text{-non}} \quad (4.5) \]
\[ V_{PN} = V_{C1} + V_{C2} + V_{C3} \quad (4.6) \]

In the shoot-through state, as shown in Figure 4.22 (b), the inverter side is shorted by both the upper and lower switching devices of any phase leg. During the shoot-through state, \(D, D_1\) and \(D_5\) are OFF, while \((D_2, D_3)\) and \((D_4, D_6)\) are ON in the cells 1 and 2 respectively. \((L_2, L_3)\) and \((L_4, L_5)\) are connected in parallel. The capacitors \(C_1, C_2\) and \(C_3\) are discharged, while the inductors \(L_1 - L_5\) stores the energy as

\[ V_{L1} = -V_{C2} - V_{C3} - V_{dc} \quad (4.7) \]
\[ V_{L2}/2 = V_{L3}/2 = -V_{C1} \quad (4.8) \]
\[ V_{L4} = V_{L5} = 0 \quad (4.9) \]

Applying the volt-second balance principle to \(L_1\) and \(L_5\) to the equations from (4.1) to (4.9), we get

\[ V_{L2\text{-non}} = V_{L3\text{-non}} = \frac{-D}{1-D} V_{C1} + V_{C2} \quad (4.10) \]
\[ V_{C2} = \frac{2D}{1-D} V_{C1} \quad (4.11) \]
\[ V_{L4\text{-non}} = V_{L5\text{-non}} = \frac{-D}{1-D} V_{C2} + V_{C3} \quad (4.12) \]
The peak dc link voltage across the inverter main circuit is expressed in (4.6) and can be rewritten as follows:

\[ V_{ph} = V_{C1} + V_{C2} + V_{C3} = \frac{1-2D}{1-2D-D^2}V_{dc} BV_{dc} \]

The boost factor, B of the proposed inverter is defined by

\[ B = \frac{1-2D}{1-2D-D^2} = \frac{1-2(T_s/T)}{1-2(T_s/T) - (T_s/T)^2} \]

To verify the operation of proposed extended SL quasi Z source inverter, simulations are performed in MATLAB/SIMULINK model, where the solver is chosen as variable step discrete with step of 2.0 μs with the following system parameters as: \( V_{dc} = 36 \text{ V} \); \( L_1 \) to \( L_5 = 50 \text{ mH} \); \( C_1, C_2 \) and \( C_3 = 1000 \text{ μF} \) and the switching frequency, \( f_s = 20 \text{ KHz} \); three phase output filters, \( L_f = 10 \text{ mH} \) and \( C_f = 1000 \text{ μf} \) and the three phase balanced load is \( R_L = 10 \Omega/\text{phase} \). The IGBT models whose internal resistance \( R_{on} = 10^{-3} \Omega \) and snubber resistance \( R_s = 10^5 \Omega \) are used as the switching devices. Table 4.7 provides the parameters chosen for the above proposed extended switched-inductor quasi Z-source inverter and the simulation are carried out under simple PWM switching scheme.
Table 4.7 Experimental parameters of the proposed XSLqZSI

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC voltage</td>
<td>36 V</td>
</tr>
<tr>
<td>Z-source network</td>
<td>L₁=L₂=L₃=L₄=L₅=50 mH</td>
</tr>
<tr>
<td></td>
<td>C₁=C₂=C₃=1000 µf</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>20 KHz</td>
</tr>
<tr>
<td>Three phase resistive load</td>
<td>10 Ω/ Phase</td>
</tr>
</tbody>
</table>

Simulation results of the proposed topology are presented. The output a.c phase voltage (peak value) obtained through simulation for the proposed extended switched inductor quasi Z source inverter are 43.11 V, 42.83 V and 42.66 V for the phases A, B and C respectively as shown in Figure 4.23. Inductor current and dc link voltage waveform is also presented in Figure 4.24 and Figure 4.25. Figure 4.26 shows the switching sequence and Figure 4.27 shows the THD values through FFT analysis.

Figure 4.23 Simulated output ac voltage waveform of proposed XSLqZSI
Figure 4.24 Simulated inductor current waveform of proposed XSLqZSI (Scale: Y axis – 1 A/div)

Figure 4.25 Simulated dc link voltage waveform of proposed XSLqZSI (Scale: Y axis – 20 V/div)

Figure 4.26 Switching sequence of proposed XSLqZSI
Figure 4.27 FFT spectrum of proposed XSLqZSI for three phases
Simulation results are validated through the experimental setup and the block diagram of the overall setup is shown in Figure 4.28

**Figure 4.28 Block diagram of proposed XSLqZSI**

In this scaled down model, the PV panels (2 Nos.) are connected as input to the extended SL impedance network, which is then connected to the main inverter circuit to feed the load. The switching pulses of the main inverter circuit are given from PWM pulse circuit generated through simple PWM control strategy. Shoot through pulses to turn ON the switches of the same phase leg are obtained through a separate circuit which is connected to the main PWM pulse generator circuit.

Connection diagram of isolation opto coupler, PWM pulse generator, shoot through pulse generator, and impedance network are shown in Figure 4.29 to Figure 4.31 with the IC details and specifications.
Figure 4.29 shows the connection diagram of optocoupler circuit, protection part of the system which triggers the proposed inverter circuit. IC MCT2E is used for the isolation optocoupler. Various components like optocoupler diodes and RLC passive elements are used in the isolation optocoupler.

Figure 4.29 Opto coupler circuit of proposed XSLqZSI
The PWM pulse generator circuit of the proposed XSLqZSI uses CMOS IC’s namely CD 4578, CD 4075, CD 4050 for counting, buffering actions and LM 3524 and LM 358 for pulse width modulation and amplification purposes and its connection diagram is shown in the Figure 4.30.

Figure 4.30 PWM pulse generator circuit of proposed XSLqZSI
The shoot through pulse generator of the proposed XSLqZSI uses CMOS IC’S like CD4069, CD 4071 and LM 158 for inverter, gate circuits and dual operational amplification purposes and its connection diagram is shown in the Figure 4.31 as

![Image of connection diagram](image.png)

**Figure 4.31 Shoot through pulse generator of proposed XSLqZSI**

Various operating units like PWM pulse generator, shoot through pulse generator, isolation opto coupler, and impedance network are assembled to form scaled down hardware model of the proposed extended switched inductor quasi Z source inverter which is shown in Figure 4.32. The components and IC’s used in these units are shown in Figures 4.33 to 4.36
Figure 4.32 Prototype of proposed extended SL quasi Z source inverter A. Isolation Opto coupler, B. PWM pulse generator, C. Shoot through pulse generator D. Inverter circuit, E. Capacitor and F. Inductor

Figure 4.33 Photograph of isolation Opto coupler
Figure 4.34 Photograph of PWM pulse generator circuit

Figure 4.35 Photograph of shoot through pulse generator circuit
From the constructed laboratory prototype to verify the simulation results of the proposed extended SLqZSI, the experimental setup is observed through the digital signal oscilloscope. Output voltage (phase to phase) is shown in Figure 4.37, which reaches 42 V. The waveforms show distortions due to the heating of the transformers, which power the PWM pulse generator, shoot through pulse generator, isolation opto coupler externally from the input supply mains.

Figure 4.37 Experimental phase to phase voltage waveform of proposed XSLqZSI
The inductor current and dc link voltage are shown in Figure 4.38 and Figure 4.39 respectively.

![Figure 4.38 Experimental inductor current waveform of proposed XSLqZSI](image)

![Figure 4.39 Experimental dc link voltage waveform of proposed XSLqZSI](image)

From the fig. 4.38, it is observed that the inductor current is less at the start conditions and have reduced stress on these passive components. The simulation results almost matches with the experimental results and further improvement needed for large sized Z source inverters.
The gate pulses of the six switches ($S_1$ to $S_6$) proposed XSLqZSI topology are shown in Figure 4.40.

Figure 4.40 Gate pulse of switches of proposed XSLqZSI (S1 to S6)
4.9 SUMMARY

Extensive simulations have been carried out for extended boost qZSI topologies in both continuous and discontinuous current modes of operation. Based on the simulation, it is concluded that these topologies are most suitable for photovoltaic systems with better voltage boosting ability and also provides an option for topology expansion for additional boost.

A new family of switched inductor/capacitor qZSI topologies is proposed by the combined analysis of switched inductor ZSI topologies with extended boost qZSI topologies. Open loop simulations have been carried out under various switching schemes for these proposed topologies produces better voltage boost.

Experimental validation of proposed extended switched inductor quasi Z source inverter has better inversion and voltage boosting ability with reduced stress on the passive components at start conditions. These proposed topologies are suitable for photovoltaic or fuel cell applications, where a low input voltage is inverted to a high ac output voltage.